CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

Department of Electronics & Communication Engineering

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(An Autonomous Institute)

ACADEMIC REGULATIONS FOR M.TECH. DEGREE COURSE

(Applicable for Students admitted from the academic year 2014-2015)

Applicable for the students of M. Tech. (Regular) Course from the Academic Year 2014-15 and onwards

The M. Tech. degree shall be conferred on candidates who are admitted to the program and who fulfil all the requirements for the award of the degree.

1.0 Eligibility for Admissions

Admission to the above program shall be made subject to eligibility, qualification and specialization as prescribed by the State Government from time to time.

2.0 Award of M. Tech. degree

2.1 A student shall be declared eligible for the award of the M. Tech. Degree, if he pursues a course of study in not less than two and not more than four academic years.

2.2 A student, who fails to fulfill all the academic requirements for the award of the degree within four academic years from the year of his admission, shall forfeit his seat in M. Tech. course.

2.3 The student shall register for all 88 credits and secure all the 88 credits.

2.4 The minimum instruction days in each semester are 90.

2.5 The medium of instruction and examination shall be English.

3.0 A. Courses of Study

The following specializations are offered at present for the M. Tech. course of study.

1. Bio-Technology
2. Embedded Systems
3. Power Electronics
4. Structural Engineering
5. Computer Science & Engineering
6. Machine Design

and any other course as approved by the College/ University/AICTE from time to time.

B. Departments offering M.Tech. programmes with specializations mentioned below:

Sl. No.	Department	M.Tech Course
1	Bio-Technology	Bio-Technology
2	ECE	Embedded Systems
3	EEE	Power Electronics
4	Civil	Structural Engineering
5	CSE	Computer Science & Engineering
6	Mechanical	Machine Design

4.0 Minimum Instructional Days and Attendance

The programs are offered on a unit basis with each subject being considered a unit.

4.1 The minimum instruction period for each semester shall be 90 clear instruction days.

4.2. A student shall be eligible to write semester end examinations if he acquires a minimum of 75% of attendance **in each of all the subjects**.

4.3. Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester shall be granted by the Institute Academic Committee.

4.4 Shortage of attendance below 65% in aggregate shall not be condoned.

4.5 Students whose shortage of attendance is not condoned in any semester are not eligible to write their end semester examination of subjects of the corresponding semester and their registration shall stand cancelled.

4.6. A fee as prescribed by the Institute Academic Committee shall be payable towards condonation of shortage of attendance.

4.7. A candidate shall put in a minimum required attendance, in at least 50% of the theory subjects in the present semester to get promoted to the next semester. In order to qualify for the award of the M. Tech. Degree, the candidate shall complete all the academic requirements of the subjects, as per the course structure.

4.8. A student will be promoted to the next semester if he satisfies the attendance requirement of the present semester including the days of attendance in sports, games, NCC and NSS activities subject to a maximum of 15 instructional days in a semester. Prior permission of the Head of the Department in writing shall be obtained by the students to avail the attendance from above mentioned activities.

5. Evaluation

The performance of the candidate in each semester shall be evaluated subject-wise, with a maximum of 100 marks for theory and 100 marks for practicals, on the basis of Internal Evaluation and End Semester Examination.

For the theory subjects 60 marks shall be awarded based on the performance in the End Semester Examination and 40 marks shall be awarded based on the Internal Evaluation. For internal evaluation there shall be the two internal examinations conducted-one in the middle of the semester and the other immediately after the completion of instruction. Each internal examination shall be conducted for a total duration of 120 minutes. The final marks secured by each candidate in the internal evaluation is arrived at by giving a weightage of 70% to the best secured internal examination and 30% weightage to the least secured internal examination. A student who is absent for any internal examination for any reason what so ever shall be deemed to have secured ‘zero’ marks in the test/ examination and no makeup test/ examination shall be conducted.

5.1

Internal Examination

Part A (20 Marks)

4 questions of 5 marks each (All questions are compulsory).

Part B (20 Marks)

4 questions to be answered out of 6 questions, each question carry 5 marks.

External Examination

Part A (20 Marks)

5 questions (1 question from each unit) of 4 marks each (Compulsory questions)

Part B (40 Marks)

5 questions (1 question from each unit with internal choice) each question carries 8 marks.

5.2 For practical subjects, 60 marks shall be awarded based on the performance in the End Semester Examinations. 40 marks shall be awarded in internal evaluation out of which 20 marks shall be for day to day evaluation and 20 marks shall be for internal examination.

5.3 There shall be seminar presentation each during of I semester as well as II semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Departmental Academic Committee consisting of Head of the Department, Supervisor and two other senior faculty members of the department. For each Seminar there will be only internal evaluation of 50 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

5.4 There shall be a Comprehensive Viva-Voce in III Semester. The Comprehensive Viva-Voce will be conducted by a Committee consisting of Head of the Department and two Senior Faculty members of the Department. The Comprehensive Viva-Voce is intended to assess the students' understanding of various subjects he has studied during the M. Tech. course of study. The Comprehensive Viva-Voce is evaluated for 100 marks by the Committee. There are no internal marks for the Comprehensive Viva-Voce. A candidate has to secure a minimum of 50% of marks to be declared successful.

5.5 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% marks in the End semester Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

5.6 In case the candidate does not secure the minimum academic requirement in any subject (as specified in 5.5) he has to reappear for the End semester Examination in that subject. A candidate shall be given one chance to re-register for each subject provided the internal marks secured by a candidate are less than 50% and so has failed in the end examination. In such a case, the candidate must re-register for the subject(s) and secure the required minimum attendance. The candidate's attendance in the re-registered subject(s) shall be calculated separately to decide upon his eligibility for writing the end examination in those subject(s). In the event of the student taking another chance, his internal marks and end examination marks obtained in the previous attempt stand cancelled.

5.7 In case the candidate secures less than the required attendance in any subject, he shall not be permitted to write the End Examination in that subject. He shall re-register the subject when next offered.

5.8 Laboratory examination for M. Tech. courses for 60 marks must be conducted with two Examiners, one of them being the Laboratory Class Teacher and the second examiner shall be appointed by the Controller of Examinations in consultation with the HOD.

6.0 Evaluation of Project / Dissertation Work:

The work on the project shall be initiated in the beginning of the III semester and the duration of the project is for two semesters. A Project Review Committee (PRC) shall be constituted comprising of Head of the Department and three other senior faculty members concerned with the M.Tech programme. The student can initiate the Project work only after obtaining the approval of PRC. This process is to be completed within four weeks of commencement of III semester.

6.1. The candidate shall be required to submit thesis or dissertation after taking up a topic approved by the Project Review Committee.

6.2 Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the previous semesters and after obtaining the approval of the Institute Academic Committee.

6.3 After satisfying 6.2, a candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work to the PRC for its approval.

6.4 If the candidate wishes to change his supervisor or topic of the project he can do so with approval of PRC. However, the PRC shall examine whether the change of topic/supervisor leads to a major change of his initial plans of project proposal. If so his date of registration for the project work starts from the date of change of supervisor or topic as the case may be.

6.7 Project work and Dissertation:

A candidate is permitted to submit project dissertation only after successful completion of all subjects (theory and practical), seminars, comprehensive viva-voce, and after the approval of PRC, not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC, the candidate shall submit the draft copy of thesis to the Head of the Department and shall make an oral presentation before the PRC. Along with the draft thesis the candidate shall submit draft copy of a paper in standard format fit for publication in Journal / Conference, based on the project thesis, to the Head of the Department with due recommendation of the supervisor.

6.7.1 Four copies of the Project Dissertation certified by the Supervisor and Head of the Department shall be submitted to the College.

6.7.2 The dissertation shall be adjudicated by one examiner selected by the College. In case the thesis is found to be acceptable; viva-voce will be arranged. For this, Head of Department shall submit a panel of 3 examiners, who are eminent in that field, with the help of the PRC. The Controller of Examinations of the college in consultation with the College Academic Committee shall nominate the examiner.

6.7.3 If the report of the examiner is not favourable, the candidate shall revise and resubmit the dissertation, in the time frame as prescribed by PRC. If the report of the examiner is unfavourable again, the thesis shall be summarily rejected. The candidate can re-register only once for conduct of project and evaluation of dissertation, and will go through the entire process as mentioned above. The total duration for the M.Tech program is limited to four years.

6.7.4 If the report of the examiner is favourable, viva-voce examination shall be conducted by a Board consisting of the Head of the Department, Supervisor and the Examiner who adjudicated the Dissertation. The Board shall jointly report the student's performance in the project work as –

(a) Excellent, or

(b) Good, or

(c) Satisfactory, or

(d) Unsatisfactory,

as the case may be. In case, the student fails in the viva-voce examination, or gets the Unsatisfactory grade, he can re-appear only once for the viva-voce examination, as per the recommendations of the Board. If he fails at the second viva-voce examination, the candidate can re-register only once for conduct of project and evaluation of Dissertation, and will go through the entire process as mentioned above. The total duration for the M.Tech program is limited to four years.

7.0 Award of Degree and Class

After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree he shall be placed in one of the following four classes:

Class Awarded	% of marks to be secured
First Class with Distinction	70% and above
First Class	Below 70% but not less than 60%
Second Class	Below 60% but not less than 50%

The marks in internal evaluation and end examination shall be shown separately in the memorandum of marks.

8. Withholding of Results

If the student has not paid the dues, if any, to the institution or if any case of indiscipline is pending against him, the result of the student will be withheld and he will not be allowed into the next semester. His degree will be withheld in such cases.

9. Transitory Regulations

9.1 Discontinued, detained, or failed candidates are eligible for admission to two earlier or equivalent subjects at a time as and when offered.

9.2 The candidate who fails in any subject will be given two chances to pass the same subject; otherwise, he has to identify an equivalent subject as per the academic regulations.

6. General

i. Wherever the words "he", "him", "his", occur in the regulations, they include "she", "her", "hers".

ii. .The academic regulation should be read as a whole for the purpose of any interpretation.

10.3 .In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Academic Council is final.

10.4 .The college may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the college.

MALPRACTICES RULES

DISCIPLINARY ACTION FOR IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/ Improper conduct	**Punishment**
1.(a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled.
3.	Impersonates any other candidate in	The candidate who has impersonated shall be expelled

	connection with the examination.	from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate Who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all end semester examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4.	Smuggles the answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all end semester Examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks	Cancellation of the performance in that subject
6.	Refuses to obey the orders of the Chief Superintendent/Assistant– Superintendent / any officer on duty or misbehaves or	In case of students of the college, they shall be expelled from examination halls and cancellation

	creates disturbance of any kind in and around the or organizes a walk out or instigates others **to** examination hall walk out, or threatens the officer- in-charge or any person on duty in or outside the examination hall of any injury**,** to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer- in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates are also debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of

		That semester/year. The candidate is also debarred and forfeits the seat.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	If the student belongs to the college, expulsion from the examination performance in that subject and all other subjects hall and cancellation of the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for other remaining examinations of the subjects of that semester/year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the College Academic Committee for further action to award suitable punishment.	

Malpractices identified by squad or special invigilators

Punishments to the candidates as per the above guidelines.

Malpractice identified at Spot center during valuation

The following procedure is to be followed in the case of malpractice cases detected during valuation, scrutiny etc. at spot center.

1) Malpractice is detected at the spot valuation. The case is to be referred to the malpractice committee. Malpractice committee will meet and discuss/question the candidate and based on the evidences, the committee will recommend suitable action on the candidate.
2) A notice is to be served to the candidate(s) involved through the Principal to his address and to the candidate(s) permanent address regarding the malpractice and seek explanations.
3) The involvement of staff who are in charge of conducting examinations, invigilators valuing examination papers and preparing / keeping records of documents relating to the examinations in such acts (inclusive of providing in correct or misleading information) that infringe upon the course of natural justice to one and all concerned at the examinations shall be viewed seriously and recommended for award of appropriate punishment after thorough enquire.
4) Based on the explanation and recommendation of the committee action may be initiated.

Malpractice committee:

i. Controller of Examinations Chairman
ii. Assistant controller of Evaluation Member
iii. Chief Examiner of the subject/ subject expert Member
iv. Concerned Head of the Department Member
v. Concerned Invigilator Member

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(An Autonomous Institute)

Institute Vision and Mission

Vision:

To be a premier academic institution striving continuously for excellence in technical education, research and technological service to the nation.

Mission:

1. Create and sustain a community of learning in which students acquire knowledge and learn to apply it professionally with a concern for the society.
2. Pursue and disseminate research findings and offer knowledge-based technological services to satisfy the needs of society and the industry.
3. Promote professional ethics, leadership qualities and social responsibilities.

Department Vision and Mission

Vision:

To produce globally competitive engineering graduates with social awareness and become centre of excellence through research in the areas of Electronics & Communication Engineering.

Mission:

- To impart quality education to the students in the domain of Electronics & Communication Engineering and related fields to make them globally competitive.
- To pursue research in Electronics & Communication Engineering and related disciplines in order to serve the needs of the society.
- Develop self-learning abilities and professional ethics to enable them to serve the society.

Program Educational Objectives

1. Excel in their professional career and higher education in Electronics & Communication Engineering and related fields
2. Exhibit leadership through professional ability and team work
3. Adapt to emerging trends for sustained growth in their relevant areas of Interest and exhibit social responsibility

Program Outcomes

1. Ability to apply the knowledge of mathematics, science, engineering fundamentals for the solution of complex engineering problems.
2. Ability to identify, formulates, research literature and analyse complex engineering problems for reaching meaningful conclusions.
3. Ability to design solution for complex engineering problems with appropriate consideration for the society.
4. Ability to use research –based knowledge and research methods including design of experiments to provide valid conclusions.
5. Ability to learn and apply appropriate modern tools for engineering solutions
6. Ability to assess societal, health, safety, legal and cultural issues and the consequent responsibilities and follow them in professional practice.
7. Ability to understand the impact of the professional practices on environment, society and its sustainable development.
8. Ability to apply ethical principles and commit to professional ethics in engineering practice.

9. Ability to function on an inter- disciplinary team.
10. Ability to communicate effectively.
11. Ability to understand engineering and management principles and apply them to one’s own work, as a member and leader in a team, to manage projects.
12. Ability to engage in lifelong learning.

M. Tech. (EMBEDDED SYSTEMS)

COURSE STRUCTURE AND SYLLABUS

R14 Regulation

I SEMESTER

Code	Group	Subject	L	P	Credits
B1201		Embedded System Design	3	0	3
B1202		Microcontrollers for Embedded System Design	3	0	3
B1203		Embedded Real Time Operating Systems	3	0	3
B1204		Embedded C	3	0	3
B1521	Elective -I	Advanced Computer Architecture	3	0	3
B1205		VLSI Technology and Design			
B1206		Embedded Computing			
B1207	Elective -II	Digital System Design	3	0	3
B1522		Soft Computing Techniques			
B1540		Advanced Operating Systems			
B1208	Lab	Embedded C Laboratory	0	3	2
B1209		Seminar	-	-	2
		Total Credits	18	3	22

II- SEMESTER

Code	Group	Subject	L	P	Credits
B1210		Hardware Software Co-Design	3	0	3
B1211		Digital Signal Processors and Architectures	3	0	3
B1212		Embedded Networking	3	0	3
B1213		CPLD and FPGA Architectures and Applications	3	0	3
B1214	Elective - III	Sensors and Actuators	3	0	3
B1215		Wireless Communications and Networks			
B1523		ADHOC AND SENSOR NETWORKS			
B1216	Elective – IV	Multimedia and Signal Coding	3	0	3
B1217		System On Chip Architecture			
B1218		Wireless LANs and PANs			
B1219	Lab	Embedded Systems Laboratory	0	3	2
B1220		Seminar	-	-	2
		Total Credits	18	3	22

III SEMESTER

Code	Group	Subject	L	P	Credits
B1221		Comprehensive Viva	-	-	2
B1222		Project Seminar	0	3	2
B1223		Project work (Continued to next semester)	-	-	18
		Total Credits	-	3	22

IV SEMESTER

Code	Group	Subject	L	P	Credits
B1223		Project work	-	-	22
		Total Credits	-	-	22

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
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M. Tech – I Semester

EMBEDDED SYSTEMS DESIGN

	L	T	P	Credits
B1201	3	1	0	3

UNIT -I:

Introduction to Embedded Systems

Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT -II:

Typical Embedded System:

Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT -III:

Embedded Firmware:

Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT -IV:

RTOS Based Embedded System Design:

Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT -V:

Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS:

1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.

REFERENCE BOOKS:

1. Embedded Systems - Raj Kamal, TMH.
2. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.
3. Embedded Systems – Lyla, Pearson, 2013
4. An Embedded Software Primer - David E. Simon, Pearson Education.

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
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I Semester

MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN

	L	T	P	Credits
B1202	3	1	0	3

UNIT –I:

ARM Architecture:
ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

UNIT –II:

ARM Programming Model – I:
Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT –III:

ARM Programming Model – II:
Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

UNIT –IV:

ARM Programming:
Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT –V:

Memory Management:
Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.

TEXT BOOKS:

1. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.

REFERENCE BOOKS:

1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
I Semester

EMBEDDED REAL TIME OPERATING SYSTEMS

	L	T	P	Credits
B1203	3	1	0	3

UNIT – I:

Introduction

Introduction to UNIX/LINUX, Overview of Commands, File I/O (open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT - II:

Real Time Operating Systems

Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency.

Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT - III:

Objects, Services and I/O

Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT - IV:

Exceptions, Interrupts and Timers

Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT - V:

Case Studies of RTOS

RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, Tiny OS, and Basic Concepts of Android OS.

TEXT BOOKS:

1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011

REFERENCE BOOKS:

1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
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I Semester
EMBEDDED C

	L	T	P	Credits
B1204	3	1	0	3

UNIT – I:

Programming Embedded Systems in C
Introduction ,What is an embedded system, Which processor should you use, Which programming language should you use, Which operating system should you use, How do you develop embedded software, Conclusions

Introducing the 8051 Microcontroller Family
Introduction, What's in a name, The external interface of the Standard 8051, Reset requirements ,Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption ,Conclusions

UNIT – II:

Reading Switches
Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code), Example: Counting goats, Conclusions

UNIT – III:

Adding Structure to the Code
Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example, Example: Restructuring the goat-counting example, Further examples, Conclusions

UNIT – IV:

Meeting Real-Time Constraints
Introduction, Creating 'hardware delays' using Timer 0 and Timer 1, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2?, The need for 'timeout' mechanisms, Creating loop timeouts, Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions

UNIT – V:

Case Study: Intruder Alarm System
Introduction, The software architecture, Key software components used in this example, running the program, the software, Conclusions

TEXT BOOKS:

1. Embedded C - Michael J. Pont, 2nd Ed., Pearson Education, 2008

REFERENCE BOOKS:

1. PICmicro MCU C-An introduction to programming, The Microchip PIC in CCS C - Nigel Gardner

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
I Semester

ADVANCED COMPUTER ARCHITECTURE
(ELECTIVE -I)

	L	T	P	Credits
B1521	3	1	0	3

UNIT -I:

Fundamentals of Computer Design:

Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, Quantitative principles of computer design, Amdahl's law.

Instruction set principles and examples- Introduction, classifying instruction set- memory addressing-type and size of operands, Operations in the instruction set.

UNIT –II:

Pipelines:

Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design:

Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT -III:

Instruction Level Parallelism (ILP) - The Hardware Approach:

Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, High performance instruction delivery- Hardware based speculation.

ILP Software Approach:

Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues - Hardware verses Software.

UNIT –IV:

Multi Processors and Thread Level Parallelism:

Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – Memory architecture, Synchronization.

UNIT –V:

Inter Connection and Networks:

Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture: Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

TEXT BOOKS:

1. John L. Hennessy, David A. Patterson - Computer Architecture: A Quantitative Approach, 3rd Edition, an Imprint of Elsevier.

REFERENCE BOOKS:

1. John P. Shen and Miikko H. Lipasti -, Modern Processor Design : Fundamentals of Super Scalar Processors
2. Computer Architecture and Parallel Processing - Kai Hwang, Faye A.Brigs., MC Graw Hill.

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
I Semester

VLSI TECHNOLOGY AND DESIGN
(ELECTIVE -I)

	L	T	P	Credits
B1205	3	1	0	3

UNIT –I:
Review of Microelectronics and Introduction to MOS Technologies:
MOS, CMOS, BiCMOS Technology.

Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: $I_{ds} - V_{ds}$ relationships, Threshold Voltage V_T, G_m, G_{ds} and ω_o, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Z_{pu}/Z_{pd}, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT –II:
Layout Design and Tools:
Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.
Logic Gates & Layouts:
Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT –III:
Combinational Logic Networks:
Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT –IV:
Sequential Systems:
Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT –V:
Floor Planning:
Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

TEXT BOOKS:
1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A. Pucknell, 2005, PHI.
2. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.

REFERENCE BOOKS:
1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.

   Principals of CMOS VLSI Design – N.H.E Weste, K. Eshraghian, 2nd Ed., Addison Wesley.

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
I Semester

EMBEDDED COMPUTING
(ELECTIVE – I)

	L	T	P	Credits
B1206	3	1	0	3

UNIT –I:
Programming on Linux Platform:
System Calls, Scheduling, Memory Allocation, Timers, Embedded Linux, Root File System, Busy Box. **Operating System Overview**: Processes, Tasks, Threads, Multi-Threading, Semaphore, Message Queue.

UNIT –II:
Introduction to Software Development Tools:
GNU GCC, make, gdb, static and dynamic linking, C libraries, compiler options, code optimization switches, lint, code profiling tools,.

UNIT –III:
Interfacing Modules:
Sensor and actuator interface, data transfer and control, GPS, GSM module interfacing with data processing and display, OpenCV for machine vision, Audio signal processing.

UNIT –IV:
Networking Basics:
Sockets, ports, UDP, TCP/IP, client server model, socket programming, 802.11, Bluetooth, ZigBee, SSH, firewalls, network security.

UNIT –V:
IA32 Instruction Set: application binary interface, exception and interrupt handling, interrupt latency, assemblers, assembler directives, macros, simulation and debugging tools.

TEXT BOOKS:
1. Modern Embedded Computing - Peter Barry and Patrick Crowley, 1st Ed., Elsevier/Morgan Kaufmann, 2012.
2. Linux Application Development - Michael K. Johnson, Erik W. Troan, Adission Wesley, 1998.
3. Assembly Language for x86 Processors by Kip R. Irvine
4. Intel® 64 and IA-32 Architectures Software Developer Manuals

REFERENCE BOOKS:
1. Operating System Concepts by Abraham Silberschatz, Peter B. Galvin and Greg Gagne.
2. The Design of the UNIX Operating System by Maurice J. Bach Prentice-Hall
3. UNIX Network Programming by W. Richard Stevens

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
I Semester

DIGITAL SYSTEM DESIGN
(ELECTIVE -II)

B1207	**L**	**T**	**P**	**Credits**
	3	1	0	3

UNIT -I:

Minimization and Transformation of Sequential Machines:
The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines.
Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

UNIT -II: Digital Design:
Digital Design Using ROMs, PALs and PLAs , BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

UNIT -III:

SM Charts:
State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

UNIT -IV:

Fault Modeling & Test Pattern Generation:
Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model.
Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

UNIT -V:

Fault Diagnosis in Sequential Circuits:
Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment

TEXT BOOKS:

1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.
3. Logic Design Theory – N. N. Biswas, PHI

REFERENCE BOOKS:

1. Switching and Finite Automata Theory – Z. Kohavi , 2nd Ed., 2001, TMH
2. Digital Design – Morris Mano, M.D.Ciletti, 4th Edition, PHI.
3. Digital Circuits and Logic Design – Samuel C. Lee , PHI

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
I Semester

SOFT COMPUTING TECHNIQUES
(ELECTIVE -II)

B1522	**L**	**T**	**P**	**Credits**
	3	1	0	3

UNIT –I: Introduction:
Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rule-based systems, the AI approach, Knowledge representation - Expert systems.

UNIT –II:
Artificial Neural Networks:
Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron, Learning and Training the neural network, Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations, Hopfield network, Self-organizing network and Recurrent network, Neural Network based controller.

UNIT –III:
Fuzzy Logic System:
Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning, Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification, Fuzzy knowledge and rule bases, Fuzzy modeling and control schemes for nonlinear systems, Self-organizing fuzzy logic control, Fuzzy logic control for nonlinear time delay system.

UNIT –IV:
Genetic Algorithm:
Basic concept of Genetic algorithm and detail algorithmic steps, Adjustment of free parameters, Solution of typical control problems using genetic algorithm, Concept on some other search techniques like Tabu search and Ant-colony search techniques for solving optimization problems.

UNIT –V: Applications:
GA application to power system optimisation problem, Case studies: Identification and control of linear and nonlinear dynamic systems using MATLAB-Neural Network toolbox, Stability analysis of Neural-Network interconnection systems, Implementation of fuzzy logic controller using MATLAB fuzzy-logic toolbox, Stability analysis of fuzzy control systems.

TEXT BOOKS:
1. Introduction to Artificial Neural Systems - Jacek.M.Zurada, Jaico Publishing House, 1999.
2. Neural Networks and Fuzzy Systems - Kosko, B., Prentice-Hall of India Pvt. Ltd., 1994.

REFERENCE BOOKS:
1. Fuzzy Sets, Uncertainty and Information - Klir G.J. & Folger T.A., Prentice-Hall of India Pvt. Ltd., 1993.
2. Fuzzy Set Theory and Its Applications - Zimmerman H.J. Kluwer Academic Publishers, 1994.
3. Introduction to Fuzzy Control - Driankov, Hellendroon, Narosa Publishers.
4. Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi.
5. Elements of Artificial Neural Networks - Kishan Mehrotra, Chelkuri K. Mohan, Sanjay Ranka, Penram International.
6. Artificial Neural Network –Simon Haykin, 2nd Ed., Pearson Education.
7. Introduction Neural Networks Using MATLAB 6.0 - S.N. Shivanandam, S. Sumati, S. N. Deepa,1/e, TMH, New Delhi.

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
I Semester

ADVANCED OPERATING SYSTEMS
(ELECTIVE -II)

	L	T	P	Credits
B1540	3	1	0	3

UNIT –I:
Introduction to Operating Systems:
Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluation of operating System

UNIT –II:
Introduction to UNIX and LINUX:
Basic commands & command arguments, Standard input, output, Input / output redirection, filters and editors, Shells and operations

UNIT –III: System Calls:
System calls and related file structures, Input / Output, Process creation & termination.
Inter Process Communication
Introduction, file and record locking, Client – Server example, pipes, FIFOs, Streams & Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

UNIT –IV:
Introduction to Distributed Systems:
Goals of distributed system, Hardware and software concepts, Design issues.
Communication in Distributed Systems:
Layered protocols, ATM networks, Client - Server model, Remote procedure call and Group communication.

UNIT –V:
Synchronization in Distributed Systems:
Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions
Deadlocks:
Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.

TEXT BOOKS:
1. The design of the UNIX Operating Systems – Maurice J. Bach, 1986, PHI.
2. Distributed Operating System - Andrew. S. Tanenbaum, 1994, PHI.
3. The Complete reference LINUX – Richard Peterson, 4th Ed., McGraw – Hill.

REFERENCE BOOKS:
1. Operating Systems: Internal and Design Principles - Stallings, 6th Ed., PE.
2. Modern Operating Systems, Andrew S Tanenbaum, 3rd Ed., PE.
3. Operating System Principles- Abraham Silberchatz, Peter B. Galvin, Greg Gagne, 7th Ed., John Wiley
4. UNIX User Guide – Ritchie & Yates.
5. UNIX Network Programming - W.Richard Stevens, 1998, PHI.

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
I Semester

EMBEDDED C LABORATORY

	L	T	P	Credits
B1208	0	0	3	2

Note:

Minimum of 10 experiments have to be conducted.

The following programs have to be tested on 89C51 Development board/equivalent using Embedded C Language on Keil IDE or Equivalent.

1. Program to toggle all the bits of Port P1 continuously with 250 mS delay.
2. Program to toggle only the bit P1.5 continuously with some delay. Use Timer 0, mode 1 to create delay.
3. Program to interface a switch and a buzzer to two different pins of a Port such that the buzzer should sound as long as the switch is pressed.
4. Program to interface LCD data pins to port P1 and display a message on it.
5. Program to interface keypad. Whenever a key is pressed, it should be displayed on LCD.
6. Program to interface seven segment display unit.
7. Program to transmit a message from Microcontroller to PC serially using RS232.
8. Program to receive a message from PC serially using RS232.
9. Program to get analog input from Temperature sensor and display the temperature value on PC Monitor.
10. Program to interface Stepper Motor to rotate the motor in clockwise and anticlockwise directions
11. Program to Sort RTOS on to 89C51 development board.
12. Program to interface Elevator.

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
I Semester

HARDWARE - SOFTWARE CO-DESIGN

B1210	L	T	P	Credits
	3	1	0	3

UNIT –I:

Co- Design Issues:
Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.
Co- Synthesis Algorithms:
Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT –II:

Prototyping and Emulation:
Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures:
Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III:

Compilation Techniques and Tools for Embedded Processor Architectures:
Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV:

Design Specification and Verification:
Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V:

Languages for System – Level Specification and Design-I:
System – level specification, design representation for system level synthesis, system level specification languages,
Languages for System – Level Specification and Design-II:
Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

TEXT BOOKS:

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers

REFERENCE BOOKS:

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
II Semester

DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES

B1211	**L**	**T**	**P**	**Credits**
	3	1	0	3

UNIT –I:

Introduction to Digital Signal Processing:

Introduction, a Digital signal-processing system, the sampling process, discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation.

Computational Accuracy in DSP Implementations:

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT –II:

Architectures for Programmable DSP Devices:

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT -III:

Programmable Digital Signal Processors:

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT –IV:

Analog Devices Family of DSP Devices:

Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor.

Introduction to Black fin Processor - The Black fin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

UNIT –V:

Interfacing Memory and I/O Peripherals to Programmable DSP Devices:

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS:

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. A Practical Approach To Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, New Age International, 2006/2009
3. Embedded Signal Processing with the Micro Signal Architecture: Woon-Seng Gan, Sen M. Kuo, Wiley-IEEE Press, 2007

REFERENCE BOOKS:

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkataramani and M. Bhaskar, 2002, TMH.
2. Digital Signal Processing – Jonatham Stein, 2005, John Wiley.
3. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. 2000, S. Chand & Co.
4. Digital Signal Processing Applications Using the ADSP-2100 Family by The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI
5. The Scientist and Engineer's Guide to Digital Signal Processing by Steven W. Smith, Ph.D., California Technical Publishing, ISBN 0-9660176-3-3, 1997
6. Embedded Media Processing by David J. Katz and Rick Gentile of Analog Devices, Newnes , ISBN 0750679123, 2005

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
II Semester

EMBEDDED NETWORKING

B1212	**L**	**T**	**P**	**Credits**
	3	1	0	3

UNIT –I:

Embedded Communication Protocols:
Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire.

UNIT –II:

USB and CAN Bus:
USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.

UNIT –III: Ethernet Basics:
Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.

UNIT –IV: Embedded Ethernet:
Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT –V:

Wireless Embedded Networking:
Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.

TEXT BOOKS:

1. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, Tony Givargis, John & Wiley Publications, 2002
2. Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port - Jan Axelson, Penram Publications, 1996.

REFERENCE BOOKS:

1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series - Dogan Ibrahim, Elsevier 2008.
2. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003.
3. Networking Wireless Sensors - Bhaskar Krishnamachari , Cambridge press 2005.

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
II Semester

CPLD AND FPGA ARCHITECTURES AND APPLICATIONS

B1213	**L**	**T**	**P**	**Credits**
	3	1	0	3

UNIT-I:

Introduction to Programmable Logic Devices:
Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II:

Field Programmable Gate Arrays:
Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT -III:

SRAM Programmable FPGAs:
Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT -IV:

Anti-Fuse Programmed FPGAs:
Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT -V:

Design Applications:
General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

REFERENCE BOOKS:

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
II Semester

SENSORS AND ACTUATORS
(ELECTIVE –III)

	L	T	P	Credits
B1214	3	1	0	3

UNIT -I:
Sensors / Transducers: Principles – Classification – Parameters – Characteristics - Environmental Parameters (EP) – Characterization
Mechanical and Electromechanical Sensors: Introduction – Resistive Potentiometer – Strain Gauge – Resistance Strain Gauge – Semiconductor Strain Gauges -Inductive Sensors: Sensitivity and Linearity of the Sensor –Types- Capacitive Sensors:– Electrostatic Transducer– Force/Stress Sensors Using Quartz Resonators – Ultrasonic Sensors

UNIT –II:
Thermal Sensors: Introduction – Gas thermometric Sensors – Thermal Expansion Type Thermometric Sensors – Acoustic Temperature Sensor – Dielectric Constant and Refractive Index thermosensors – Helium Low Temperature Thermometer – Nuclear Thermometer – Magnetic Thermometer – Resistance Change Type Thermometric Sensors – Thermoemf Sensors– Junction Semiconductor Types– Thermal Radiation Sensors –Quartz Crystal Thermoelectric Sensors – NQR Thermometry – Spectroscopic Thermometry – Noise Thermometry – Heat Flux Sensors
Magnetic sensors: Introduction – Sensors and the Principles Behind – Magneto-resistive Sensors – Anisotropic Magnetoresistive Sensing – Semiconductor Magnetoresistors– Hall Effect and Sensors – Inductance and Eddy Current Sensors– Angular/Rotary Movement Transducers – Synchros – Synchro-resolvers - Eddy Current Sensors – Electromagnetic Flowmeter – Switching Magnetic Sensors SQUID Sensors

UNIT -III:
Radiation Sensors: Introduction – Basic Characteristics – Types of Photosensistors/Photo detectors– X-ray and Nuclear Radiation Sensors– Fiber Optic Sensors
Electro analytical Sensors: Introduction – The Electrochemical Cell – The Cell Potential - Standard Hydrogen Electrode (SHE) – Liquid Junction and Other Potentials – Polarization – Concentration Polarization-– Reference Electrodes - Sensor Electrodes – Electro ceramics in Gas Media .

UNIT -IV:
Smart Sensors: Introduction – Primary Sensors – Excitation – Amplification – Filters – Converters – Compensation– Information Coding/Processing - Data Communication – Standards for Smart Sensor Interface – The Automation
Sensors –Applications: Introduction – On-board Automobile Sensors (Automotive Sensors)– Home Appliance Sensors – Aerospace Sensors — Sensors for Manufacturing –Sensors for environmental Monitoring

UNIT -V:
Actuators: Pneumatic and Hydraulic Actuation Systems- Actuation systems – Pneumatic and hydraulic systems - Directional Control valves – Presure control valves – Cylinders - Servo and proportional control valves – Process control valves – Rotary actuators
Mechanical Actuation Systems- Types of motion – Kinematic chains – Cams – Gears – Ratchet and pawl – Belt and chain drives – Bearings – Mechanical aspects of motor selection
Electrical Actuation Systems-Electrical systems -Mechanical switches – Solid-state switches Solenoids – D.C. Motors – A.C. motors – Stepper motors

TEXT BOOKS:
1. D. Patranabis – “Sensors and Transducers” –PHI Learning Private Limited.
2. W. Bolton – “Mechatronics” –Pearson Education Limited.

REFERENCE BOOKS:
1. Sensors and Actuators – D. Patranabis – 2nd Ed., PHI, 2013.

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
II Semester
WIRELESS COMMUNICATIONS AND NETWORKS
(ELECTIVE –III)

	L	T	P	Credits
B1215	3	1	0	3

UNIT -I:

The Cellular Concept-System Design Fundamentals: Introduction, Frequency Reuse, Channel Assignment Strategies, Handoff Strategies- Prioritizing Handoffs, Practical Handoff Considerations, Interference and system capacity – Co channel Interference and system capacity, Channel planning for Wireless Systems, Adjacent Channel interference , Power Control for Reducing interference, Trunking and Grade of Service, Improving Coverage & Capacity in Cellular Systems- Cell Splitting, Sectoring .

UNIT –II:

Mobile Radio Propagation: Large-Scale Path Loss: Introduction to Radio Wave Propagation, Free Space Propagation Model, Relating Power to Electric Field, The Three Basic Propagation Mechanisms, Reflection-Reflection from Dielectrics, Brewster Angle, Reflection from prefect conductors, Ground Reflection (Two-Ray) Model, Diffraction-Fresnel Zone Geometry, Knife-edge Diffraction Model, Multiple knife-edge Diffraction, Scattering, Outdoor Propagation Models- Longley-Ryce Model, Okumura Model, Hata Model, PCS Extension to Hata Model, Walfisch and Bertoni Model, Wideband PCS Microcell Model, Indoor Propagation Models-Partition losses (Same Floor), Partition losses between Floors, Log-distance path loss model, Ericsson Multiple Breakpoint Model, Attenuation Factor Model, Signal penetration into buildings, Ray Tracing and Site Specific Modeling.

UNIT –III:

Mobile Radio Propagation: Small –Scale Fading and Multipath: Small Scale Multipath propagation-Factors influencing small scale fading, Doppler shift, Impulse Response Model of a multipath channel- Relationship between Bandwidth and Received power, Small-Scale Multipath Measurements-Direct RF Pulse System, Spread Spectrum Sliding Correlator Channel Sounding, Frequency Domain Channels Sounding, Parameters of Mobile Multipath Channels-Time Dispersion Parameters, Coherence Bandwidth, Doppler Spread and Coherence Time, Types of Small-Scale Fading-Fading effects Due to Multipath Time Delay Spread, Flat fading, Frequency selective fading, Fading effects Due to Doppler Spread-Fast fading, slow fading, Statistical Models for multipath Fading Channels-Clarke's model for flat fading, spectral shape due to Doppler spread in Clarke's model, Simulation of Clarke and Gans Fading Model, Level crossing and fading statistics, Two-ray Rayleigh Fading Model.

UNIT -IV:

Equalization and Diversity: Introduction, Fundamentals of Equalization, Training A Generic Adaptive Equalizer, Equalizers in a communication Receiver, Linear Equalizers, Non linear Equalization-Decision Feedback Equalization (DFE), Maximum Likelihood Sequence Estimation (MLSE) Equalizer, Algorithms for adaptive equalization-Zero Forcing Algorithm, Least Mean Square Algorithm, Recursive least squares algorithm. Diversity Techniques-Derivation of selection Diversity improvement, Derivation of Maximal Ratio Combining improvement, Practical Space Diversity Consideration-Selection Diversity, Feedback or Scanning Diversity, Maximal Ratio Combining, Equal Gain Combining, Polarization Diversity, Frequency Diversity, Time Diversity, RAKE Receiver.

UNIT -V:

Wireless Networks: Introduction to wireless Networks, Advantages and disadvantages of Wireless Local Area Networks, WLAN Topologies, WLAN Standard IEEE 802.11,IEEE 802.11 Medium Access Control, Comparision of IEEE 802.11 a,b,g and n standards, IEEE 802.16 and its enhancements, Wireless PANs, Hiper Lan, WLL.

TEXT BOOKS:

1. Wireless Communications, Principles, Practice – Theodore, S. Rappaport, 2nd Ed., 2002, PHI.
2. Wireless Communications-Andrea Goldsmith, 2005 Cambridge University Press.
3. Mobile Cellular Communication – Gottapu Sasibhushana Rao, Pearson Education, 2012.

REFERENCE BOOKS:

1. Principles of Wireless Networks – Kaveh Pah Laven and P. Krishna Murthy, 2002, PE
2. Wireless Digital Communications – Kamilo Feher, 1999, PHI.
3. Wireless Communication and Networking – William Stallings, 2003, PHI.
4. Wireless Communication – Upen Dalal, Oxford Univ. Press
5. Wireless Communications and Networking – Vijay K. Gary, Elsevier.

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
II Semester

ADHOC AND SENSOR NETWORKS
(ELECTIVE – III)

B1523	**L**	**T**	**P**	**Credits**
	3	1	0	3

UNIT – I Introduction to Ad Hoc Wireless Networks: Characteristics of MANETS, Applications of MANETS, Challenges Routing In MANETS: Topology based versus position based approaches, Topology based routing protocols, and position based routing, other routing protocols

UNIT – II Data Transmission In MANETS: The broadcast storm, Multicasting, Geocasting. TCP Over Ad Hoc Networks: TCP protocol overview, TCP and MANETS, Solutions for TCP over Ad Hoc

UNIT – III Basics Of Wireless Sensors And Applications: The Mica Mote, Sensing and Communication Range, Design Issues, Energy Consumption, Clustering of Sensors, Applications. Data Retrieval In Sensor Networks: Classification of WSNs, MAC Layer, Routing Layer, High-Level Application Layer Support, Adapting to the Inherent Dynamic Nature of WSNs.

UNIT – IV Security: Security in Ad Hoc Wireless Networks, Key Management, Secure Routing, Cooperation in MANETs, Intrusion Detection Systems Sensor Network Platforms and Tools: Sensor network Hardware, Sensor Network Programming Challenges, and Node-Level Software Platforms.

UNIT – V Operating System-Tiny OS: Imperative Language: nesC, Data flow style language: Tiny GALS, Node- Level Simulators, NS-2 and its sensors network extension, TOSSIM.

TEXT BOOKS:

1. Ad Hoc and Sensor Networks: Theory and Applications, Carlos de Morais Cordeiro and Dharma Prakash Agrawal, World Scientific Publications / Cambridge University Press, 2006.
2. Wireless Sensor Networks: An Information Processing Approach, Feng Zhao, Leonidas Guibas, Elsevier Science Imprint, Morgan Kauffman Publishers, 2005.

REFERENCE BOOKS:

1. Ad Hoc Wireless Networks: Architectures and Protocols, C. Siva Ram Murthy and B. S. Manoj, Pearson Education, 2004.
2. Guide to Wireless Ad Hoc Networks, Sudip Misra, Isaac Woungang, and Subhas Chandra Misra, Springer International Edition, 2011.
3. Guide to Wireless Sensor Networks, Sudip Misra, Isaac Woungang, and Subhas Chandra Misra, Springer International Edition, 2012.
4. Wireless Mesh Networking, Thomas Krag and Sebastin Buettrich, O'Reilly Publishers,2007.
5. Wireless Sensor Networks – Principles and Practice, Fei Hu, Xiaojun Cao, An Auerbach book, CRC Press, Taylor & Francis Group, 2010.
6. Wireless Ad hoc Mobile Wireless Networks-Principles, Protocols and Applications, Subir Kumar Sarkar, et al., Auerbach Publications, Taylor & Francis Group, 2008.
7. Wireless Ad hoc Networking, Shih-Lin Wu, Yu-Chee Tseng, Auerbach Publications, Taylor & Francis Group, 2007
8. Wireless Ad hoc and Sensor Networks–Protocols, Performance and Control, Jagannathan Sarangapani, CRC Press, Taylor & Francis Group, 2007, rp2010.
9. Security in Ad hoc and Sensor Networks, Raheem Beyah, et al., World Scientific Publications /Cambridge University Press, 2010.

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
II Semester

MULTI MEDIA AND SIGNAL CODING
(ELECTIVE -IV)

B1216	**L**	**T**	**P**	**Credits**
	3	1	0	3

UNIT -I:

Introduction to Multimedia: Multimedia, World Wide Web, Overview of Multimedia Tools, Multimedia Authoring, Graphics/ Image Data Types, and File Formats.

Color in Image and Video: Color Science – Image Formation, Camera Systems, Gamma Correction, Color Matching Functions, CIE Chromaticity Diagram, Color Monitor Specifications, Out-of-Gamut Colors, White Point Correction, XYZ to RGB Transform, Transform with Gamma Correction, L*A*B* Color Model. Color Models in Images – RGB Color Model for CRT Displays, Subtractive Color: CMY Color Model, Transformation from RGB to CMY, Under Color Removal: CMYK System, Printer Gamuts, Color Models in Video – Video Color Transforms, YUV Color Model, YIQ Color Model, Ycbcr Color Model.

UNIT -II:

Video Concepts: Types of Video Signals, Analog Video, Digital Video.

Audio Concepts: Digitization of Sound, Quantization and Transmission of Audio.

UNIT -III:

Compression Algorithms:

Lossless Compression Algorithms: Run Length Coding, Variable Length Coding, Arithmetic Coding, Lossless JPEG, Image Compression.

Lossy Image Compression Algorithms: Transform Coding: KLT And DCT Coding, Wavelet Based Coding.

Image Compression Standards: JPEG and JPEG2000.

UNIT -IV:

Video Compression Techniques: Introduction to Video Compression, Video Compression Based on Motion Compensation, Search for Motion Vectors, H.261- Intra-Frame and Inter-Frame Coding, Quantization, Encoder and Decoder, Overview of MPEG1 and MPEG2.

UNIT -V:

Audio Compression Techniques: ADPCM in Speech Coding, G.726 ADPCM, Vocoders – Phase Insensitivity, Channel Vocoder, Formant Vocoder, Linear Predictive Coding, CELP, Hybrid Excitation Vocoders, MPEG Audio – MPEG Layers, MPEG Audio Strategy, MPEG Audio Compression Algorithms, MPEG-2 AAC, MPEG-4 Audio.

TEXT BOOKS:

1. Fundamentals of Multimedia – Ze- Nian Li, Mark S. Drew, PHI, 2010.
2. Multimedia Signals & Systems – Mrinal Kr. Mandal Springer International Edition 1st Edition, 2009

REFERENCE BOOKS:

1. Multimedia Communication Systems – Techniques, Stds& Netwroks K.R. Rao, Zorans. Bojkoric, Dragorad A.Milovanovic, 1st Edition, 2002.
2. Fundamentals of Multimedia Ze- Nian Li, Mark S.Drew, Pearson Education (LPE), 1st Edition, 2009.
3. Multimedia Systems John F. Koegel Bufond Pearson Education (LPE), 1st Edition, 2003.
4. Digital Video Processing – A. Murat Tekalp, PHI, 1996.
5. Video Processing and Communications – Yaowang, Jorn Ostermann, Ya-QinZhang, Pearson, 2002

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
II Semester

SYSTEM ON CHIP ARCHITECTURE
(ELECTIVE -IV)

B1217	**L**	**T**	**P**	**Credits**
	3	1	0	3

UNIT –I:

Introduction to the System Approach:

System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT –II: Processors:

Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT –III:

Memory Design for SOC:

Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT -IV:

Interconnect Customization and Configuration:

Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT –V:

Application Studies / Case Studies:

SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
II Semester

WIRELESS LANS AND PANS
(ELECTIVE-IV)

B1218	**L**	**T**	**P**	**Credits**
	3	1	0	3

UNIT –I:
Wireless System & Random Access Protocols:
Introduction, First and Second Generation Cellular Systems, Cellular Communications from 1G to 3G, Wireless 4G systems, The Wireless Spectrum; Random Access Methods: Pure ALOHA, Slotted ALOHA, Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA).

UNIT –II: Wireless LANs:
Introduction, importance of Wireless LANs, WLAN Topologies, Transmission Techniques: Wired Networks, Wireless Networks, comparison of wired and Wireless LANs; WLAN Technologies: Infrared technology, UHF narrowband technology, Spread Spectrum technology

UNIT –III:
The IEEE 802.11 Standard for Wireless LANs:
Network Architecture, Physical layer, The Medium Access Control Layer; MAC Layer issues: Hidden Terminal Problem, Reliability, Collision avoidance, Congestion avoidance, Congestion control, Security, The IEEE 802.11e MAC protocol

UNIT –IV: Wireless PANs:
Introduction, importance of Wireless PANs, The Bluetooth technology: history and applications, technical overview, the Bluetooth specifications, piconet synchronization and Bluetooth clocks, Master-Slave Switch; Bluetooth security; Enhancements to Bluetooth: Bluetooth interference issues, Intra and Inter Piconet scheduling, Bridge selection, Traffic Engineering, QoS and Dynamics Slot Assigment, Scatternet formation.

UNIT –V:
The IEEE 802.15 working Group for WPANs:
The IEEE 802.15.3, The IEEE 802.15.4, ZigBee Technology, ZigBee components and network topologies, The IEEE 802.15.4 LR-WPAN Device architecture: Physical Layer, Data Link Layer, The Network Layer, Applications; IEEE 802.15.3a Ultra wideband.

TEXT BOOKS:
1. Ad Hoc and Sensor Networks - Carlos de Morais Cordeiro and Dharma Prakash Agrawal, World Scientific, 2011.
2. Wireless Communications and Networking - Vijay K.Garg, Morgan Kaufmann Publishers, 2009.

REFERENCE BOOKS:
1. Wireless Networks - Kaveh Pahlaram, Prashant Krishnamurthy, PHI, 2002.
2. Wireless Communication- Marks Ciampor, Jeorge Olenewa, Cengage Learning, 2007.

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
II Semester

EMBEDDED SYSTEMS LABORATORY

B1219	**L**	**T**	**P**	**Credits**
	0	0	3	2

Note:

A. The following programs are to be implemented on ARM based Processors/Equivalent.
B. Minimum of 10 programs from Part –I and 6 programs from Part -II are to be conducted.

PART- I:

The following Programs are to be implemented on ARM Processor

1. Simple Assembly Program for
    a. Addition | Subtraction | Multiplication | Division
    b. Operating Modes, System Calls and Interrupts
    c. Loops, Branches
2. Write an Assembly programs to configure and control General Purpose Input/Output (GPIO) port pins.
3. Write an Assembly programs to read digital values from external peripherals and execute them with the Target board.
4. Program for reading and writing of a file
5. Program to demonstrate Time delay program using built in Timer / Counter feature on IDE environment
6. Program to demonstrates a simple interrupt handler and setting up a timer
7. Program demonstrates setting up interrupt handlers. Press button to generate an interrupt and trace the program flow with debug terminal.
8. Program to Interface 8 Bit LED and Switch Interface
9. Program to implement Buzzer Interface on IDE environment
10. Program to Displaying a message in a 2 line x 16 Characters LCD display and verify the result in debug terminal.
11. Program to demonstrate I2C Interface on IDE environment
12. Program to demonstrate I2C Interface – Serial EEPROM
13. Demonstration of Serial communication. Transmission from Kit and reception from PC using Serial Port on IDE environment use debug terminal to trace the program.
14. Generation of PWM Signal
15. Program to demonstrate SD-MMC Card Interface.

PART- II:

Write the following programs to understand the use of RTOS with ARM Processor on IDE Environment using ARM Tool chain and Library:

1. Create an application that creates two tasks that wait on a timer whilst the main task loops.
2. Write an application that creates a task which is scheduled when a button is pressed, which illustrates the use of an event set between an ISR and a task
3. Write an application that Demonstrates the interruptible ISRs(Requires timer to have higher priority than external interrupt button)
4. a).Write an application to Test message queues and memory blocks. b).Write an application to Test byte queues
5. Write an application that creates two tasks of the same priority and sets the time slice period to illustrate time slicing.

Interfacing Programs:

6. Write an application that creates a two task to Blinking two different LEDs at different timings
7. Write an application that creates a two task displaying two different messages in LCD display in two lines.
8. Sending messages to mailbox by one task and reading the message from mailbox by another task.

9. Sending message to PC through serial port by three different tasks on priority Basis.
10. Basic Audio Processing on IDE environment.