CMR COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution)

ACADEMIC REGULATION R-18

FOR CBCS BASED M. TECH. (REGULAR) DEGREE PROGRAMMES

(Applicable for the students of M. Tech. programme admitted into I year from Academic Year 2018-19 and onwards)

1.0 Eligibility for Admissions

Admission to the above program shall be made subject to eligibility, qualification and specialization as prescribed by Government of Telangana State from time to time.

Admission shall be made on the basis of merit/rank obtained by the candidates at the qualifying Entrance Test conducted by the Government of Telangana or on the basis of any other order of merit as approved by the University, subject to reservations as laid down by the Government from time to time.

2.0 Award of M. Tech. degree

2.1 A student shall be declared eligible for the award of the M. Tech. Degree, if he pursues a course of study in not less than two and not more than four academic years. However, he is permitted to write the examinations for two more years after four academic years of course work, failing which he shall forfeit his seat in M.Tech. programme.

2.2 The M. Tech. degree of Jawaharlal Nehru Technological University Hyderabad shall be conferred on candidates who are admitted to the program and who fulfil all the requirements for the award of the degree.

2.3 The student shall register for all 68 credits and secure all the 68 credits.

2.4 The medium of instruction and examination shall be English.

3.0 A. Courses of Study

The following specializations are offered at present for the M. Tech. course of study.

1. Embedded Systems
2. Power Electronics
3. Structural Engineering
4. Computer Science & Engineering

and any other course as approved by the College/ University/AICTE from time to time.

B. Departments offering M.Tech. programmes with specializations mentioned below:

Sl. No.	Department	M.Tech Course
1	ECE	Embedded Systems
2	EEE	Power Electronics
3	Civil	Structural Engineering
4	CSE	Computer Science & Engineering

4.0 Course Registration

4.1 A 'Faculty Advisor or Counselor' shall be assigned to each student, who will advise him about the PG Programme, its Course Structure and Curriculum, Choice/Option for Courses, based on his competence, progress, pre-requisites and interest.

4.2 Academic Section of the College invites 'Registration Forms' from students within 15 days from the commencement of class work through 'ON-LINE SUBMISSIONS', ensuring 'DATE and TIME Stamping'. The ON-LINE Registration Requests for any 'CURRENT SEMESTER' shall be completed BEFORE the commencement of SEEs (Semester End Examinations) of the 'PRECEDING SEMESTER'.

4.3 A Student can apply for ON-LINE Registration, ONLY AFTER

obtaining the 'WRITTEN APPROVAL' from his Faculty Advisor, which should be submitted to the College Academic Section through the Head of Department (a copy of the same being retained with Head of Department, Faculty Advisor and the Student).

4.4 If the Student submits ambiguous choices or multiple options or erroneous entries - during ON-LINE Registration for the Course(s) under a given/ specified Course Group/ Category as listed in the Course Structure, thereby causing discrepancy, the decision of Head of the Department shall be final.

4.5 Course Options exercised through ON-LINE Registration are final and cannot be changed /inter-changed; further, alternate choices will also not be considered. However, if the Course that has already been listed for Registration (by the Head of Department) in a Semester could not be offered due to any unforeseen or unexpected reasons, then the Student shall be allowed to have alternate choice - either for a new Course (subject to offering of such a Course), or for another existing Course (subject to availability of seats), which may be considered. Such alternate arrangements will be made by the Head of Department, with due notification and time-framed schedule, within the first week from the commencement of Class-work for that Semester.

5.0. Attendance

The programs are offered on a unit basis with each course t being considered a unit.

5.1 The minimum instruction period for each semester shall be 90 clear instruction days.

5.2 A student shall be eligible to write semester end examinations of a course if he acquires a minimum of 75% of attendance in that course.

5.3 Condonation of shortage of attendance in each Course up to 10% (65% and above and below 75%) in each semester may be granted by the Institute Academic Committee on valid medical reasons.

5.4 Shortage of attendance below 65% shall not be condoned.

5.5 Students whose shortage of attendance is not condoned in any semester for a course(s) are not eligible to write their end semester examination of those courses and their registration for these courses shall stand cancelled. They have to register for these courses later when offered.

5.6 A fee as prescribed by the Institute Academic Committee shall be payable towards condonation of shortage of attendance.

5.7 A candidate shall put in a minimum required attendance, in at least 3 theory Courses in I semester for promoting to II semester.

5.8 In order to qualify for the award of the M. Tech. Degree, the candidate shall complete all the academic requirements of the courses, as per the course structure.

5.9 A student shall not be promoted to the next semester unless he satisfies the attendance requirement of the present semester as applicable. They may re-register for the semester when offered next. If a candidate fulfils the attendance requirement in the present semester, he shall not be eligible for re- registration into the same class.

6.0 Evaluation

6.1 The performance of the candidate in each semester shall be evaluated Course-wise, with a maximum of 100 marks for theory and 100 marks for practicals, on the basis of Internal Evaluation and Semester End Examination.

6.2 For the theory courses 70 marks shall be awarded based on the performance in the Semester End Examination and 30 marks shall be awarded based on the Internal Evaluation. For internal evaluation there shall be the two internal examinations conducted- one in the middle of the semester and the other immediately after the completion of instruction period. Each internal examination shall be conducted for a total duration of 120 minutes. The final marks secured by the student in 'internal evaluation' for the semester are arrived at by giving a weightage of 70% to the best secured 'internal examination' and 30% weightage to the least secured 'internal examination'. A student who is absent for any internal examination for any reason what so ever shall be deemed to have secured 'zero' marks in the test/ examination and no make-up test/ examination shall be conducted.

6.3 Question paper pattern for evaluation

I. Internal Examination

Part A (10 Marks)

5 questions of 2 marks each (All questions are compulsory).

Part B (20 Marks)

4 questions to be answered out of 6 questions, each question carries 5 marks.

II. External Examination

Part A (20 Marks)

5 questions (1 question from each unit) of 4 marks each (Compulsory questions)

Part B (50 Marks)

5 questions (1 question from each unit with internal choice) each question carries 10 marks.

6.4 For practical courses, 70 marks shall be awarded based on the performance in the End Semester Examinations. 30 marks shall be awarded for day to day performance in the practicals as internal marks. Laboratory end examination for M. Tech. courses for 70 marks must be conducted with two Examiners, one of them being the Laboratory Course Teacher and the second examiner shall be

External Examiner. External Examiner shall be appointed by the Controller of Examinations from other institutions or industry.

6.5 There shall be Mini project with seminar presentation during II semester. For Mini project with seminar, a student under the supervision of a faculty member, shall do a mini project and submit it to the department in a report form and shall make an oral presentation before the Departmental Academic Committee consisting of Head of the Department, Supervisor and two other senior faculty members of the department. For each Seminar there will only be internal evaluation for 50 marks. A candidate has to secure for each seminar a minimum of 50% of maximum marks to be declared successful. If he fails to secure minimum marks, he has to re-appear during the supplementary examinations.

6.6 Each student shall start the Project Work during the IV Semester as per the instructions of the Project Guide/ Project Supervisor assigned by the Head of the Department.

a) The Project Work shall be divided and carried out in 2 phases : Phase – I (Project-I) during III Semester, and Phase – II (Project-II) during IV Semester, and the student has to prepare two independent Project Work Reports – one each during each phase. First Report shall include the Project Work carried out under Phase – I, and the Second Report (Final Report) shall include the Project Work carried out under Phase – I and Phase – II put together. Phase – I and Phase – II of the Project Work shall be evaluated for 100 marks each.

b) Out of the total 100 marks allotted for each Phase of the Project Work, 40 marks shall be for the Continuous Internal Evaluation(CIE), and 60 marks shall be for the End Semester Viva-voce Examination (SEE). The marks earned under CIE for both Phases of the Project shall be awarded by the Project Guide/Supervisor (based on the continuous evaluation of

student's performance during the two Project Work Phases/periods); and the marks earned under SEE shall be awarded by the Project Viva-voce Committee/ Board (based on the work carried out, report prepared and the presentation made by the student at the time of Viva-voce Examination).

c) For the Project Phase - I, the Viva-voce shall be conducted at the end of the III Semester, before the commencement of the semester End Examinations, at the Department Level by a Committee comprising of the HoD or One Professor and Supervisor (no external examiner), and the Project Phase – II Viva-voce (or Final Project Viva-voce) shall be conducted by a Committee comprising of an External Examiner, the Head of the Department and the Project Supervisor at the end of the IV Semester, before the commencement of the semester End Examinations. The External Examiner shall be nominated by the CoE from the panel of 3 names of external faculty members (Professors or Associate Professors outside the College) submitted by the HoD.

d) If a student does not appear for any of the two Viva-Voce examinations at the scheduled times as specified above, he may be permitted to reappear for Project Phase-I and/or Project Phase-II Viva-voce examinations, as and when they are scheduled in that semester; if he fails in such 'one reappearance' evaluation

also, he has to reappear for the same in the next subsequent semester(s), as and when they are scheduled, as supplementary candidate. For the registration of Project Phase-II the student must have passed Project Phase-I.

A candidate shall be deemed to have secured the minimum academic requirement in a course if he secures a minimum of 40% marks in the End semester Examination and a minimum aggregate

of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

6.7 In case the candidate does not secure the minimum academic requirement in any course (as specified in 5.9) he has to reappear for the Semester End Examination in that course.

6.8 A candidate shall be given one chance to re-register for the Courses if the internal marks secured by a candidate are less than 50% and has failed in the end examination. In such a case, the candidate must re-register for the Course(s) and secure the required minimum attendance. The candidate's attendance in the re-registered Course(s) shall be calculated separately to decide upon his eligibility for writing the end examination in those Courses(s). In the event of the student taking another chance, his internal marks and end examination marks obtained in the previous attempt stand cancelled.

6.9 In case the candidate secures less than the required attendance in any course, he shall not be permitted to write the End Examination in that course. He shall re-register the course when next offered.

7.0 Examinations and Assessment – The Grading System

7.1 Marks will be awarded to indicate the performance of each student in each Theory Course or Lab/Practical, or Project, etc., based on the % marks obtained in CIE + SEE (Continuous Internal Evaluation + Semester End Examination, both taken together) as specified in item 6 above, and a corresponding Letter Grade shall be given.

7.2 As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades

(UGC Guidelines) and corresponding range of percentage of marks shall be followed:

% of Marks Secured (class intervals)	Letter Grade (UGC Guidelines)	Grade Points
80% and above (≥ 80%, ≤ 100%)	**O (Outstanding)**	**10**
Below 80% but not less than 70% (≥ 70%, <80%)	**A^+ (Excellent)**	**9**
Below 70% but not less than 60% (≥ 60%, <70%)	**A (Very Good)**	**8**
Below 60% but not less than 55% (≥ 55%, <60%)	**B^+ (Good)**	**7**
Below 55% but not less than 50% (≥ 50%, < 55%)	**B (above Average)**	**6**
Below 50% (< 50%)	**F (FAIL)**	**0**
Absent	**AB**	**0**

7.3 A student obtaining 'F' Grade in any Course shall be considered ' failed ' and is required to reappear as 'Supplementary Candidate' in the Semester End Examination (SEE), as and when offered. In such cases, his Internal Marks (CIE Marks) in those Courses will remain the same as those he obtained earlier.

7.4 A student not appeared for examination the 'AB' Grade will be allocated in any Course shall be considered 'failed' and will be required to reappear as 'Supplementary Candidate' in the Semester End Examination (SEE), as and when offered.

7.5 A Letter Grade does not imply any specific Marks percentage and it will be the range of marks percentage.

7.6 In general, a student shall not be permitted to repeat any Course (s) only for the sake of 'Grade Improvement' or 'SGPA/CGPA Improvement'

7.7 A student earns Grade Point (GP) in each Course, on the basis of

the Letter Grade obtained by him in that Course. The corresponding 'Credit Points '(CP) are computed by multiplying, the Grade Point with Credits for that particular Courses.

Credit Points (CP) = Grade Point (GP) x Credit … For a Course.

7.8 The Student passes the Course only when he **gets GP ≥ 6 (B Grade or above)**

7.9 The Semester Grade Point Average (SGPA) is calculated by dividing the Sum of Credit Points (∑CP) secured from All Courses registered in a Semester, by the Total Number of Credits registered during that Semester. SGPA is rounded off to TWO Decimal Places, SGPA is thus computed as.

SGPA = { ∑Ni=1 Ci Gj } / { ∑Ni =1 Ci} ….For each Semester.

Where 'i' is the Course indicator index (takes into account all Courses in a Semester), 'N' is the no. of Courses 'REGISTERED' for the Semester (as specifically required and listed under the Course Structure of the parent Department), Ci is the no. of Credits allotted to the ith Course, and Gi represent the Grade Points (GP) corresponding to the Letter Grade awarded for that ith Course.

7.10 The Cumulative Grade Point Average (CGPA) is measure of the overall cumulative performance of a student over all Semesters considered for registration. The CGPA is the ratio of the Total Credit Points secured by a student in All registered Courses in All Semesters, and the Total Number of Credits registered in All the Semesters. CGPA is rounded off to TWO Decimal Places. CGPA is thus computed from the I Year Second Semester onwards, as the end of each Semester, as per the formula.

CGPA = {∑M j=1 C j G j } / {∑M j=1 C j} } …. For all S Semester registered

{ it., upto and inclusive of S Semester, S ≥2).

Where 'M' is the TOTAL no. of Subject (as specifically required and listed under the Course Structured of the parent Department) the Student has 'REGISTERED' from the 1st Semester onwards upto and inclusive of the Semester S (Obviously M > N), 'j ' is the Subject indicator index (takes into account all Courses from 1 to S Semesters),C j is the no. of Credits allotted to the jth Courses from Gj represent the Grade Points (GP) corresponding to the Letter Grade awarded for the jth Course. After registration and completion of II Semester however, the SGPA of that Semester itself may be taken as the CGPA, as there are no cumulative effects.

7.11. For Calculations listed in item 7.6 – 7.10, performance in failed Courses (securing F Grade) will also be take into account, and the credits of such Courses will also be included in the multiplications and summations.

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8.0 Evaluation of Project/Dissertation Work

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

8.1 A Project Review Committee (PRC) shall be constituted with Head of the Department as Chairperson, Project Supervisor and one senior faculty member of the Department offering the M.Tech programme as members.

8.2 Registration of Project Work: A Candidate is permitted to register for the project work after satisfying the attendance requirement of all the courses, both theory and practical of I year.

8.3 After satisfying 8.2, a candidate has to submit, in consultation with his project Supervisor, the title, objective and plan of action of his project work to the PRC for approval. Only after obtaining the approval of the PRC the student can initiate the Project work.

8.4 If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the PRC. However, the PRC shall examine whether or not the changes of topic/supervisor leads to a major changes of his initial plans of project proposal. If yes his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

8.5 A candidate shall submit his project status report in two stages at least with a gap of 3 months between them.

8.6 The work on the project shall be initiated at the beginning of the III semester and the duration of the project is two semesters. A candidate is permitted to submit Project Thesis only after successful completion of all theory and practical courses with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Head of the Department and make an oral presentation before the PRC.

8.7 After approval from the PRC, the soft copy of the thesis should be submitted to the College for ANTI-PLAGIARISM check and the plagiarism report should be included in the final thesis. If the result of above check is less than 24%, then only thesis will be accepted for submission.

8.8 Three copies of the Project Thesis certified by the supervisor shall be submitted to the College.

8.9 For Project Work, Review-I will be conducted in III Semester and carries a maximum internal marks of 40. The evaluation should be done by the PRC for 20 marks and Project Supervisor for 20 marks. The Supervisor and PRC will examine the Literature Survey in the same domain, Problem Definition, Objective, Scope of Work. A candidate has to secure a minimum of 50% of marks to be declared successful in Project Work Review I. If he fails to secure minimum required marks he has to reappear during the

supplementary examination.

8.10 Project Work Review II in IV Semester carries 40 internal marks. The evaluation should be done by the PRC for 20 marks and the Project Supervisor for 20 marks. The PRC will examine the overall progress of the Project Work and decide the eligibility of the Project for final submission. A candidate has to secure a minimum of 50% of marks to be declared successful in Project Work Review II. If he fails to fulfill minimum marks, he has to reappear for Review-II during the supplementary examination.

8.11 The thesis shall be adjudicated by the committee consisting of one senior faculty selected by the Head of the Department, the guide concerned, Head of the Department and external examiner.

8.12 If the report of the committee is not favourable, the candidate shall revise and resubmit the Thesis. If the report of the committee is unfavourable again, the thesis shall be summarily rejected.

8.13 For Project Work Evaluation (Viva Voice) will be conducted on acceptance of the Thesis in IV Semester. This is an external evaluation for 60 marks and will be evaluated by the committee. The External Examiner for the committee shall be appointed by the Controller of Examinations. The candidate has to secure minimum of 50% marks in Project Evaluation (Viva Voice) examination for its successful completion.

8.14 If he fails to secure minimum marks as specified in 8.13, he will reappear for the Viva Voice examination only after three months. In the reappeared examination also if the candidate fails to secure minimum prescribed marks the registration for the programme stands cancelled and he will not be eligible for the award of the degree.

8.15 The Head of the Department shall coordinate and make arrangements for the conduct of Project Viva Voice examination.

9.0 Award of Degree and Class

9.1 A Student who registers for all the specified Courses as listed in the Course Structure, satisfies all the Course Requirements, and passes the examinations prescribed in the entire PG Programme (PGP), and secured the required number of 88 Credits (with CGPA ≥ 6.0), shall be declared to have 'QUALIFIED' for the award of the M.Tech. Degree in the chosen Branch of Engineering and Technology, with the specialization for which he took admission.

9.2 Award of Class

After a student has satisfied the requirements prescribed for the completion of the programme, becomes eligible for the award of M.Tech. Degree, he shall be placed in one of the following three classes based on the CGPA.

Class Awarded	CGPA
First Class and Distinction	≥ 7.75
First Class	6.75 ≤ CGPA > 7.75
Second Class	6.00 ≤ CGPA < 6.75

9.3 A student with final CGPA (at the end of the PGP) < 6.00 will not be eligible for the Award of Degree.

10. Withholding of Results

If the student has not paid the dues, if any, to the institution or if any case of indiscipline is pending against him, the result of the student will be withheld and he will not be allowed into the next semester.

11. General

11.1 Wherever the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”, “hers”.

11.2 The academic regulation should be read as a whole for the purpose of any interpretation.

11.3 In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Academic Council is final.

11.4 The college may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the college.

MALPRACTICES RULES
DISCIPLINARY ACTION FOR
IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/ Improper conduct	**Punishment**
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
1. (b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other Courses the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the Courses of that Semester/year. The Hall Ticket of thecandidate is to be cancelled.
3.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance

		of the original candidate who has been impersonated, shall be cancelled in all the Courses of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the Remaining Courses of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all end semester examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4.	Smuggles the answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination	Expulsion from the examination hall and cancellation of performance in that subject and all the other Courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the Courses of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all end semester Examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks	Cancellation of the performance in that subject
6.	Refuses to obey the orders of the Chief Superintendent/ Assistant–Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the college	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other Courses the

	or organizes a walk out or instigates others to examination hall walkout, or threatens the officer- in-charge or any person on Duty in or outside the examination hall of any injury, to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer- in-charge, or any person on Duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the Courses of that semester/year. The candidates are also debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other Courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the Courses of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other Courses the candidate has already appeared including practical examinations and project work and shall not be permitted

		for the remaining examinations of the Courses of that semester/year. The candidate is also debarred and forfeits the seat.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	If the student belongs to the college, expulsion from the examination hall an cancellation of performance in that subject and all other Courses hall and all other Courses that candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the Courses of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other Courses the candidate has already appeared including practical examinations and project work and shall not be permitted for other remaining examinations of the Courses of that semester/year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other Courses the candidate has appeared including practical examinations and project work of that semester/year.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the College Academic Committee for further action to award suitable punishment.	

Malpractices identified by squad or special invigilators

Punishments to the candidates as per the above guidelines.

Malpractice identified at Spot center during valuation

The following procedure is to be followed in case of malpractice cases detected during valuation, scrutiny etc. at spot center.

1 Malpractice is detected at the spot valuation. The case is to be referred to the malpractice committee. Malpractice committee will meet and discuss/question the candidate and based on the evidences, the committee will recommend suitable action on the candidate.

2 A notice is to be served to the candidate(s) involved through the Principal to his address and to the candidate(s) permanent address regarding the malpractice and seek explanations.

3 The involvement of staff who are in charge of conducting examinations, invigilators valuing examination papers and preparing / keeping records of documents relating to the examinations in such acts (inclusive of providing incorrect or misleading information) that infringe upon the course of natural justice to one and all concerned at the examinations shall be viewed seriously and recommended for award of appropriate punishment after thorough enquiry.

4 Based on the explanation and recommendation of the committee, action may be initiated.

5 Malpractice committee:

i.	Controller of Examinations	Chairman
ii.	Assistant controller of Evaluation	Member
iii.	Chief Examiner of the subject/ subject expert	Member
iv.	Concerned Head of the Department	Member
v.	Concerned Invigilator	Member

DEPARTMENT OF
ELECTRONICS & COMMUNICATION ENGINEERING

COURSE STRUCTURE FOR M. TECH (EMBEDDED SYSTEMS)
EFFECTIVE FROM ACEDEMIC YEAR 2018-19

I SEMESTER

S.No	CODE	Group	COURSE TITLE	L	T	P	C
1	B30201	Core 1	Microcontrollers for Embedded System Design	3	0	0	3
2	B30202	Core 2	Embedded Programming	3	0	0	3
3	B30215	PE -I	VLSI Technology & Design	3	0	0	3
4	B30216		Image & Video Processing				
5	B30217		System Design with Embedded Linux				
6	B30218	PE - II	Embedded Networking	3	0	0	3
7	B30219		CPLD and FPGA Architecture & Applications				
8	B30220		Embedded Computing				
9	B30203	Lab 1	Embedded Programming Lab	0	0	4	2
10	B30204	Lab 2	Scripting Languages Lab	0	0	4	2
11	B30212		Research Methodology and IPR	2	0	0	2
12	C30001	AUD 1	English for Research Paper Writing	2	0	--	0
			Total	**16**	**0**	**8**	**18**

II SEMESTER

S.No	CODE	Group	COURSE TITLE	L	T	P	C
1	B30205	Core 3	System On Chip Architecture	3	0	0	3
2	B30206	Core 4	Embedded Real Time Operating System	3	0	0	3
3	B30221	PE- III	Digital System Design	3	0	0	3
4	B30222		Analog and Digital CMOS VLSI Design				
5	B30223		Communication Buses & Interfaces				

6	B30224	PE - IV	Wireless LANs and PANs	3	0	0	3
7	B30225		Advanced Computer Architecture				
8	B30226		Advanced Microcontroller and Its Applications				
9	B30207	Lab 1	Embedded System Design Lab	0	0	4	2
10	B30208	Lab 2	Programmable System on Chip Lab		0	4	2
11	B30209	PROJ	Mini Project with Seminar	0	0	4	2
12	C30002	AUD 2	Value Education	2	0	0	0
			TOTAL	**14**	**0**	**12**	**18**

III SEMESTER

S. No	CODE	Group	Title	L	T	P	C
1	B30227	PE - V	Design of Fault Tolerant Systems	3	0	0	3
2	B30228		CMOS Mixed Signal Design				
3	B30229		Hardware Software Co-Design				
4		OE	Open Elective	3	0	0	3
5	B30210	PROJ	Dissertation Phase - I	0	0	20	10
			TOTAL	**6**	**0**	**20**	**16**

IV SEMESTER

S. No	CODE	Group	Course Title	L	T	P	C
1	B30211	PROJ	Dissertation Phase - II	0	0	32	16
			TOTAL	**0**	**0**	**32**	**16**

Open Elective		Department offering
B30230	Application Specific Integrated Circuits Design	ECE
B30231	Embedded Systems	ECE
B30331	Renewable energy sources	EEE
B30332	Industrial safety	EEE
B30532	Big Data and Analytics	CSE
B30533	Python Programming	CSE
B30431	Green building	CIVIL
B30432	Construction Project Management	CIVIL

S. No	Category
Core	Core Course
PE	Professional Elective
AUD	Audit Course
OE	Open Elective
PROJ	Project Work

(B30201) MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN

M.Tech (ES)-I Semester	L	T	P	C
	3	0	0	3

UNIT –I: ARM Architecture
ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

UNIT –II: ARM Programming Model – I
Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT –III: ARM Programming Model – II
Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

UNIT –IV: ARM Programming
Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT –V: Memory Management
Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.

TEXT BOOKS:

1. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.

REFERENCE BOOKS:

1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.

Course Outcomes:

1. Expected to understand the selection procedure of Processors in the Embedded domain.

2. Design Procedure for Embedded Firmware.
3. Expected to visualize the role of Real Time Operating Systems in Embedded Systems
4. Expected to evaluate the Correlation between task synchronization and latency issues

(B30202) EMBEDDED PROGRAMMING

M.Tech (ES)-I Semester	L	T	P	C
	3	0	0	3

UNIT – I: Programming Embedded Systems in C
Introduction, what is an embedded system, which processor should you use, which programming language should you use, which operating system should you use, how do you develop embedded software, Conclusions
Introducing the 8051 Microcontroller Family: Introduction, What's in a name, the external interface of the Standard 8051, Reset requirements, Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption, Conclusions

UNIT – II: Reading Switches
Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code), Example: Counting goats, Conclusions

UNIT – III: Adding Structure to your Code
Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example, Example: Restructuring the goat-counting example, Further examples, Conclusions

UNIT – IV: Meeting Real-Time Constraints
Introduction, Creating 'hardware delays' using Timer 0 and Timer 1, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2?, The need for 'timeout' mechanisms, Creating loop timeouts, Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions

UNIT – V: Case Study: Intruder Alarm System
Introduction, The software architecture, Key software components used in this example, running the program, the software, Conclusions

TEXT BOOKS:

1. Embedded C by **Michael J. Pont** , A Pearson Education

REFERENCE BOOKS:

1. PIC micro MCU C-An introduction to programming, The Microchip PIC in CCS C By Nigel Gardner

Course Outcomes:

1. Explain the basics of Embedded C with reference to 8051.
2. Demonstrate how to handle control and data pins at hardware level.
3. Introduce objective nature of Embedded C.
4. Explain the specifications of real time embedded programming with case studies.

(B30215) VLSI TECHNOLOGY & DESIGN
(PROFESSIONAL ELECTIVE- I)

M.Tech (ES)-I Semester	L	T	P	C
	3	0	0	3

UNIT –I: Review of Microelectronics and Introduction to MOS Technologies:
MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: $I_{ds} – V_{ds}$ relationships, Threshold Voltage V_T, G_m, G_{ds} and ω_o, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Z_{pu}/Z_{pd}, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT –II: Layout Design and Tools:
Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.
Logic Gates & Layouts: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT –III: Combinational Logic Networks:
Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT–IV: Sequential Systems:
Memory cells and Arrays, clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT –V: Floor Planning:
Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A. Pucknell, 2005, PHI.
2. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Principals of CMOS VLSI Design – N.H.E Weste, K. Eshraghian, 2nd Ed., Addison Wesley.

Course Outcomes:

1. Explain the concepts of FET fundamentals for VLSI design.
2. Narrate stick diagrams and layouts.
3. Design the subsystems based on VLSI concepts.

(B30216) IMAGE & VIDEO PROCESSING

(PROFESSIONAL ELECTIVE- I)

M.Tech (ES)-I Semester	L	T	P	C
	3	0	0	3

UNIT – I: Fundamentals of Image Processing and Image Transforms
Basic steps of Image Processing System Sampling and Quantization of an image, Basic relationship between pixels.
Image Segmentation: Segmentation concepts, Point, Line and Edge Detection, Thresholding, Region based segmentation.

UNIT – II: Image Enhancement
Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, smoothing spatial filters, Sharpening spatial filters. Frequency domain methods: Basics of filtering in frequency domain, image smoothing, image sharpening, Selective filtering.

UNIT – III: Image Compression
Image compression fundamentals - Coding Redundancy, Spatial and Temporal redundancy, Compression models: Lossy & Lossless, Huffman coding, Bit plane coding, Transform coding, Predictive coding, Wavelet coding, Lossy Predictive coding, JPEG Standards.

UNIT - IV: Basic Steps of Video Processing
Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, Filtering operations.

UNIT – V: 2-D Motion Estimation
Optical flow, General Methodologies, Pixel Based Motion Estimation, Block- Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

TEXT BOOKS:

1. Digital Image Processing – Gonzaleze and Woods, 3rd ed., Pearson.
2. Video Processing and Communication – Yao Wang, Joem Ostermann and Ya–quin Zhang. 1st Ed., PH Int.

REFRENCE BOOKS:

1. Digital Video Processing – M. Tekalp, Prentice Hall International
2. Digital Image Processing – S.Jayaraman, S.Esakkirajan, T.Veera Kumar–TMH, 2009

Course Outcomes:

1. Explain image representation, filtering, compression.
2. Describe the basics of video processing, representation, motion estimation.

(B30217) SYSTEM DESIGN WITH EMBEDDED LINUX
(PROFESSIONAL ELECTIVE – I)

M.Tech (ES)-I Semester	L	T	P	C
	3	0	0	3

UNIT-I:
Embedded Linux Vs Desktop Linux, Embedded Linux Distributions

UNIT-II: Embedded Linux
Architecture, Kernel Architecture – HAL, Memory manager, Scheduler, File System, I/O and
Networking subsystem, IPC, User space, Start-up sequence

UNIT-III : Board Support Package
Embedded Storage: MTD, Architecture, Drivers, Embedded File System
Embedded Drivers: Serial, Ethernet, I2C, USB, Timer, Kernel Modules

UNIT-IV: Porting Applications
Real-Time Linux: Linux and Real time, Programming, Hard Real-time Linux

UNIT –V: Building and Debugging:
Kernel, Root files system, Embedded Graphics and Case study of uClinux

TEXT BOOKS:
1. Karim Yaghmour, "Building Embedded Linux Systems", O'Reilly & Associates
2. P Raghvan, Amol Lad, Sriram Neelakandan, "Embedded Linux System Design and Development", Auerbach Publications

REFRENCE BOOKS:
1. Christopher Hallinan, "Embedded Linux Primer: A Practical Real World Approach", Prentice Hall, 2nd Edition, 2010.
2. Derek Molloy, "Exploring Beagle Bone: Tools and Techniques for Building with Embedded Linux", Wiley, 1st Edition, 2014.

Course Outcomes:

At the end of this course, students will be able to

1. Expalin the embedded Linux development model.
2. Write, debug, and profile applications and drivers in embedded Linux.
3. Create Linux BSP for a hardware platform

(B30218) EMBEDDED NETWORKING
(PROFESSIONAL ELECTIVE – II)

M.Tech (ES)-I Semester	L	T	P	C
	3	0	0	3

UNIT –I: Embedded Communication Protocols:
Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Fire wire.

UNIT –II: USB and CAN Bus:
USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration – Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.

UNIT-III: Ethernet Basics
Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.

UNIT-IV: Embedded Ethernet
Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT –V: Wireless Embedded Networking:
Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.

Text books
1. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, Tony Givargis, John & Wiley Publications, 2002

2. Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port - Jan Axelson, Penram Publications, 1996.

Reference books

1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series - Dogan Ibrahim, Elsevier 2008.
2. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003.
3. Networking Wireless Sensors - Bhaskar Krishnamachari , Cambridge press 2005.

Course Outcomes:

At the end of this course, students will be able to

1. Expected to acquire knowledge on communication protocols of connecting Embedded Systems.
2. Expected to master the design level parameters of USB and CAN bus protocols.
3. Formulate the design issues of Ethernet in Embedded networks.
4. Acquire the knowledge of wireless protocols in Embedded domain.

(B30219) CPLD AND FPGA ARCHITECTURES & APPLICATIONS
(PROFESSIONAL ELECTIVE – II)

M.Tech (ES)-I Semester	L	T	P	C
	3	0	0	3

UNIT-I: Introduction to Programmable Logic Devices
Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II: Field Programmable Gate Arrays
Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT -III: SRAM Programmable FPGAs
Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT -IV: Anti-Fuse Programmed FPGAs
Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT -V: Design Applications
General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

Text Books

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

Reference Books

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K.

Chan/Samiha Mourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

Course Outcomes
After completion of the course students able to

1. Illustrate the features and architectures of industrial CPLDs with different families.
2. Explain the features and architectures of industrial FPGAs with different families.
3. Use programming techniques in FPGA design methodology.
4. Design and implement complex real time digital circuits.

(B30220) EMBEDDED COMPUTING
(PROFESSIONAL ELECTIVE – II)

M.Tech (ES)-I Semester	L	T	P	C
	3	0	0	3

UNIT –I: Programming on Linux Platform
System Calls, Scheduling, Memory Allocation, Timers, Embedded Linux, Root File System, Busy Box. **Operating System Overview**: Processes, Tasks, Threads, Multi-Threading, Semaphore, Message Queue.

UNIT –II: Introduction to Software Development Tools
GNU GCC, make, gdb, static and dynamic linking, C libraries, compiler options, code optimization switches, lint, code profiling tools,

UNIT –III: Interfacing Modules
Sensor and actuator interface, data transfer and control, GPS, GSM module interfacing with data processing and display, OpenCV for machine vision, Audio signal processing.

UNIT –IV: Networking Basics
Sockets, ports, UDP, TCP/IP, client server model, socket programming, 802.11, Bluetooth, ZigBee, SSH, firewalls, network security.

UNIT –V: IA32 Instruction Set
Application binary interface, exception and interrupt handling, interrupt latency, assemblers, assembler directives, macros, simulation and debugging tools.

TEXT BOOKS:
1. Modern Embedded Computing - Peter Barry and Patrick Crowley, 1st Ed., Elsevier/Morgan Kaufmann, 2012.
2. Linux Application Development - Michael K. Johnson, Erik W. Troan, Adission Wesley, 1998.
3. Assembly Language for x86 Processors by Kip R. Irvine
4. Intel® 64 and IA-32 Architectures Software Developer Manuals

REFERENCE BOOKS:
1. Operating System Concepts by Abraham Silberschatz, Peter B. Galvin and Greg Gagne.
2. The Design of the UNIX Operating System by Maurice J. Bach Prentice-Hall

3. UNIX Network Programming by W. Richard Stevens

Course Outcomes

After successful completion of the course, student will be able to

1. Write an Embedded Program on Linux and learn software development Tools.
2. Explain about Interfacing modules, Embedded Network basics and some communication modules.
3. Illustrate Instructions Sets for binary applications and assemblers.

(B30203) EMBEDDED PROGRAMMING LAB

M.Tech (ES)-I Semester	L	T	P	C
	0	0	4	2

Note: A minimum of 10 experiments has to be conducted.

The following programs have to be tested on 89C51 Development board/equivalent using Embedded C Language on Keil IDE or Equivalent.

1. Program to toggle all the bits of Port P1 continuously with 250 ms delay.
2. Program to toggle only the bit P1.5 continuously with some delay. Use Timer 0, mode 1 to create delay.
3. Program to interface a switch and a buzzer to two different pins of a Port such that the buzzer should sound as long as the switch is pressed.
4. Program to interface LCD data pins to port P1 and display a message on it.
5. Program to interface keypad. Whenever a key is pressed, it should be displayed on LCD.
6. Program to interface seven segment display unit.
7. Program to transmit a message from Microcontroller to PC serially using RS232.
8. Program to receive a message from PC serially using RS232.
9. Program to get analog input from Temperature sensor and display the temperature value on PC Monitor.
10. Program to interface Stepper Motor to rotate the motor in clockwise and anticlockwise directions
11. Program to Sort RTOS on to 89C51 development board.
12. Program to interface Elevator.

(B30204) SCRIPTING LANGUAGES LAB

M.Tech (ES)-I Semester	L	T	P	C
	0	0	4	2

Note: A minimum of 10 experiments has to be conducted.

Python Programming

1. Write a Python script to print prime numbers between 1-50.
2. Python script to a) Find the length of a string. b) Count no of words in a string. c). Reverse a string. d). Search for a specific string
3. Write a Python script that reads data from one file and write into another file.
4. a) Write a python Function to solve a quadratic equation.
   b) Write a Python function to find the factors of given number
5. a) Write a python program to find the factorial of a number.
   b) Write a python program to generate Fibonacci series.
6. Write a python program to make a simple calculator.
7. Write a python program to sort words in alphabetical order.
8. Write a python program to add two matrices.
   a). Write a Python program for displaying employee table from the database containing fields (empid, empname, age, gender)
   b). Write a Python Program for lottery game
9. Write a Python program for finding Names of the persons from the given text file containing personal information
10. Write a Python program for Sudoku game
11. Write a Python program for plotting bar chart,line chart, pie chart and scatter plot using plotly or matplotlib
12. Write a putin program for finding eigen values using numpy

Suggested Reading:

Programming Python, 4th edition. Powerful Object-Oriented Programming Mark Lutz. O'Reilly, 2010

(B30212) RESEARCH METHODOLOGY AND IPR

M. Tech (ES) – I Semester

L	T	P	C
2	0	0	2

UNIT-I

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem.

Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations.

UNIT-II

Effective literature studies approach, analysis, Plagiarism, Research ethics, Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee.

UNIT-III

Nature of Intellectual Property: Patents, Designs, Trademarks and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT-IV

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

UNIT-V

New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

Suggested Reading

1. Stuart Melville and Wayne Goddard, “Research methodology: an introduction for science & engineering students’”
2. Wayne Goddard and Stuart Melville, “Research Methodology: An Introduction”
3. Ranjit Kumar, 2nd Edition, “Research Methodology: A Step by Step Guide for beginners”
4. Halbert, “Resisting Intellectual Property”, Taylor & Francis Ltd ,2007.

5. Mayall, “Industrial Design”, McGraw Hill, 1992.
6. Niebel, “Product Design”, McGraw Hill, 1974.
7. Asimov, “Introduction to Design”, Prentice Hall, 1962.
8. Robert P. Merges Peter S. Menell, Mark A. Lemley, “Intellectual Property in New Technological Age”, 2016.
9. T. Ramappa, “Intellectual Property Rights Under WTO”, S. Chand, 2008

Course Outcomes:

At the end of this course, students will be able to

1. Analyze research related information & formulate research problem.
2. Follow research ethics.
3. Explain the importance of IPR and the need of information about Intellectual Property Right to be promoted among students in general & engineering.
4. Illustrate how IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

(C30001) ENGLISH FOR RESEARCH PAPER WRITING

M.Tech (ES)-I Semester **L T P C**
2 0 0 0

Unit I

1. Planning and Preparation, Word Order, Breaking up long sentences.
2. Structuring Paragraphs and Sentences, Being Concise and Removing, Redundancy.
3. Avoiding Ambiguity and Vagueness

Unit II

4. Clarifying Who Did What. Highlighting Your Findings.
5. Hedging and Introduction

Unit III

6. Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

Unit IV

7. Key skills are needed when writing a Title
8. Key skills are needed when writing an Abstract
9. Key skills are needed when writing an Introduction
10. Skills needed when writing a Review of the Literature

Unit V

11. Skills are needed when writing the Methods
12. Skills needed when writing the Results
13. Skills are needed when writing the Discussion
14. Skills are needed when writing the Conclusions useful phrases
15. How to ensure paper is as good as it could possibly be the first-time submission

COURSE OUTCOMES

On completion of the course students will be able to

1. Identify the required word order in sentences.
2. Illustrate meaningful sentence structures.
3. Clarify the findings of his research.
4. Argue and defend his research methods.
5. Predict the outcome of his research and will write meaningful conclusions.

Suggested Studies

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Model Curriculum of Engineering & Technology PG Courses [Volume-I][41]
3. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
4. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman'sbook.
5. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht
6. Heidelberg London, 2011

SEMESTER - II

(B30205) SYSTEM ON CHIP ARCHITECTURE

M.Tech (ES)-II Semester	L	T	P	C
	3	0	0	3

UNIT –I: Introduction to the System Approach
System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT –II: Processors
Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT –III: Memory Design for SOC
Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation, SOC Memory System, Models of Simple Processor – memory interaction.

UNIT -IV: Interconnect Customization and Configuration
Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buse, Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT –V: Application Studies / Case Studies
SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques – Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

Course Outcomes:

1. Introduction to SOC Architecture and design.
2. Processor design Architectures and limitations
3. To acquires the knowledge of memory architectures on SOC.
4. To Illustrate the interconnection strategies and their customization on SOC.

(B30206) EMBEDDED REAL TIME OPERATING SYSTEM

M.Tech (ES)-II Semester	L	T	P	C
	3	0	0	3

UNIT – I: Introduction
Introduction to UNIX/LINUX, Overview of Commands, File I/O (open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT - II: Real Time Operating Systems
Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency.
Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT - III: Objects, Services and I/O
Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT - IV: Exceptions, Interrupts and Timers
Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT - V: Case Studies of RTOS
RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, Tiny OS, and Basic Concepts of Android OS.

TEXT BOOKS:

1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011

REFERENCE BOOKS:

1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh

Course Outcomes:

1. Explain real-time concepts such as pre-emptive multitasking, task priorities, priority inversions, mutual exclusion, context switching, and synchronization, interrupt latency and response time, and semaphores.
2. Describe how a real-time operating system kernel is implemented.
3. Able explain how tasks are managed and how the real-time operating system implements time management.
4. Discuss how tasks can communicate using semaphores, mailboxes, and queues.
5. Implement a real-time system on an embedded processor and work with real time operating systems like RT Linux, Vx Works, MicroC /OSII, Tiny Os

(B30221) DIGITAL SYSTEM DESIGN

(PROFESSIONAL ELECTIVE – III)

M.Tech (ES)-II Semester	L	T	P	C
	3	0	0	3

UNIT -I: Minimization and Transformation of Sequential Machines

The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines.

Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

UNIT -II: Digital Design:

Digital Design Using ROMs, PALs and PLAs, BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

UNIT -III: SM Charts

State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

UNIT -IV: Fault Modeling & Test Pattern Generation

Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model.

Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

UNIT -V: Fault Diagnosis in Sequential Circuits

Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment

TEXT BOOKS:

1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.

3. Logic Design Theory – N. N. Biswas, PHI

REFERENCE BOOKS:

1. Switching and Finite Automata Theory – Z. Kohavi , 2nd Ed., 2001, TMH
2. Digital Design – Morris Mano, M.D.Ciletti, 4th Edition, PHI.
3. Digital Circuits and Logic Design – Samuel C. Lee , PHI

Course Outcomes

After completion of the course students able to

1. Explain how to design complex digital systems using minimization techniques.
2. Explain the design approaches using PAL's and PLA's.
3. Design large scale digital systems using CPLDs and FPGAs.
4. Design and identify the faults in digital systems and diagnosis method for minimization faults.

(B30222) ANALOG AND DIGITAL CMOS VLSI DESIGN
(PROFESSIONAL ELECTIVE – III)

M.Tech (ES)-II Semester	L	T	P	C
	3	0	0	3

UNIT -I: Review
Basic MOS structure and its static behavior, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay, Stick diagram and Layout, Wire delay models. Inverter: Static CMOS inverter, Switching threshold and noise margin concepts and their evaluation, Dynamic behavior, Power consumption.

UNIT -II: Physical design flow
Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model, Machine model.
Combinational logic: Static CMOS design, Logic effort, Pass transistor logic, Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, CMOS transmission gate logic.

UNIT -III: Sequential logic
Static latches and registers, Bi-stability principle, MUX based latches, Static SR flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers and Non-bistable sequential circuit.
Advanced Technologies: Giga-scale dilemma, Short channel effects, High–k, Metal Gate Technology, FinFET, TFET etc.

UNIT -IV: Single Stage Amplifier
CS stage with resistance load, Divide connected load, Current source load, Triode load, CS stage with source degeneration, Source follower, Common-gate stage, Cascade stage, Choice of device models. **Differential Amplifiers:** Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbert cell.

UNIT -V: Operational amplifiers
One stage OPAMP, Two stage OPAMP, Gain boosting, common mode feedback, Slew rate, PSRR, Compensation of 2 stage OPAMP, Other compensation techniques.

TEXT BOOKS:

1. J P Rabaey, A P Chandrakasan, B Nikolic, "Digital Integrated circuits: A design perspective", Prentice Hall electronics and VLSI series, 2nd Edition.
2. Behzad Razavi , "Design of Analog CMOS Integrated Circuits", TMH, 2007.

REFERENCE BOOKS:

1. Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, 2nd Edition.
2. Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford, 3rd Edition
3. R J Baker, "CMOS circuit Design, Layout and Simulation", IEEE Inc., 2008. TMH, 3rdEdition

Course Outcomes:

At the end of this course, students will be able to

1. Analyze, design, optimize and simulate analog and digital circuits using CMOS constrained by the design metrics.
2. Connect the individual gates to form the building blocks of a system.
3. Use EDA tools like Cadence, Mentor Graphics and other open source software tools like Cadence

(B30223) COMMUNICATION BUSES & INTERFACES (PROFESSIONAL ELECTIVE – III)

M.Tech (ES)-II Semester	L	T	P	C
	3	0	0	3

UNIT -I:
Serial Busses- _ Physical interface, Data and Control signals, features.

UNIT -II:
Limitations and applications of RS232, RS485, I2C & SPI.

UNIT -III:
CAN- Architecture, Data transmission, Layers, Frame formats, applications.

UNIT -IV:
PCIe- Revisions, Configuration space, Hardware protocols, applications

UNIT -V:
USB- Transfer types, enumeration, Descriptor types and contents, Device driver

TEXT BOOKS:
1. Jan Axelson, "Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems ", Lakeview Research, 2nd Edition
2. Mike Jackson, Ravi Budruk, "PCI Express Technology", Mindshare Press

REFERENCE BOOKS:
1. Jan Axelson, "Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems", Lakeview Research, 2nd Edition
2. Wilfried Voss, "A Comprehensible Guide to Controller Area Network", Copperhill Media Corporation, 2nd Edition, 2005.

Courses Outcomes:
At the end of the course, students will be able to:
1. Select a particular serial bus suitable for a particular application.

2. Develop APIs for configuration, reading and writing data onto serial bus.
3. Design and develop peripherals that can be interfaced to desired serial bus.

(B30224) WIRELESS LANs AND PANs
(PROFESSIONAL ELECTIVE – IV)

M.Tech (ES)-II Semester	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

UNIT –I: Wireless System & Random-Access Protocols
Introduction, First and Second Generation Cellular Systems, Cellular Communications from 1G to 3G, Wireless 4G systems, The Wireless Spectrum; Random Access Methods: Pure ALOHA, Slotted ALOHA, Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA).

UNIT –II: Wireless LANs
Introduction, importance of Wireless LANs, WLAN Topologies, Transmission Techniques: Wired Networks, Wireless Networks, comparison of wired and Wireless LANs; WLAN Technologies: Infrared technology, UHF narrowband technology, Spread Spectrum technology

UNIT –III: The IEEE 802.11 Standard for Wireless LANs
Network Architecture, Physical layer, The Medium Access Control Layer; MAC Layer issues: Hidden Terminal Problem, Reliability, Collision avoidance, Congestion avoidance, Congestion control, Security, The IEEE 802.11e MAC protocol

UNIT –V: The IEEE 802.15 working Group for WPANs
Introduction, importance of Wireless PANs, The Bluetooth technology: history and applications, technical overview, the Bluetooth specifications, piconet synchronization and Bluetooth clocks, Master-Slave Switch; Bluetooth security; Enhancements to Bluetooth: Bluetooth interference issues, Intra and Inter Piconet scheduling, Bridge selection, Traffic Engineering, QoS and Dynamics Slot Assigment, Scatternet formation.

UNIT –V: The IEEE 802.15 working Group for WPANs
The IEEE 802.15.3, The IEEE 802.15.4, ZigBee Technology, ZigBee components and network topologies, The IEEE 802.15.4 LR-WPAN Device architecture: Physical Layer, Data Link Layer, The Network Layer, Applications; IEEE 802.15.3a Ultra wideband.

TEXT BOOKS:

1. Ad Hoc and Sensor Networks - Carlos de Morais Cordeiro and Dharma Prakash Agrawal, World Scientific, 2011.

2. Wireless Communications and Networking - Vijay K.Garg, Morgan Kaufmann Publishers, 2009.

REFERENCE BOOKS:

1. Wireless Networks - Kaveh Pahlaram, Prashant Krishnamurthy, PHI, 2002.
2. Wireless Communication- Marks Ciampor, Jeorge Olenewa, Cengage Learning, 2007

COURSE OUTCOMES:

After going through this course, the student will be able to

1. Explain about Wireless Systems & Networks and multiple division and modulation techniques used in LAN's and PAN's.
2. Adhere to the protocols and architecture while using Wireless Networks and decide which wireless standard is useful for different applications.
3. Work using WLANs and PANs and design project related to wireless communication systems.
4. Write scientific articles through term assignments.

(B30225) ADVANCED COMPUTER ARCHITECTURE (PROFESSIONAL ELECTIVE – IV)

M.Tech (ES)-II Semester	L	T	P	C
	3	0	0	3

UNIT -I: Fundamentals of Computer Design

Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, Quantitative principles of computer design, Amdahl's law.

Instruction set principles and examples- Introduction, classifying instruction set- memory addressing-type and size of operands, Operations in the instruction set.

UNIT –II: Pipelines

Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design:

Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT -III: Instruction Level Parallelism (ILP) - The Hardware Approach

Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, High performance instruction delivery- Hardware based speculation.

ILP Software Approach: Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues - Hardware verses Software.

UNIT –IV: Multi Processors and Thread Level Parallelism

Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – Memory architecture, Synchronization.

UNIT –V: Inter Connection and Networks

Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture: Intel IA-64 ILP in embedded and mobile markets

Fallacies and pit falls.

TEXT BOOKS:

1. John L. Hennessy, David A. Patterson - Computer Architecture: A Quantitative Approach, 3rd Edition, an Imprint of Elsevier.

REFERENCE BOOKS:

1. John P. Shen and Miikko H. Lipasti -, Modern Processor Design : Fundamentals of Super Scalar Processors
2. Computer Architecture and Parallel Processing - Kai Hwang, Faye A.Brigs., MC Graw Hill.

Course Outcomes:

After completion of the course students able to

1. Illustrate advanced computer architecture aspects
2. Describe and explain instruction level parallelism with static scheduling, out-of-order execution and network-on-chip architectures
3. Explain the operation of modern CPUs including pipelining, memory systems and busses.
4. Design and emulate a single cycle or pipelined CPU by given specifications.

(B30226) ADVANCED MICROCONTROLLER AND ITS APPLICATIONS

(PROFESSIONAL ELECTIVE – IV)

M.Tech (ES)-III Semester	L	T	P	C
	3	0	0	3

UNIT – I: Overview of Microcomputer systems

Addresses, General Operation of a computer, Microprocessors in Digital System design. Purpose of micro controller. Difference between microprocessor and microcontroller. Advantages and Disadvantages. Block diagram of a microcontroller – operation, Microcontroller functioning. Microprocessors architectures Architecture, RISC and CISC processors. Memory organization, ports, interrupts.

UNIT-II: Internal architecture

Introduction to ARM7TDMI processor – Pin Description, Pin functionality, internal architecture, Instruction Set and Instruction Cycle timings, ARM 32- bit and THUMB (16-bit) operating modes, Switching between ARM and THUMB instructions. Types of memory – Code memory, External Memory, Internal memory, Register Set

UNIT-III:

PIC16F877 Instructions Set, addressing modes, Assembly language Programs. PIC16F877 PERIPHERALS: Timers, CCP modules, ADC modules, configuration word and programming.

UNIT – IV: SERIAL COMMUNICATION MODULES

UART, I2C, PSP, EEPROM, Reset, Oscillator modes, configuration word and programming. INTERFACING: Interfacing of keys, Display - LEDs, 7-segment LED (multiplexed display) & LCDs, (Programs in assembly and C). DAC and ADC, generation of PWM with PIC micro controller. (Programs in assembly and C)

UNIT – V: APPLICATIONS OF MICROCONTROLLERS

EX: RPM meter, event counter, temperature, controller. (Programs in assembly and C). Development Tools: Simulators, debuggers, cross compilers, in-circuit Emulators for the microcontrollers.

TEXT BOOKS:

1. J.B.PEATMAN Design with PIC microcontrollers-, PHI 1998.
2. B Barrnett Cox & Cull, Embedded C programming and the microchip PIC- Thomson Publications 2004.

REFERENCE BOOKS:

1. Ajay .V. Deshmukh Micro Controller theory and Application, TATA McGraw –Hill, 2008, 1st Edition

Course Outcomes

After successful completion of the course, student will be able to

1 Explain the architecture of PIC microcontroller.
2 Program PIC microcontroller using various techniques.
3 Design and develop PIC microcontroller based embedded circuit.

(B30207) EMBEDDED SYSTEM DESIGN LAB

M.Tech (ES)-II Semester	L	T	P	C
	0	0	4	2

Note:

A. The following programs are to be implemented on ARM based Processors/Equivalent.
B. Minimum of 10 programs from Part –I and 6 programs from Part - II are to be conducted.

PART- I:

The following Programs are to be implemented on ARM Processor

1. Simple Assembly Program for
    a. Addition | Subtraction | Multiplication | Division
    b. Operating Modes, System Calls and Interrupts
    c. Loops, Branches
2. Write an Assembly programs to configure and control General Purpose Input/ Output (GPIO) port pins.
3. Write an Assembly programs to read digital values from external peripherals and execute them with the Target board.
4. Program for reading and writing of a file
5. Program to demonstrate Time delay program using built in Timer / Counter feature on IDE environment
6. Program to demonstrates a simple interrupt handler and setting up a timer
7. Program demonstrates setting up interrupt handlers. Press button to generate an interrupt and trace the program flow with debug terminal.
8. Program to Interface 8 Bit LED and Switch Interface
9. Program to implement Buzzer Interface on IDE environment
10. Program to Displaying a message in a 2 line x 16 Characters LCD display and verify the result in debug terminal.
11. Program to demonstrate I2C Interface on IDE environment
12. Program to demonstrate I2C Interface – Serial EEPROM

13. Demonstration of Serial communication. Transmission from Kit and reception from PC using Serial Port on IDE environment use debug terminal to trace the program.

14. Generation of PWM Signal
15. Program to demonstrate SD-MMC Card Interface.

PART- II:

Write the following programs to understand the use of RTOS with ARM Processor on IDE Environment using ARM Tool chain and Library:

1. Create an application that creates two tasks that wait on a timer whilst the main task loops.
2. Write an application that creates a task which is scheduled when a button is pressed, which illustrates the use of an event set between an ISR and a task
3. Write an application that Demonstrates the interruptible ISRs(Requires timer to have higher priority than external interrupt button)

4. a).Write an application to Test message queues and memory blocks. b).Write an application to Test byte queues
5. Write an application that creates two tasks of the same priority and sets the time slice period to illustrate time slicing.

Interfacing Programs:

6. Write an application that creates a two task to Blinking two different LEDs at different timings
7. Write an application that creates a two task displaying two different messages in LCD display in two lines.

8. Sending messages to mailbox by one task and reading the message from mailbox by another task.
9. Sending message to PC through serial port by three different tasks on priority Basis.
10. Basic Audio Processing on IDE environment.

(B30208) PROGRAMMABLE SYSTEM ON CHIP LAB

M.Tech (ES)-II Semester	L	T	P	C
	0	0	4	2

Note: Minimum of 10 experiments has to be conducted.

1. Write a program to toggle all the led to port and with some time delay using ARM7
2. Write a program to interface LCD with ARM7
3. Write a program to interface 4*4 matrix keypad with ARM7
4. Write a program for interfacing LED and PWM and to verify the output in the ARM7
5. Write a program to interface Stepper motor with ARM7
6. Write a program for interfacing of DC motor with ARM7
7. Write a program to study and characteristics of the programmable gain amplifier (PGA)
8. Write a Program realization of low pass, high pass and band pass filters and their characteristics
9. Write a program to interface ADC and DAC with PSOC
10. Digital function implementation using digital blocks A. Counter for blinking LED B. PWW Digital buffer and digital inverter
11. Write a program to verify Timer operation in different modes
12. Write a Program to interface stepper motor with PSOC

Reference Books

1. Michael J. Pont, “Embedded C”, Pearson Education, 2nd Edition, 2008.
2. Nigel Gardner, “The Microchip PIC in CCS C”. Ccs Inc, 2nd Revision Edition, 2002.

(C30002) VALUE EDUCATION

M.Tech (ES)-II Semester	L	T	P	C
	2	0	0	0

UNIT-I

1. Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism.
2. Moral and non- moral valuation. Standards and principles
3. Value judgements

Unit II

4. Importance of cultivation of values.
5. Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness.
6. Honesty, Humanity. Power of faith, National Unity
7. Patriotism. Love for nature ,Discipline

Unit III

8. Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline.
9. Punctuality, Love and Kindness.
10. Avoid fault Thinking.
11. Free from anger, Dignity of labour.

Unit IV

12. Universal brotherhood and religious tolerance.
13. True friendship.
14. Happiness Vs suffering, love for truth.
15. Aware of self-destructive habits.
16. Association and Cooperation.
17. Doing best for saving nature

Unit V

18. Character and Competence –Holy books vs Blind faith.
19. Self-management and Good health.
20. Science of reincarnation.
21. Equality, Nonviolence ,Humility, Role of Women.
22. All religions and same message.
23. Mind your Mind, Self-control.
24. Honesty, Studying effectively

Suggested reading

1. Chakroborty, S.K. “Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi

Course Outcomes

On completion of the course, students will be able to

1. Identifies the social values and work ethics.
2. Classifies the moral and non-moral values.
3. Demonstrates love and kindness to fellow human beings.
4. Draws inference from the Holy books about the characters and their competence.
5. Able to judge his fellow beings character through their behaviour.

III SEMESTER

(B30227) DESIGN OF FAULT TOLERANT SYSTEMS
(PROFESSIONAL ELECTIVE – V)

M.Tech (ES)- III Semester	L	T	P	C
	3	0	0	3

UNIT-I: Fault Tolerant Design

Basic concepts: Reliability concepts, Failures & faults, Reliability and Failure rate, Relation between reliability and mean time between failure, maintainability and availability, reliability of series, parallel and parallel-series combinational circuits.

Fault Tolerant Design: Basic concepts-static, dynamic, hybrid, triple modular redundant system (TMR), 5MR reconfiguration techniques, Data redundancy, Time redundancy and software Redundancy concepts.

UNIT-II: Self-Checking circuits & Fail-safe Design

Self-Checking Circuits: Basic concepts of self-checking circuits, Design of Totally self checking checker, Checkers using m out of n codes, Berger code, Low cost residue code.

Fail Safe Design: Strongly fault secure circuits, fail safe design of sequential circuits using partition theory and Berger code, totally self checking PLA design.

UNIT-III: Design for Testability

Design for testability for combinational circuits: Basic concepts of Testability, Controllability and observability, The Reed Muller's expansion technique, use of control and syndrome testable designs.

Design for testability by means of scan: Making circuits Testable, Testability Insertion, Full scan DFT technique- Full scan insertion, flip-flop Structures, Full scan design and Test, Scan Architectures-full scan design, Shadow register DFT, Partial scan methods, multiple scan design, other scan designs.

UNIT-IV: Logic Built-in-self-test:

BIST Basics-Memory-based BIST,BIST effectiveness, BIST types, Designing a BIST, Test Pattern Generation-Engaging TPGs, exhaustive counters, ring counters, twisted ring counter, Linear feedback shift register, Output Response Analysis-Engaging ORA's, One's counter, transition counter, parity checking, Serial LFSRs, Parallel Signature analysis, BIST architectures-BIST related terminologies, A centralized and separate

Board-level BIST architecture, Built-in evaluation and self test(BEST), Random Test socket(RTS), LSSD On chip self test, Self –testing using MISR and SRSG, Concurrent BIST, BILBO, Enhancing coverage, RT level BIST design-CUT design, simulation and synthesis, RTS BIST insertion, Configuring the RTS BIST, incorporating configurations in BIST, Design of STUMPS, RTS and STUMPS results.

UNIT-V: Standard IEEE Test Access Methods:

Boundary Scan Basics, Boundary scan architecture- Test access port, Boundary scan registers, TAP controller, the decoder unit, select and other units, Boundary scan Test Instructions-Mandatory instructions, Board level scan chain structure-One serial scan chain, multiple-scan chain with one control test port, multiple-scan chains with one TDI,TDO but multiple TMS, Multiple-scan chain, multiple access port, RT Level boundary scan-inserting boundary scan test hardware for CUT, Two module test case, virtual boundary scan tester, Boundary Scan Description language.

TEXTBOOKS:

1. Fault Tolerant & Fault Testable Hardware Design- Parag K.Lala, 1984,PHI
2. Digital System Test and Testable Design using HDL models and Architectures - Zainalabedin Navabi, Springer International Edition.

REFERENCES:

1. Digital Systems Testing and Testable Design-Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman, Jaico Books
2. Essentials of Electronic Testing- Bushnell & Vishwani D.Agarwal, Springers.
3. Design for Test for Digital IC’s and Embedded Core Systems-Alfred L. Crouch, 2008, Pearson Education.

Course Outcomes:

1. Describe fundamental concepts in fault tolerant design.
2. Design requirements of self check-in circuits
3. Test pattern generation using LFSR
4. Design for testability rules and techniques for combinational circuits
5. Explan scan architectures & Design of built-in-self test.

(B30228) CMOS MIXED SIGNAL DESIGN
(PROFESSIONAL ELECTIVE – V)

M.Tech (ES)- III Semester	L	T	P	C
	3	0	0	3

UNIT-I:
Switched Capacitor Circuits Introduction to Switched Capacitor circuits-basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT-II:
Phased Lock Loop (PLL) Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs- PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

UNIT-III:
Data Converter Fundamentals DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT-IV:
Nyquist Rate A/D Converters Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time- interleaved converters.

UNIT-V:
Oversampling Converters Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

TEXT BOOKS:
1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013

REFERENCE BOOKS:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters- Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience,2009

Course outcomes:

After the Completion of the course, the students will be able to

1. Demonstrate first order filter with least interference
2. Extend the concept of phase locked loop for designing PLL application with minimum jitter by considering non-ideal effects.
3. Design different A/D, D/A, modulators, demodulators and different filter for real time applications

(B30229) HARDWARE SOFTWARE CO-DESIGN
(PROFESSIONAL ELECTIVE – V)

M.Tech (ES)-II Semester	L	T	P	C
	3	0	0	3

UNIT –I: Co- Design Issues

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT –II: Prototyping and Emulation

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III: Compilation Techniques and Tools for Embedded Processor Architectures

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV: Design Specification and Verification

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V: Languages for System – Level Specification and Design-I

System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

TEXT BOOKS:

1. Hardware / Software Co- Design Principles and Practice – Jorgen

Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers

REFERENCE BOOKS:

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer

Course Outcomes:

1. Explain various types of models
2. Describe interrelationship between Hardware and software in a embedded system
3. Explain firmware development process and tools
4. Explain validation methods and adaptability.

(B30230) APPLICATION SPECIFIC INTEGRATED CIRCUITS DESIGN

(OPEN ELECTIVE)

M.Tech (ES)-III Semester	L	T	P	C
	3	0	0	3

UNIT-I: Types of ASICs

Design flow – Economics of ASICs – ASIC cell libraries – CMOS logic cell data path logic cells – I/O cells – cell compilers.

UNIT-II : ASIC Library design:

Transistors as resistors – parasitic capacitance – logical effort programmable ASIC design software: Design system – logic synthesis – half gate ASIC.

UNIT-III: Low level design entry

Schematic entry – low level design languages – PLA tools – EDIF – An overview of VHDL and Verilog.

UNIT-IV: Logic synthesis

Logic synthesis in Verilog & VHDL simulation.

UNIT-V: ASIC Construction

Floor Planning & Placement Algorithms -Routing

Text Books:

1. Application specific Integrated Circuits", J.S. Smith, Addison Wesley.
2. Principles of CMOS VLSI Design: A System Perspective, N. Westle & K. Eshraghian, Addison – Wesley Pub.Co.1985. Technological Age", 2016.

References:

1. Basic VLSI Design :Systems and Circuits, Douglas A. Pucknell & Kamran Eshraghian, Prentice Hall of India Private Ltd. , New Delhi , 1989.
2. Introduction to VLSI System,C. Mead & L. Canway, Addison Wesley Pub

3. Introduction to NMOS & VLSI System Design, A. Mukharjee, Prentice Hall,
4. Digital Integrated Circuits: A Design Perspective, Jan A. Rabey, Prentice Hall of India Pvt Ltd

Course Outcomes:

After completion of the course the student will be able to

1. Analyze different types of ASICs and their libraries.
2. Design programmable ASICs, Low level design ASICs using Verilog & VHDL.
3. Explain different methods of software ASIC design their simulation, testing and construction of ASICs.

(B30231) EMBEDDED SYSTEMS

(OPEN ELECTIVE)

M.Tech (ES)-III Semester	L	T	P	C
	3	0	0	3

UNIT-I: Embedded Computing & CPU fundamentals

Embedded Computing: Microprocessors, embedded design process, system description formalisms. Instruction sets- CISC and RISC;

CPU fundamentals: programming I/Os, co-processors, supervisor mode, exceptions, memory management units and address translation, pipelining, super scalar execution, caching, CPU power consumption.

UNIT-II: Embedded computing platform & Program design and analysis

Embedded Computing platform: CPU bus, memory devices, I/O devices, interfacing, designing with microprocessors, debugging techniques.

Program design and analysis: models of program, assembly and linking, compilation techniques, analysis and optimization of execution time, energy, power and size.

UNIT-III: Processes and operating systems

Multiple tasks and multiple processes, context switching, scheduling policies, inter-process communication mechanisms.

UNIT-IV: Hardware accelerators & Networks

Hardware accelerators: CPUs and accelerators, accelerator system design.

Networks: Distributed embedded architectures, networks for embedded systems, network-based design and Internet-enabled systems.

UNIT-V: System design techniques

Design methodologies, requirements analysis, system analysis and architecture design, quality assurance.

Text Books:

1. Wolf, W. Computers as components- Principles of embedded computing system design. Academic Press (Indian edition available

from Harcourt India Pvt. Ltd., 27M Block market, Greater Kailash II, New Delhi-110 048.)

Reference Books

1. Manuel Jiménez Rogelio, PalomeraIsidoro Couvertier "Introduction to Embedded Systems Using Microcontrollers and the MSP430" Springer Publications, 2014.
2. Frank Vahid, Tony D. Givargis, "Embedded system Design: A Unified Hardware/Software Introduction", John Wily & Sons Inc.2002.
3. Peter Marwedel, "Embedded System Design", Science Publishers, 2007.

Course Outcomes:

1. Explain the basis of selection of Processors in the Embedded domain.
2. Design Procedure for Embedded System.
3. Visualize the role of Real time Operating Systems in Embedded Systems
4. Evaluate the architectures & networks for Embedded system.

(B30331) RENEWABLE ENERGY SOURCES

(OPEN ELECTIVE)

M. Tech (ES) – III Semester

L	T	P	C
3	0	0	3

Unit – I: Solar Energy

Principles of solar radiation: Role and potential of new and renewable source, the solar energy option, Environmental impact of solar power, physics of the sun, the solar constant, extraterrestrial and terrestrial solar radiation, solar radiation on titled surface, instruments for measuring solar radiation and sun shine, solar radiation data.

Solar energy collection: Flat plate and concentrating collectors, classification of concentrating collectors, orientation and thermal analysis, advanced collectors. **Storage and applications**: Different methods, Sensible, latent heat and stratified storage, solar ponds. Solar Applications-solar heating/cooling technique, solar distillation and drying, photovoltaic energy conversion.

Unit-II: Wind energy

Sources and potentials, horizontal and vertical axis windmills, performance characteristics, Betz criteria

Unit-III: Bio-mass

Principles of Bio-Conversion, Anaerobic/aerobic digestion, types of Bio-gas digesters, gas yield, combustion characteristics of bio-gas, utilization for cooking, I.C. Engine operation and economic aspects.

Unit-IV: Geothermal energy

Resources, types of wells, methods of harnessing the energy, potential in India.

Ocean energy: OTEC, Principles utilization, setting of OTEC plants, thermodynamic cycles. Tidal and wave energy: Potential and conversion techniques, mini-hydel power plants, and their economics.

Unit-V: Direct energy conversion

Need for DEC, Carnot cycle, limitations, principles of DEC.

Text Books

1. Non-Conventional Energy Sources /G.D. Rai
2. Renewable Energy Technologies /Ramesh & Kumar /Narosa

Reference Books

1. Renewable energy resources/ Tiwari and Ghosal/ Narosa.
2. Non-Conventional Energy / Ashok V Desai /Wiley Eastern.
3. Non-Conventional Energy Systems / K Mittal /Wheeler
4. Solar Energy /Sukhame

Course Outcomes

On completion of the course, students will be able to

1. Interpret the principles of solar radiation, collection and application.
2. Explain the concepts of Wind energy generation
3. Demonstrate the concepts of Bio-mass energy and operation of IC engines
4. Illustrate the perception of Geo-thermal energy and production in India
5. Elucidate the ideology of direct energy conversion

(B30332) INDUSTRIAL SAFETY
(OPEN ELECTIVE)

M. Tech (ES) – III Semester

L	T	P	C
3	0	0	3

Unit-I
Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and fire fighting, equipment and methods.

Unit-II
Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

Unit-III
Wear and Corrosion and their prevention: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

Unit-IV
Fault tracing: Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment's
like, I. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.

Unit-V
Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of

mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

Reference:

1. Maintenance Engineering Handbook, Higgins & Morrow, Da Information Services.
2. Maintenance Engineering, H. P. Garg, S. Chand and Company.
3. Pump-hydraulic Compressors, Audels, Mcgrew Hill Publication.
4. Foundation Engineering Handbook, Winterkorn, Hans, Chapman & Hall London

Course outcomes:

Up on the completion of the course students will be able to

1. Demonstrate the concepts of industrial safety, accidents and preventive measures.
2. Explain the Fundamentals of maintenance engineering.
3. Explain Wear and Corrosion and their prevention
4. Interpret the Fault tracing and draw decision tree for problems in machine tools.
5. Explain the concepts of Periodic and preventive maintenance

(B30532) BIG DATA AND ANALYTICS

(OPEN ELECTIVE)

M. Tech (ES) – III Semester

L	T	P	C
3	0	0	3

Unit-I

Types of Digital Data-Classification of Digital Data; Introduction to Big Data- Characteristics of Data, Evolution of Big Data, Definition of Big Data, Challenges with Big Data, What is Big Data?, Why Big Data?, Traditional Business Intelligence (BI) versus Big Data, A Typical Data Warehouse Environment, A Typical Hadoop Environment.

Unit-II

Big Data Analytics-What is Big Data Analytics?, What Big Data Analytics Isn't?. Classification of Analytics; Data Science, Terminologies Used in Big Data Environments, Top Analytics Tools; The Big Data Technology Landscape-NoSQL (Not Only SQL), Hadoop.

Unit-III

Introducing Hadoop, Why Hadoop?, RDBMS versus Hadoop, Distributed Computing Challenges, History of Hadoop, Hadoop Overview-Use Case of Hadoop, Hadoop Distributors-HDFS (Hadoop Distributed File System)- Managing Resources and Applications with Hadoop YARN (Yet another Resource Negotiator)- Interacting with Hadoop Ecosystem.

Unit- IV

Introduction to MongoDB-What is MongoDB?, Why MongoDB?, Terms Used in RDBMS and MongoDB-Data Types in MongoDB, MongoDB Query Language Introduction to MAPREDUCE Programming-Introduction-Mapper, Reducer, Combiner, Partitioner, Searching, Sorting, Compression.

Introduction to Hive-What is Hive? Hive Architecture, Hive Data Types, Hive File Format, Hive Query Language (HQL).

Unit-V

Introduction to Pig-What is Pig?, The Anatomy of Pig, Pig on Hadoop, Pig Philosophy, Use Case for Pig: ETL Processing, Pig

Latin Overview, Data Types in Pig, Running Pig, Execution Modes of Pig, HDFS Commands, Relational Operators, Eval Function, Complex Data Types, Piggy Bank, User-Defined Functions (UDF), Parameter Substitution, Diagnostic Operator, Word Count Example using Pig.
Introduction to Machine Learning-Introduction to Machine Learning, Machine Learning Algorithms.

Textbooks:

1. Big Data and Analytics by by Seema Acharya (Author), Subhashini Chellappan, Wiley Publisher.

References:

1. Big Data, Black Book, by DT Editorial Services, Dreamtech Press (2016).

Course Outcomes:

Students shall be able to

1. Define Big Data.
2. Classify Analytics.
3. Create Big Data Applications using Hadoop frame work.
4. Analyse Machine Learning Algorithms.
5. Write Pig Scripts.

(B30533) PYTHON PROGRAMMING

(OPEN ELECTIVE)

M. Tech (ES) – III Semester

L	T	P	C
3	0	0	3

Unit-I

Introduction to Python Programming: How a Program Works, Using Python, Program Development Cycle, Input, Processing, and Output, Displaying Output with the Print Function, Comments, Variables, Reading Input from the Keyboard, Performing Calculations (Operators. Type conversions, Expressions), More about Data Output. Decision Structures and Boolean Logic: if, if-else, if-elif-else Statements, Nested Decision Structures, Comparing Strings, Logical Operators, Boolean Variables. Repetition Structures: Introduction, while loop, for loop, Calculating a Running Total, Input Validation Loops, Nested Loops

Unit-II

Functions: Introduction, Defining and Calling a Void Function, Designing a Program to Use Functions, Local Variables, Passing Arguments to Functions, Global Variables and Global Constants, Value-Returning Functions Generating Random Numbers, Writing Our Own Value-Returning Functions, The math Module, Storing Functions in Modules. File and Exceptions: Introduction to File Input and Output, Using Loops to Process Files, Processing Records, Exceptions

Unit-III

Lists and Tuples: Sequences, Introduction to Lists, List slicing, Finding Items in Lists with the in Operator, List Methods and Useful Built-in Functions, Copying Lists, Processing Lists, Two-Dimensional Lists, Tuples. Strings: Basic String Operations, String Slicing, Testing, Searching, and Manipulating Strings. Dictionaries and Sets: Dictionaries, Sets, Serializing Objects. Recursion: Introduction, Problem Solving with Recursion, Examples of Recursive Algorithms

Unit-IV

Object-Oriented Programming: Procedural and Object-Oriented Programming, Classes, Working with Instances, Techniques for Designing Classes, Inheritance, Polymorphism.

Unit-V

GUI Programming: Graphical User Interfaces, Using the tkinter Module, Display text with Label Widgets, Organizing Widgets with Frames, Button Widgets and Info Dialog Boxes, Getting Input with Entry Widget, Using Labels as Output Fields, Radio Buttons, Check Buttons.

TEXTBOOKS:

1. Starting Out with Python by Tony Gaddis, Pearson, 3 edition;

References:

1. Python Programming: Using Problem Solving Approach by Reema Thareja, Oxford University Press, First edition;
2. Fundamentals of Python, Kenneth A. Lambert, Cengage Learning,1 edition;
3. Foundations for Analytics with Python by Clinton W. Brownley, O'Reilly Media; 1 edition

Course Outcomes:

Students shall be able to

1. Develop simple applications using Python.
2. Write modular programs in python.
3. Work with python instances.
4. Develop GUI applications using python.

(B30431) GREEN BUILDINGS

(OPEN ELECTIVE)

M. Tech (ES) – III Semester

L	T	P	C
3	0	0	3

Unit-I

Overview of the significance of energy use and energy processes in building - Indoor activities and environmental control - Internal and external factors on energy use and the attributes of the factors - Characteristics of energy use and its management - Macro aspect of energy use in dwellings and its implications.

Unit-II

Indoor environmental requirement and management - Thermal comfort - Ventilation and air quality - Air-conditioning requirement - Visual perception - Illumination requirement - Auditory requirement.

Unit-III

Climate, solar radiation and their influences - Sun-earth relationship and the energy balance on the earth's surface - Climate, wind, solar radiation, and temperature - Sun shading and solar radiation on surfaces - Energy impact on the shape and orientation of buildings.

Unit-IV

End-use, energy utilization and requirements - Lighting and day lighting - End -use energy requirements - Status of energy use in buildings Estimation of energy use in a building. Heat gain and thermal performance of building envelope - Steady and non-steady heat transfer through the glazed window and the wall - Standards for thermal performance of building envelope -Evaluation of the overall thermal transfer.

Unit-V

Energy management options - Energy audit and energy targeting - Technological options for energy management.

Reference Books

1. J. Krieder and A. Rabl, Heating and Cooling of Buildings - Design for Efficiency, McGraw Hill, 1994.
2. S.M. Guinnes and Reynolds, Mechanical and Electrical Equipment for Buildings, Wiley, 1989.
3. Shaw, Energy Design for Architects, AEE Energy Books, 1991.

4. ASHRAE, Handbook of Fundamentals, Atlanta, 1997.
5. Donald W. Abrams, Low Energy Cooling – A Guide to the Practical Application of Passive Cooling and Cooling Energy Conservation Measures, Van Nostrand Reinhold Co., New York, 1986

Course Outcomes

After completing this course, students will be able to:

1. Describe and use the basic terms and concepts used in green buildings.
2. Recognize and analyze green buildings.
3. Identify and define green building systems and materials.
4. Analyze and solve design problems utilizing principles of green building.
5. Assimilate knowledge gained in this course to evaluate green buildings.

(B30432) CONSTRUCTION PROJECT MANAGEMENT

(OPEN ELECTIVE)

M. Tech (ES) – III Semester

L	T	P	C
3	0	0	3

Unit-I

Management process- Roles, management theories, Social responsibilities, planning and strategic management, strategic implementation, Decision making tools and techniques-Organizational structure, Human resource management- motivation performance- leadership.

Unit-II

Classification of construction projects, Construction Stages, Resources-Functions of Construction Management and its Applications, Preliminary planning –Collection of Data-Contract planning –Scientific Methods of Management; Network Techniques in construction management- Bar Chart-Grant Chart, CPM- PERT-Cost & Time optimization.

Unit-III

Resource planning – planning for manpower, materials, Cost, equipment, Labour, Scheduling, Forms of, Scheduling-Resource allocation, budget and budgetary control methods.

Unit-IV

Contract-types of contract, contract document, specification, important conditions of contract- tender and tender document- Deposits by contractor –Arbitration, negotiation – M- Book –Muster rolls- stores.

Unit-V

Management information systems- Labour Regulations: Social security-welfare Legislation-laws relating to wages , Bonus and industrial disputes, Labour administration – insurance and safety Regulations- Workmen‘s compensation Act – other labour laws- safety in construction : legal and financial aspects of accidents in construction , occupational and safety hazard assessment , human factors in safety , legal and financial aspects of accidents , occupational and safety hazard assessment.

Text Books

1. Ghalot, P.S., Dhir, D.M., Construction planning and Management, Wiley Eastern limited,1992

2. Chikara, K.K., Construction Project Management, Tata McGraw Hill publishing Co, Ltd New Delhi,1998
3. Punima, B.C., Project planning and Control with PERT and CPM, Laxmi Publications New Delhi 1987

Reference:

1. Construction Management and Planning by Sengupta, B. Guha, H., Tata McGraw Hill Publications

Course Outcomes:

Upon the successful completion of this course, the students will be able to:

1. Explain the importance of construction planning and functioning of various earth moving equipment.
2. Explain of production of aggregate products and concreting.
3. Apply the gained knowledge to project management and construction techniques.