EDC COURSE FILE

CMR COLLEGE OF ENGINEERING & TECHNOLOGY

KANDLAKOYA, MEDCHAL, HYDERABAD.

ECE DEPARTMENT

Electronic Devices And Circuits COURSE FILE

CONTENTS:

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2. Course Plan
3. Previous Question Papers
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COURSE SYLLABUS

(A2401) ELECTRONIC DEVICES AND CIRCUITS

UNIT-I: P-N JUNCTION DIODE

Qualitative theory of p-n junction, p-n junction as a Diode, Diode equation, volt-ampere charecteristics,Temperature dependence of VI characteristic, Ideal versus practical-Resistance levels (static and dynamic),transition and diffusion capacitances, diode equivalent circuits, load line analysis,breakdown mechanisms in semiconductor diodes, Zener diode characteristics.

SPECIAL PURPOSE ELECTRONIC DEVICES

Principle of operation and characteristics of Tunnel diode (with the help of energy band diagram) and varactor diode, principle of operation of Schottky barrier diode, SCR and semiconductor photo diode.

UNIT-II: RECTIFIERS AND FILTERS

The P-N junction as a rectifiers, Half wave rectifier, Full wave rectifier ,Bridge rectifier, harmonic components in a rectifier circuit, Inductor filters, Capacitor filters, L-section filters, Pi-section filters, comparison of filters, voltage regulation using Zener diode.

UNIT-III: BIPOLAR JUNCTION TRANSISTOR

The junction transistor, transistor current components, transistor as an amplifier, transistor construction, BJT operation, BJT symbol, common base, common emitter and common collector configurations, limits of operation, BJT specifications. The Unijunction transistor.

UNIT-IV: TRANSISTOR BIASING AND STABILIZATION

Operating point, the DC and AC load lines, need for biasing, fixed bias, collector feedback bias, emitter feedback bias, collector–emitter feedback bias, voltage divider bias, bias stability, stabilization factors, stabilization against variations in V_{BE} and β, bias compensation using diodes and transistors, thermal runaway, thermal stability. BJT hybrid model, determination of h-parameters from transistor characteristics, analysis of a transistor amplifier circuit using h-parameters, comparison of CB, CE, CC amplifier configurations.

UNIT-V: FIELD EFFECT TRANSISTOR

The junction field effect transistor (construction, principle of operation, symbol)-pinch –off voltage, volt-amp characteristics, the JFET small signal model, MOSFET (construction, principle of operation, symbol), MOSFET characteristics in enhancement and depletion modes

FET AMPLIFIERS

FET common source amplifier, common drain amplifier, generalized FET amplifier, biasing FET, FET as voltage variable resistor, comparison of BJT and FET.

TEXT BOOKS:

1. Milliman's electronic devices and circuits-J.Millman, C.C.Halkias, and Satyabrata Jit, second ed...1998, TMH.
2. Electronic devices and circuits-R.L.Boylestad and Louis Nashelsky, 9 ed…2006, PEI/PHI.
3. Introduction to electronic devices and circuits-Robert T.Paynter, PE, PE.

REFERENCES:

1. Integrated electronics –J.Millman and Christos C.Halkias, 1991 ed..2008, TMH.
2. Electronic devices and circuits –K.Lal kishore,2 ed..,2005,BSP.
3. Electronic devices and circuits-Anil K.Maini, Varsha Agarwal, 1 ed...2009, wileyIndia Pvt Ltd.
4. Electronic devices and circuits-S.Salivahanan, N.Suresh kumar,A.Vallavaraj,2 ed..2008,TMH

COURSE PLAN

CMR COLLEGE OF ENGINEERING & TECHNOLOGY

Kandlakoya (V), Medchal (M), RR Dist. A.P.

DEPARTMENT OF ECE

COURSE PLAN

Subject: ELECTRONIC DEVICES AND CIRCUITS

Class: B.Tech III Semester EEE-A Section

A.Y: 2017-18

Name of the Faculty: Mr. B.CHAKRADHAR

Unit / Topic	No. Of Periods Required	Cumulative Periods	Planned Date	Covered Date
Unit-1: P-N Junction Diode				
Introduction to Electronic Devices & Circuits	2	2	4/7/2017	
Introduction &Qualitative Theory of p-n junction	3	5	6/7/2017	
p-n junction as a Diode	1	6	11/7/2017	
Diode Equation	2	8	12/7/2017	
Volt-Ampere Characteristics	1	9	14/7/2017	
Temperature dependence of VI characteristics, static and Dynamic Resistances	1	10	19/7/2017	
Transition and Diffusion Capacitances	2	12	20/7/2017	
Diode Equivalent Circuits, Load Line Analysis	1	13	21/7/2017	
Breakdown Mechanisms in Semiconductor Diodes, Zener Diodes Characteristics.	1	14	25/7/2017	
Special Purpose Electronic Devices				
Principle of Operation and Characterises of Tunnel Diode	1	15	27/7/2017	

Varactor Diode	1	16	28/7/2017	
SCR characteristics	1	17	1/8/2017	
Semiconductor photo Diode	1	18	28/7/2017	
Unit II: Rectifiers and Filters				
The p-n junction as a rectifier	1	19	3/8/2017	
Half wave Rectifier	1	20	4/8/2017	
Centre tapped Full Wave Rectifier, Bridge Rectifier	2	22	9/8/2017	
Harmonic Components in a Rectifier Circuit	1	23	11/8/2017	
Inductor Filters	1	24	16/8/2017	
Capacitor filters, L-section Filters	1	25	17/8/2017	
π-Section Filters ,Comparison of Filters	1	26	18/8/2017	
Voltage regulation using Zener Diode	1	27	23/8/2017	
Unit-III: Bipolar Junction Transistor				
The Junction Transistor	1	28	24/8/2017	
Transistor as an amplifier	1	29	24/8/2017	
Transistor Construction, BJT Operation, BJT symbol	1	30	25/8/2017	
Common Base configuration	1	31	29/8/2017	
Common Emitter Configuration	2	33	30/8/2017	
Common Collector Configuration	1	34	1/9/2017	
Limits of Operation ,BJT Specifications	1	35	5/9/2017	
BJT Hybrid Model	1	36	12/9/2017	
Determination of h-parameter from Transistor characteristics	1	37	13/9/2017	
Analysis of a Transistor Amplifier Circuit using h-parameters	2	39	15/9/2017	
Comparison of CB,CE and CC Amplifier Configurations	1	40	20/9/2017	

Uni Junction Transistor	1	41	22/9/2017	
Unit-IV:Transistor Baising and Stabilization				
Operating Point, The DC and AC Load lines	1	42	26/9/2017	
Need for Biasing, Fixed Bias	1	43	27/9/2017	
Collector FeedBack Bias, Emitter Feedback Bias	1	44	28/9/2017	
Collector-Emitter Feedback Bias	1	45	29/9/2017	
Voltage Divider Bias	1	46	3/10/2017	
Bias Stability ,Stabilization Factors	2	48	4/10/2017	
Stabilization against variations in VBE	1	49	4/10/2017	
Bias Compensation using Diodes and Transistors	2	51	5/10/2017	
Thermal Runaway ,Thermal Stability	2	53	6/10/2017	
Unit-V: Field Effect Transistor				
The junction Field Effect transistor(Construction, Principle of operation, symbol)-pinch-off voltage	2	5	10/10/2017	
volt-Ampere Characteristics ,The JFET Small Signal Model	2	57	11/10/2017	
MOSFET(Construction, principle of operation, symbol)	2	59	12/10/2017	
MOSFET characteristics in Enhancement and Depletion modes	1	60	13/10/2017	
FET Amplifiers				
FET Common Source Amplifier	2	62	20/10/2017	
FETCommon Drain Amplifier, Generalized FET Amplifier	3	65	24/10/2017	
Biasing FET	1	66	25/10/2017	
FET as Voltage Variable Resistor	1	67	26/10/2017	
Comparison of BJT ,FET and UJT	2	69	26/10/2017	

TEXT BOOKS:

1. Millman's Electronic Devices and Circuits- JACOB.MILLMAN, C.C.HALKIAS, and SATYABRATA JIT, 3rd edition. 1998, TMH

2. Electronic Devices and Circuit Theory-R.L.Boylestad and Louis Nashelsky, 11th edition, PEI/PHI.

3. Introduction to Electronic Devices and Circuits -Rober T.paynter, PE.

REFERENCE BOOKS

1. Integrated Electronics –J.Millman and Christos C.Halkias, 1991 ed., 2008, TMH.
2. Electronic Devices and Circuits-K.Lal Kishore, 2ed. 2005, BSP.
3.Electronic Devices and Circuits-Anil K.Maini,Varsha Agarwal,1 ed., 2009,wiley India Pvt.Ltd.

4. Electronic Devices and Circuits-S.Salivahanan, N.Suresh Kumar, A.Vallavaraj, 2 ed., 2008, TMH.

Initials of the Faculty **Initials of the HOD** **Initials of the Principal**

PREVIOUS QUESTION PAPERS

Hall Ticket No. | | | | | | | | | | |

Question Paper Code: A1401

CMR COLLEGE OF ENGINEERING & TECHNOLOGY

(AUTONOMOUS)

B.Tech III Semester Supplementary Examinations NOV/DEC– 2016

(Regulation: CMRCET-R14)

ELECTRONIC DEVICES & CIRCUITS

(EEE & ECE)

Date:02.12.2016 AN | Time: 3 hours | Max.Marks:70

PART-A

Answer all TEN questions (Compulsory)

Each question carries TWO marks. 10x2=20M

1. When a reverse bias is applied to a Ge PN junction diode, the reverse saturation current at room temperature is 0.3μA. Determine the current flowing in the diode when 0.15V forward bias is applied at room temperature?
2. Define a load line in a simple diode circuit?
3. What are the advantages of Bridge rectifier?
4. Calculate the value of inductance to use in the inductor filter connected to a fullwave rectifier operating at 60Hz to provide a DC output with 4% ripple for a 100Ω load?
5. Define intrinsic stand-off ratio of UJT?
6. The reverse saturation current in a transistor is 8μA. If the transistor common base current gain is 0.979, calculate the collector and emitter currents for 40μA base current?
7. What is the condition for thermal stability?Explain?
8. Determine the emitter current I_E , collector current I_C for a transistor with α_{dc}=0.97 and collector to base leakage current 10μA, I_B is 50μA?
9. Explain how an FET is used as a voltage variable resistor?
10. For a given JFET, I_{DSS}=15mA, V_p=-4V, V_{DS}=10V. Find the value of resistance Rs for a drain current of I_{DS}=7mA?

PART-B

Answer any FIVE questions. One question from each unit either A or B (Compulsory)

Each question carries TEN Marks. 5x10=50M

11) A. i. Find the value of dc resistance and ac resistance of a Germanium diode at 25^0C with Io=25 μA and at an applied voltage of 0.2V across the diode? [5M]

ii. With a neat sketch, explain the operation of PN junction diode? [5M]

(OR)

B. i. If two similar Germanium diodes are connected back to back and the voltage V is impressed upon, Determine the voltage across each diode and current through each diode. Assume similar value of Io=1 μA for both the diodes and η=1? [5M]

ii. Explain the two transistor analogy of an SCR? [5M]

12) A. i. A full wave rectifier is fed with a voltage, 50Sin100πt. Its load resistance is 400Ω. The diodes used in the rectifier have an average forward resistance of 30Ω. Compute the
(i) Average and rms values of load current, [6M]
(ii) Ripple factor and
(iii) Efficiency of rectification.

ii. Define line regulation and load regulation in a voltage regulator? [4M]

(OR)

B. i. Discuss about the Zener breakdown mechanism in detail. [4M]
ii. Draw the circuit diagram of Zener shunt regulator and explain in detail? [6M]

13) A. Draw the circuit diagram for a transistor in CE configuration and explain its i/p and o/p characteristics with neat sketches.

(OR)

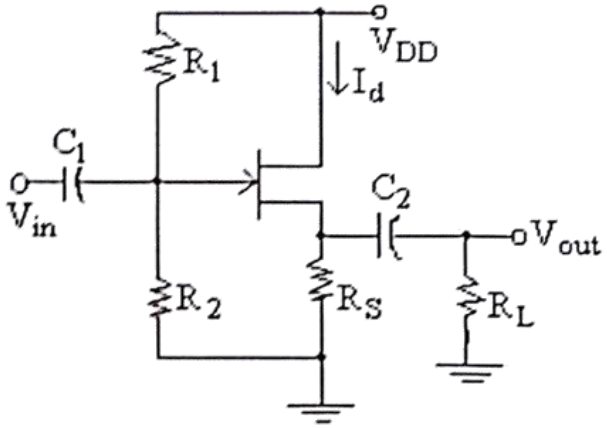
B. Derive the equations for voltage gain, current gain, input impedance and output admittance for a BJT using low frequency h-parameters model for CC configuration?

14)A. Determine the quiescent current and collector to emitter voltage for a Ge transistot with β=50 in self biasing arrangement. Draw the circuit with a given component value with Vcc=20V, Rc=2Kohm, Re=100ohms, R1=100Kohm, and R2=5Kohm. Also find the stability factor?

(OR)

B. i. What is transistor biasing? What are the basic conditions which are to be necessarily fulfilled for achieving faithful amplification of input signal in transistor amplifiers? [5M]
ii. Derive an expression for the stability factor of an emitter-feedback bias circuit? [5M]

15) A. The FET circuits given below has R1=3.5MΩ, R2=1.5MΩ, R_S=2KΩ, R_L=20KΩ & gm=2.5mS. Find its input impedance, output impedance and voltage gain?



(OR)

B. Draw a generalized FET amplifier circuit and its Thevenins equivalent circuits and find the voltage gain, output resistance and input resistance of CD amplifier circuits?

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Hall Ticket No. | | | | | | | | | | Question Paper Code: A1401

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
B.Tech III Semester Supplementary Examinations May–2017
(Regulation: CMRCET-R14)
ELECTRONIC DEVICES & CIRCUITS
(Common to EEE & ECE)

Date:10.05.2017 Time: 3 hours Max.Marks:70

PART-A
Answer all TEN questions (Compulsory)
Each question carries TWO marks. 10x2=20M

1. What is semiconductor?
2. What is energy level diagram?
3. What is rectifier explain the ripple factor of bridge rectifier
4. Explain the ripple factor of L-section filter
5. Write the characteristics of JFET
6. What is pinch off voltage?
7. What do you understand by DC and AC load line?
8. What is meant by operating point Q?
9. Define the channel width of JFET.
10. Define Base spreading resistance.

PART-B
Answer any FIVE questions. One question from each unit either A or B (Compulsory)
Each question carries TEN Marks. 5x10=50M

11) A. Explain the working of P-N junction diode with its V-I characteristics and mention the applications of P-N junction diode

(OR)

B. Explain the Zener diode and it's breakdown mechanism?

12) A. Draw the circuit diagram of a full wave rectifier and explain its working principle. Derive expression for the ripple factor , regulation and efficiency.

(OR)

B. Explain the working of zener voltage regulator with neat circuit diagram.

(P.T.O)

13) A. Explain the operation of BJT and its modes of operations?

(OR)

B. Write comparisons of CC, CE, and CB configuration?

14) A. What is thermal runaway? Explain about thermal runaway and explain how to avoid thermal runaway in BJT circuit.

(OR)

B. What is biasing and what is need of biasing and explain collector –base bias.

15) A. Explain the operation of JFET.

(OR)

B. Explain the operation of MOSFET in enhancement mode with neat sketches.

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Hall Ticket No. | | | | | | | | | | Question Paper Code: A2401

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
B.Tech III Semester Regular Examinations NOV-2016
(Regulation: CMRCET-R15)
ELECTRONIC DEVICES & CIRCUITS
(Common to EEE & ECE)

Date:18.11.2016 Time: 3 hours Max.Marks:70

PART-A
Answer all TEN questions (Compulsory)
Each question carries TWO marks. 10x2=20M

1. What are the breakdown mechanisms in zener diode?
2. What are the applications of zener diodes?
3. Define ripple factor of a rectifier.
4. What is rectifier explain the ripple factor of bridge rectifier
5. Draw the o/p characteristics of CE configuration.
6. Define current amplification factor of a transistor CE configuration.
7. What is a bias? What is the need for biasing?
8. Why voltage divider bias is commonly used in amplifier circuits?
9. How FET is known as voltage variable resistor?
10. Define the channel width of JFET.

PART-B
Answer any FIVE questions. One question from each unit either A or B (Compulsory)
Each question carries TEN Marks. 5x10=50M

11) A. Explain the working of P-N junction diode with its V-I characteristics and mention the applications of P-N junction diode.

(OR)

B. Derive the expression for transition and diffusion capacitance.

12) A. Derive the ripple factor of full wave rectifier with capacitor filter.

(OR)

B. Draw the circuit diagram of a half wave rectifier and explain its working principle. Derive expression for the ripple factor , regulation and efficiency.

(P.T.O)

13) A. What is thermal runaway. Explain about thermal runaway and explain how to avoid thermal runaway in BJT circuit.

(OR)

B. What is biasing and what is need of biasing and explain fixed bias circuit.

14) A. Explain about CE configuration with neat sketches and draw the hybrid model for BJT in CE configuration.

(OR)

B. Write comparisons of CC, CE, and CB configuration?

15) A. Explain about FET common source amplifier.

(OR)

B. Explain about construction and principle of operation of junction field effect transistor.

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MID EXAM PAPERS

Hall Ticket No. | | | | | | | | | | | **Question Paper Code: A2401**

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

B.TECH III Semester Mid-1 Examinations September – 2017

(Regulation: CMRCET-R15)

Subject Name:EDC

Date: 09/09/2017 **Time: 10.00-11.20 AM**

Max.Marks:20

PART-A

Answer all five questions (Compulsory)

Each question carries ONE mark. **5x1=5Marks**

1. Define the Reverse saturation current and dynamic resistance of the PN diode.
2. Draw the symbol of Tunnel diode, Zener diode, Semiconductor photo diode and Varactor diode.
3. Compare the values of $I_{dc,}$ $V_{dc,}$ Efficiency, Ripple factor and PIV for HWR and Center tapped FWR.
4. Define the terms Line regulation and Load regulation.
5. Define current gain in CB configuration.

PART-B

Answer any THREE questions. Each question carries FIVE Marks. 03x5=15Marks

1. With neat energy band diagrams, explain the V-I characteristics of Tunnel diode. Also discuss the negative resistance property of Tunnel diode.
2. Discuss about the Avalanche breakdown and Zener breakdown mechanism in detail.
3. Explain the Centre tapped FWR with neat sketches, and derive the following
   i) DC current delivered to load ii) Rectifier Efficiency iii) Ripple Factor iv) PIV
4. Explain the working of Zener shunt regulator with neat circuit diagram.
5. Draw the circuit diagram for transistor in CB configuration and explain its i/p and o/p characteristics with neat sketches.

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Hall Ticket No. | | | | | | | | | | | **Question Paper Code: A2401**

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

B.TECH III Semester Mid-1 Examinations September – 2017

(Regulation: CMRCET-R15)

Subject Name:EDC

Date: 09/09/2017 **Time: 10.00-11.20 AM**

Max.Marks:20

PART-A

Answer all five questions (Compulsory)

Each question carries ONE mark. 5x1=5Marks

1. Discuss the effect of temperature on PN junction diode.
2. Define the Drift and Diffusion current.
3. Draw the block diagram of Regulated power supply.
4. What is the advantage of Bridge rectifier over centre tapped FWR.
5. What are the various modes of operating a BJT?

PART-B

Answer any THREE questions. Each question carries FIVE Marks. 03x5=15Marks

1. Discuss the capacitance effect in PN junction diode and derive the expression for Diffusion and Transition capacitance.
2. i) Which type of diode capacitance is utilized in Varactor diode operation? Explain its principle of operation.
   ii) Obtain the Transition capacitance of the junction diode at reverse bias voltage of 12V if the transition capacitance is 15PF at the reverse voltage of 8V.
3. With neat sketches explain the bridge rectifier in detail.
4. A Full wave rectifier uses two silicon diodes of forward resistances 20Ω each. A DC voltmeter connected across the load of 1 KΩ reads 55.4V calculate
   $i)$ I_{rms} ii) Average voltage across each diode iii) Ripple factor iv) Transformer secondary rating.
5. What is Base width modulation explain in detail.

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Hall Ticket No. | | | | | | | | | | | **Question Paper Code: A2401**

CMR COLLEGE OF ENGINERRING & TECHNOLOGY

(AUTONOMOUS)

B.Tech (ECE)-III SEMESTERIMID EXAMINATION, AUGUST -2016

Subject: Electronic Devices & CircuitsDate& Time: 10/07/2016&10:00 to 11.20AmMax Marks: 20

PART A

Answer all the following questions. (5 x 1 = 05)

6. Define the Reverse saturation current and dynamic resistance of the PN diode.
7. Draw the symbol of Tunnel diode, Zener diode, Semiconductor photo diode and Varactor diode.
8. Give the values of PIV, Ripple factor and Efficiency forHWR and Center tapped FWR.
9. Define the terms Line regulation and Load regulation.
10. Write the expression for Diode current and describe each term.

PART B

Answer any three of the following questions. (3 x 5 = 15)

6. With neat energy band diagrams, explain the V-I characteristics of Tunnel diode. Also discuss the negative resistance property of Tunnel diode.
7. Explain the concept of diode capacitance, derive expression for transition capacitance.
8. Define the following terms and derive the equations with respect to half wave Rectifier.
   i) Ripple Factor ii) PIV iii) Rectifier Efficiency iv) % Regulation
9. Draw the circuit diagram of a Full wave Rectifier with Capacitor filter, explain its operation with necessary equations.
10. Derive the expression for diode current in a PN junction diode

Hall Ticket No. | | | | | | | | | | | **Question Paper Code: A2401**

CMR COLLEGE OF ENGINERRING & TECHNOLOGY

(AUTONOMOUS)

B.Tech (ECE)-III SEMESTERI MID EXAMINATION AUGUST - 2016

Subject: Electronic Devices & Circuits Date& Time: 10/07/2016 & 10:00 to 11.20Am Max Marks: 20

PART A

Answer all the following questions. (5 x 1 = 05)

6. Discuss the effect of temperature on PN junction diode.
7. Define the Drift and Diffusion current.
8. Draw the block diagram of Regulated power supply.
9. Draw the circuit diagram of Bridge Rectifier.
10. Discuss about Avalanche breakdown.

PART B

Answer any three of the following questions. (3 x 5 = 15)

6. What do you understand by depletion region at P-N junction? What is the effect of forward and reverse biasing of P-N junction on the depletion region? Explain with necessary diagrams.
7. i) Which type of diode capacitance is utilized in Varactor diode operation? Explain its principle of operation.
   ii) Obtain the Transition capacitance of the junction diode at reverse bias voltage of 12V if the transition capacitance is 15PF at the reverse voltage of 8V.
8. With neat sketches and necessary waveforms explain the regulation characteristics of Zener diode.
9. A Full wave rectifier uses two silicon diodes of forward resistances 20Ω each. A DC voltmeter connected across the load of 1 KΩ reads 55.4V calculate
   $i)$ I_{rms} ii) Average voltage across each diode iii) Ripple factor iv) Transformer secondary rating.
10. i) Discuss about the Avalanche breakdown and Zener breakdown mechanism.
    iii) Explain the necessity of a bleeder resistor in L-section filter used with FWR.

Hall Ticket No. | | | | | | | | | | | **Question Paper Code: A2401**

CMR COLLEGE OF ENGINERRING & TECHNOLOGY

(AUTONOMOUS)

B.Tech (ECE)-III SEMESTER II MID EXAMINATION, OCTOBER -2016

Subject: Electronic Devices & Circuits Date &Time: 26/10/2016 & 10:00 to 11.20Am Max Marks: 20

PART A

Answer all the following questions. (5 x 1 = 05)

1. Define α, β and γ of a transistor and show that how they are related to each other.
2. What is the need for biasing? List of the different types of transistor biasing methods.
3. Sketch the transfer curve defined by I_{DSS} = 12mA and V_P= -6V.
4. Define the JFET parameters and derive the relationship among them.
5. Draw the circuit symbols of the following
   (i) N-channel JFET
   (ii) P- channel JFET
   (iii) N-channel Enhancement MOSFET
   (iv) P-channel Depletion MOSFET.

PART B

Answer any three of the following questions. (3 x 5 = 15)

1. (a) Draw the circuit diagram of NPN transistor in Common Emitter (CE) configuration. With neat sketches and necessary equations, describe its static input-output characteristics and clearly indicate the cut-off, saturation & active regions on the output characteristics?
   (b) Calculate the values of I_C and I_E for a transistor with α_{dc} = 0.99 and I_{CBO} = 5μA, if I_B is measured as 20 μA.
2. Explain the construction & operation of a N-channel MOSFET in enhancement and depletion modes with the help of static drain characteristics and transfer characteristics?
3. (a) What is 'Thermal Runaway' in transistors? Derive the condition to prevent 'Thermal Runaway' in Bipolar Junction Transistors.
   (b) Design a collector to base bias circuit using silicon transistor to achieve a stability factor of 20, with the following specifications: V_{CC} = 16V, V_{BE} = 0.7V, V_{CEQ} = 8V, I_{CQ} = 4 mA & β= 50.
4. (a) With the help of neat sketches and characteristic curves explain the construction & operation of a JFET and mark the regions of operation on the characteristics?
   b) Show that in Field Effect Transistor, the transconductance, $g_m = g_{mo}[1- V_{GS}/ Vp]$
5. (a) Explain the basic construction and working of UJT. Draw its equivalent circuit.
   (b) Explain the operation of UJT as relaxation oscillator and derive the frequency of oscillation with necessary waveforms.

Hall Ticket No. | | | | | | | | | | | **Question Paper Code: A2401**

CMR COLLEGE OF ENGINERRING & TECHNOLOGY

(AUTONOMOUS)

B.Tech (ECE)-III SEMESTER II MID EXAMINATION, OCTOBER -2016

Subject: Electronic Devices & Circuits Date &Time: 26/10/2016 & 10:00 to 11.20Am Max Marks: 20

PART A

Answer all the following questions. (5 x 1 = 05)

1. Compare the merits & demerits of a Bipolar Junction Transistor (BJT) with Field effect Transistor (FET) in detail?
2. With reference to a BJT, define the following terms:
   i) Emitter efficiency.
   ii) Base transportation factor.
   iii) Large signal current gain.
3. Define the stability factors S, S^1 and S^{11}.
4. Draw the UJT circuit symbol and equivalent circuit.
5. Explain the operation of JFET as voltage variable resistor.

PART B

Answer any three of the following questions. (3 x 5 = 15)

1. Draw the circuit diagram of NPN transistor in Common Base (CB) configuration. With neat sketches and necessary equations, describe its static input- output characteristics and clearly indicate the cut-off, saturation & active regions on the output characteristics?
2. Draw the basic circuit and small-signal model of Common Drain FET amplifier. Derive expressions for voltage gain and output resistance?
3. Explain the construction & operation of P -channel MOSFET in enhancement and depletion modes with the help of static drain characteristics and transfer characteristics?
4. (a) What is bias compensation? Explain diode compensation techniques for V_{BE} and I_{CO} variations.
   (b) Design a collector to base circuit to have operating point of (10V, 4mA). The circuit is supplied with 20V and uses a silicon transistor of h_{fe}=250.
5. (a) Explain the analysis of CE amplifier using simplified h-parameter model. Derive expressions for A_V, A_I, R_i & R_0.
6. (b) Draw the hybrid equivalent circuits for CB, CE and CC configurations.

ASSIGNMENT QUESTIONS

CMR COLLEGE OF ENGINEERING & TECHNOLOGY

(AUTONOMOUS)

B.TECH III Semester- ASSIGNMENT-1 QUESTIONS PAPER September – 2017

(Regulation: CMRCET-R15)

Subject Name:EDC

Answer all five questions **5x1=5Marks**

1. Derive the expression for total diode current interms of applied voltage.

2. With neat energy band diagrams, explain the V-I characteristics of Tunnel diode. Also discuss the negative resistance property of Tunnel diode.

3. A) With neat sketches explain HWR and derive the expression for $I_{dc,}$ $V_{dc,}$ Efficiency, Ripple factor and PIV.

   b) A voltage of 200Coswt is applied to HWR with load resistance of 5KOhms. Find the maximum Dc current component, Rms current, Ripple factor & Efficiency.

4 a) Draw the circuit diagram for a FWR with capacitor filter and derive the expression for Ripple factor.

b) What is the ripple factor if a power supply of 220 V, 50 Hz is to be Full Wave rectified and filtered with a 220μF capacitor before delivering to a resistive load of 120Ω? Compute the value of the capacitor for the ripple factor to be less than 15%.

5. Discuss about the current components in a BJT.

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B.Tech (ECE)-III SEMESTERI Assignment Test, AUGUST -2016

Subject: Electronic Devices & Circuits **Max Marks: 05**

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1. Explain the operation of silicon PN junction diode, and obtain the forward and reverse bias V-I characteristics.
2. Sketch V-I characteristics of a PN diode for the following conditions:
   i) $R_f = 0, V\gamma = 0, R_r = \infty$
   ii) $R_f = 0, V\gamma = 0.6V, R_r = \infty$
   iii) R_f = Non-zero, fixed value, $V\gamma = 0, R_r = \infty$
   iv) R_f = Non-zero, fixed value, $V\gamma = 0.6V, R_r = \infty$
   Where $V\gamma$ is the cut-in voltage, R_f is the forward dynamic resistance & R_r is the reverse dynamic resistance of the diode.
3. I) Discuss the Avalanche breakdown and Zener breakdown mechanism in detail.
   ii) With neat sketches and necessary waveforms explain about the regulation characteristics of Zener diode.
4. Draw the block diagram of Regulated power supply and derive the expression for Ripple factor, DC output voltage and Efficiency of FWR.
5. A 230 V, 60Hz voltage is applied to the primary of a 5:1 step down, center tapped transformer used in a full wave rectifier having a load of 900Ω .If the diode resistance and the secondary coil resistance together has a resistance of 100Ω, determine
   i) dc voltage across the load. ii) dc current flowing through the load.
   iii) dc power delivered to the load. iv) PIV across each diode.

CMR COLLEGE OF ENGINERRING & TECHNOLOGY

(AUTONOMOUS)

B.Tech (ECE)-III SEMESTERI Assignment Test, AUGUST -2016

Subject: Electronic Devices & Circuits **Max Marks: 05**

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1. (a) Explain the operation of transistor as an amplifier with an example.
   (b) What are the BJT limits of operation?
2. (a) What is stabilization?
   (b) Draw the BJT fixed bias circuit and derive the expression for stability factor S.
3. How to obtain quiescent point graphically for a given transistor amplifier of CE configuration.
4. What the different FET biasing techniques explain any one.
5. Draw the basic circuit and small-signal model of Common Gate FET amplifier. Derive expressions for voltage gain and output resistance?

TEACHING NOTES

UNIT I

Contents:

1. Semiconductor Materials
2. PN Junction Diode
3. V-I Characteristics of Diode
4. Diode Current Equation
5. Transition and Diffusion Capacitances
6. Tunnel Diode
7. Varactor Diode
8. SCR Characteristics
9. Semiconductor Photo Diode

UNIT-I

INSULATOR:

An insulator is a material that offers a very low level of conductivity under Pressure from an applied voltage source. In this material Forbidden energy gap is large (E_G 6e.V).So, electron can not acquire enough energy and hence conduction is not possible. Ex: Diamond is a perfect insulator.

SEMI CONDUCTOR:

A semiconductor is a material that has a conductivity level somewhere in between the extremes of an insulator and a conductor. Energy gap is only about 1ev. Ex: Germanium, Silicon (Energy gap of Germanium is about 0.785 eV and for silicon it is 1.21 eV).

CONDUCTOR:

Conductor is a material that will support a generous flow of charge when a voltage source of limited magnitude is applied across its terminals. There is no energy gap in conductors. Conduction band and valence band are overlapped. Ex: Copper, Aluminium.

DOPING:

Adding impurities in a semiconductor is called Doping.

Pure semiconductor is called intrinsic semiconductor. Semiconductor with impurities added are called extrinsic semiconductor.

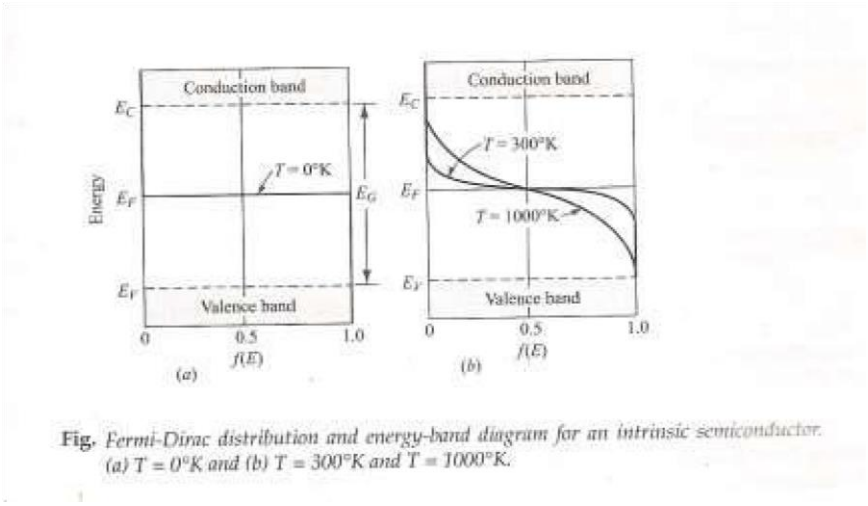


Fig. *Fermi-Dirac distribution and energy-band diagram for an intrinsic semiconductor. (a) T = 0°K and (b) T = 300°K and T = 1000°K.*

EXTRINSIC MATERIALS

The characteristics of semiconductor materials can be altered significantly by the addition of certain impurity atoms into the relatively pure semiconductor material. These impurities, although only added to perhaps 1 part in 10 million, can alter the band structure sufficiently to totally change the electrical properties of the material. A semiconductor material that has been subjected to the doping process is called an extrinsic material. There are two extrinsic materials of immeasurable importance to semiconductor device fabrication: *n*-type and *p*- type.

n-Type Material

Both the *n*- and *p*-type materials are formed by adding a predetermined number of impurity atoms into a germanium or silicon base. The *n*-type is created by introducing those impurity elements that have *five* valence electrons (*pentavalent*), such as *antimony, arsenic,* and *phosphorus.* The effect of such impurity elements is indicated in

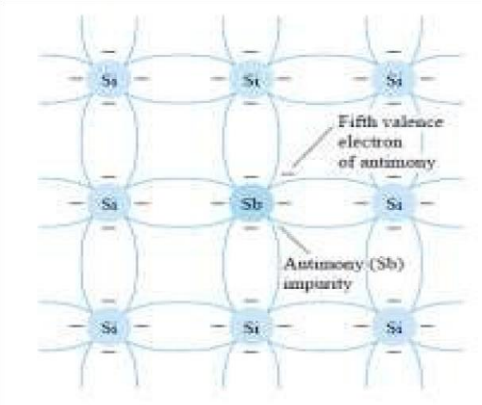


Figure.1 Antimony impurity in n-type material

Note that the four covalent bonds are still present. There is, however, an additional fifth electron due to the impurity atom, which is *un associated* with any particular covalent bond.

Diffused impurities with five valence electrons are called donor atoms**.** The effect of this doping process on the relative conductivity can best be described through the use of the energy-band diagram of Fig. 1.1.

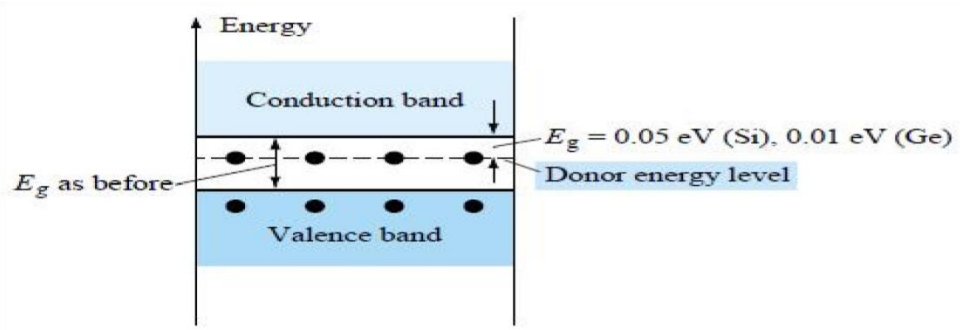
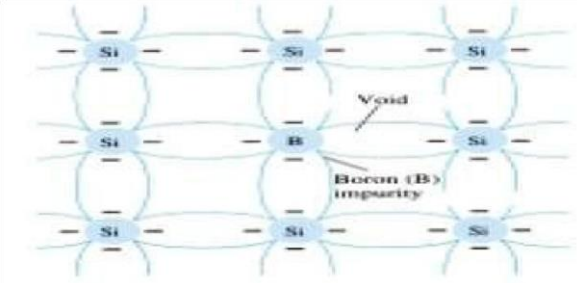


Figure 1.1 Effect of donor impurities on the energy band structure.

p-Type Material

The *p*-type material is formed by doping a pure germanium or silicon crystal with impurity atoms having *three* valence electrons. The elements most frequently used for this purpose are *boron*, *gallium*, and *indium.* The effect of one of these elements, boron, on a base of silicon is indicated in Fig. 1.2.



Note that there is now an insufficient number of electrons to complete the covalent bonds of the newly formed lattice. The resulting vacancy is called a *hole* and is represented by a small circle or positive sign due to the absence of a negative charge. Since the resulting vacancy will readily *accept* a ―free‖ electron: The diffused impurities with three valence electrons are called acceptor atoms.

Majority and Minority Carriers

In the intrinsic state, the number of free electrons in Ge or Si is due only to those few electrons in the valence bands that have acquired sufficient energy from thermal or light sources to break the covalent bond or to the few impurities that could not be removed. The vacancies left behind in the covalent bonding structure represent our very limited supply of holes. In an *n*-type material the number of holes has not changed significantly from this intrinsic level. The net result, therefore, is that the number of electrons far outweighs the number of holes. For this reason:
In an n-type material (Fig. 1.13a) the electron is called the majority carrier and the hole the minority carrier.

For the *p*-type material the number of holes far outweighs the number of electrons, as shown in Fig. 1.13b. Therefore: In a p-type material the hole is the majority carrier and the electron is the minority carrier. When the fifth electron of a donor atom leaves the parent atom, the atom remaining acquires a net positive charge: hence the positive sign in the donor-ion representation. For similar reasons, the negative sign Appears in the Acceptor ion.

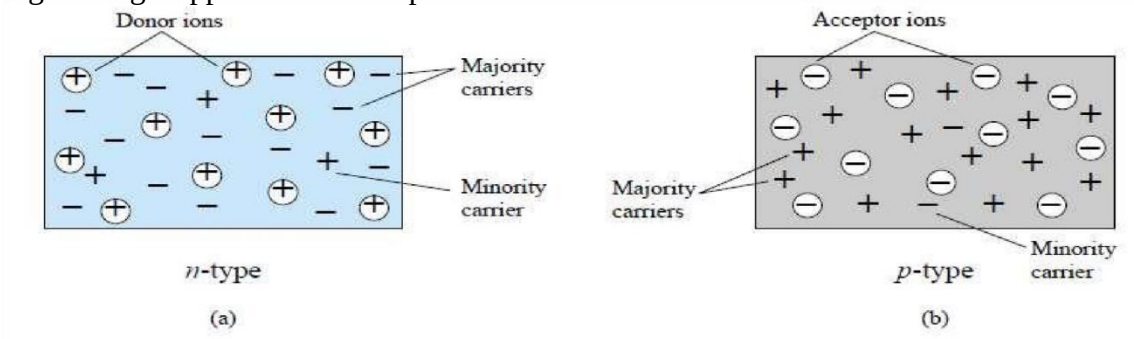


Figure 1.13(a) *n* type material; (b) *p*-type material.

Fermi Level in N & P- type materials is shown in below Fig:

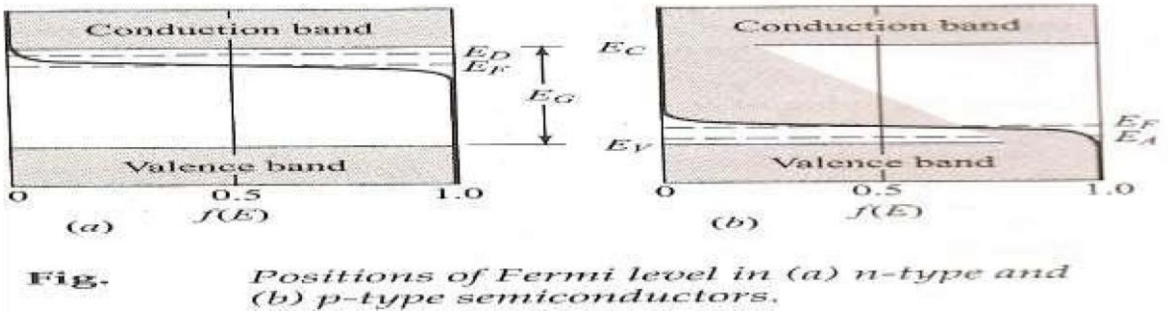


Fig. *Positions of Fermi level in (a) n-type and (b) p-type semiconductors.*

In N type material Fermi level is just below the conduction band. In P type material Fermi level is just above the valence band.

PN diode characteristics in forward bias and reverse bias regions:

The semiconductor diode is formed by simply bringing these materials together (constructed from the same base—Ge or Si), as shown in Fig. 1.14. At the instant the two materials are ―joined‖ the electrons and holes in the region of the junction will combine, resulting in a lack of carriers in the region near the junction. This region of uncovered positive and negative ions is called the depletion region due to the depletion of carriers in this region. Since the diode is a two-terminal device, the application of a voltage across its terminals leaves three possibilities: *nobias* (V_D= 0 V), *forward bias* (V_D>0 V), and *reverse bias* (V_D<0 V)

Under no-bias (no applied voltage) conditions, any minority carriers (holes) in the *n*-type material that find themselves within the depletion region will pass directly into the *p*-type material. The closer the minority carrier is to the junction, the greater the attraction for the layer of negative ions and the less the opposition of the positive ions in the depletion region of the *n*-type material. For the purposes of future discussions we shall assume that all the minority carriers of the *n*-type material that find themselves in the depletion region due to their random motion will pass directly into the *p*type material. Similar discussion can be applied to the minority carriers (electrons) of the *p*-type material. This carrier flow has been indicated in Fig. 1.14 for the minority carriers of each material. The majority carriers (electrons) of the *n*-type material must overcome the attractive forces of the layer of positive ions in the *n*-type material and the shield of negative ions in the *p*-type material to migrate into the area beyond the depletion region of the *p*-type material. However, the number of majority carriers is so large in the *n*-type material that there will invariably be a small number of majority carriers with sufficient kinetic energy to pass through the depletion region into the *p*-type material. Again, the same type of discussion can be applied to the majority carriers (holes) of the *p*type material. The resulting flow due to the majority carriers is also shown in Fig. 1.14. In the absence of an applied bias voltage, the net flow of charge in any one direction for a semiconductor diode is zero. The symbol for a diode is repeated in Fig. 1.15 with the associated *n*- and *p*-type regions. Note that the arrow is associated with the *p*-type component and the bar with the *n*-type region. As indicated, for V_D= 0 V, the current in any direction is 0 mA.

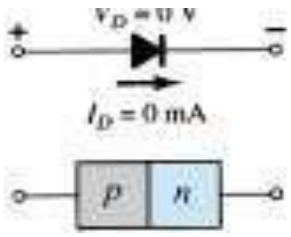


Figure 1.15 No-bias conditions for a semiconductor diode.

Reverse-Bias Condition (V_D < 0 V)

If an external potential of *V* volts is applied across the *p-n* junction such that the positive terminal is connected to the *n*-type material and the negative terminal is connected to the *p*-type material as shown in Fig. 1.16, the number of uncovered positive ions in the depletion region of the *n* type material will increase due to the large number of ―free‖ electrons drawn to the positive potential of the applied voltage. For similar reasons, the number of uncovered negative ions will increase in the *p*-type material. The net effect, therefore, is a widening of the depletion region. This widening of the depletion region will establish too great a barrier for the majority carriers to overcome, effectively reducing the majority carrier flow to zero as shown in Fig. 1.16.

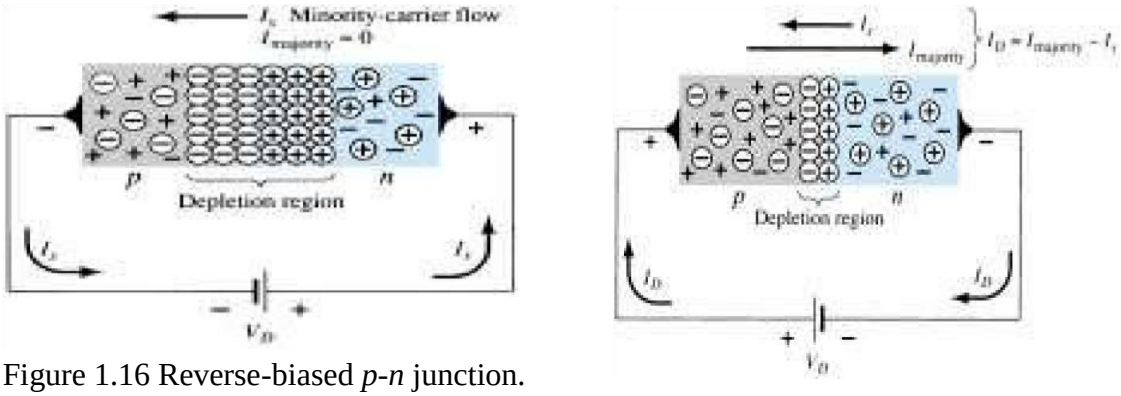
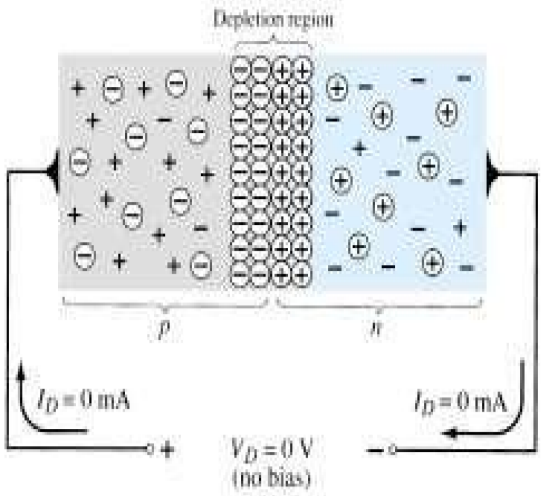


Figure 1.16 Reverse-biased *p-n* junction.

The number of minority carriers, however, that find themselves entering the depletion region will not change, resulting in minority-carrier flow vectors of the same magnitude indicated in Fig. 1.14 with no applied voltage the current that exists under reverse-bias conditions is called the reverse saturation current and is represented by I_o.

Forward-Bias Condition (V_D> 0 V)

A *forward-bias* or ―on‖ condition is established by applying the positive potential to the *p*-type material and the negative potential to the *n*-type material as shown in Fig. 1.18. A semiconductor diode is forward-biased when the association p-type and positive and n-type and negative has been established.



The application of a forward-bias potential V_D will ―pressure‖ electrons in the *n*-type material and holes in the *p*-type material to recombine with the ions near the boundary and reduce the width of the depletion region as shown in Fig. 1.18. The resulting minority-carrier flow of electrons from the *p*type material to the *n*-type material (and of holes from the *n*-type material to the *p*-type material) has not changed in magnitude (since the conduction level is controlled primarily by the limited number of impurities in the material), but the reduction in the width of the depletion region has resulted in a heavy majority flow across the junction. An electron of the *n*-type material now sees a reduced barrier at the junction due to the reduced depletion region and a strong attraction for the positive potential applied to the *p*-type material. As the applied bias increases in magnitude the depletion region will continue to decrease in width until a flood of electrons can pass through the junction, resulting in an exponential rise in current as shown in the forward-bias region of the characteristics of Fig. 1.19. Note that the vertical scale of Fig. 1.19 is measured in milli amperes and the horizontal scale in the forward-bias region has a maximum of 1 V. Typically, therefore, the voltage across a forward biased diode will be less than 1 V.

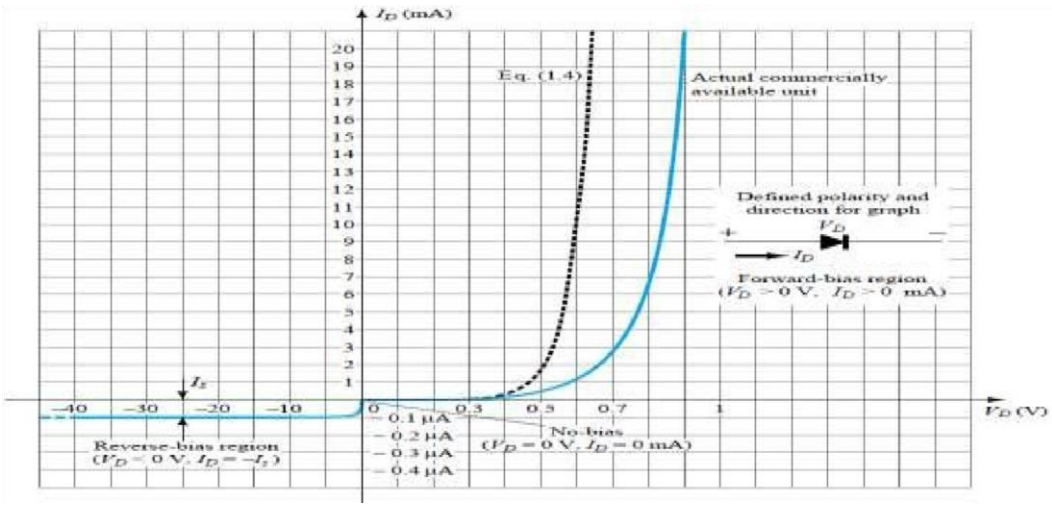


Figure 1.19 Silicon semiconductor diode characteristics.

Equation for diode junction current:

$$i_D = I_o(e^{v_D/\eta V_T} - 1) \quad \text{A}$$

where $V_T = kT/q$; V

V_D_ diode terminal voltage, Volts

Io _ temperature-dependent saturation current, µA T _ absolute temperature of p-n junction, K

k _ Boltzmann's constant 1.38x 10 $^{-23}$J/K) q _ electron charge 1.6x10^{-19} C

η = empirical constant, 1 for Ge and 2 for Si

Temperature Effects

Temperature can have a marked effect on the characteristics of a silicon semiconductor diode as shown in Fig. 1.24. It has been found experimentally that the reverse saturation current I_o will just about double in magnitude for every 10°C increase in temperature.

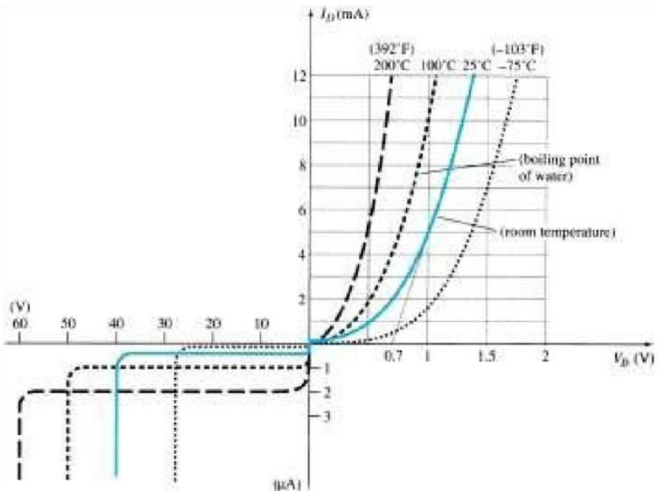


Figure 1.24 Variation in diode characteristics with temperature change.

It is not uncommon for a germanium diode with an I_o in the order of 1 or 2 A at 25°C to have a leakage current of 100 A _ 0.1 mA at a temperature of 100°C. Typical values of I_o for silicon are much lower than that of germanium for similar power and current levels. The result is that even at high temperatures the levels of I_o for silicon diodes do not reach the same high levels obtained for germanium—a very important reason that silicon devices enjoy a significantly higher level of development and utilization in design. Fundamentally, the open-circuit equivalent in the reverse bias region is better realized at any temperature with silicon than with germanium. The increasing levels of I_o with temperature account for the lower levels of threshold voltage, as shown in Fig. 1.24. Simply increase the level of I_o in and not rise in diode current. Of course, the level of *TK* also will be increase, but the increasing level of I_o will overpower the smaller percent change in *TK*. As the temperature increases the forward characteristics are actually becoming more ―ideal

TRANSITION AND DIFFUSION CAPACITANCE

Electronic devices are inherently sensitive to very high frequencies. Most shunt capacitive effects that can be ignored at lower frequencies because the reactance $X_C=1/2\pi fC$ is very large (open-circuit equivalent). This, however, cannot be ignored at very high frequencies. X_C will become sufficiently small due to the high value of *f* to introduce a low-reactance ―shorting‖ path. In the *p-n* semiconductor diode, there are two capacitive effects to be considered. In the reverse-bias region we have the transition- or depletion-region capacitance (C_T), while in the forward-bias region we have the diffusion (C_D) or storage capacitance. Recall that the basic equation for the capacitance of a parallel plate capacitor is defined by $C= €A/d$, where *€* is the permittivity of the dielectric (insulator) between the plates of area *A* separated by a distance *d.* In the reverse-bias region there is a depletion region (free of carriers) that behaves essentially like an insulator between the layers of opposite charge. Since the depletion width (*d*) will increase with increased reverse-bias potential, the resulting transition capacitance will decrease. The fact that the capacitance is dependent on the applied reverse-bias potential has application in a number of electronic systems. Although the effect described above will also be present in the forward-bias region, it is overshadowed by a capacitance effect directly dependent on the rate at which charge is injected into the regions just outside the depletion region. The capacitive effects described above are represented by a capacitor in parallel with the ideal diode, as shown in Fig. 1.38. For low- or mid-frequency applications (except in the power area), however, the capacitor is normally not included in the diode symbol.

A Light-Emitting-Diode (LED) display generates light energy as current is passed through the individual segments. It refers to the backlight system used in many newer LCD televisions and not the chips that produce the images.

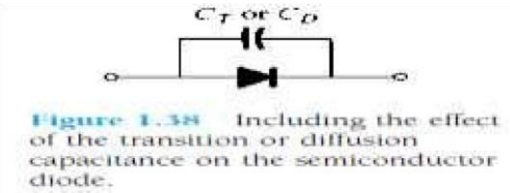


Figure 1.38 Including the effect of the transition or diffusion capacitance on the semiconductor diode.

A liquid-crystal display (LCD) controls the reflection of available light. Traditional LCD TVs are normally back lit by fluorescent bulbs.

LCD TVs and LED TVs work by blocking light. The following explains how they work-

-A solution of TN liquid crystals is inserted between two perpendicularly aligned panes of polarized glass. It is possible to manipulate the intensity of light as it passes through this crystalline matrix and out of the glass panel at the other end by twisting one of the panes wrt the other.

-Depending on the voltage of the electrical charge running through them, liquid crystals will untwist so that the intensity of light that can pass through the second polarized pane is affected.

-Fundamentally, these displays can switch between light states (where the liquid crystals are fully twisted) and dark states (where the liquid crystals are fully untwisted), or somewhere along the gray scale in between.

The following are the advantages of LEDs over LCDs

LEDs are longer lasting than fluorescent bulbs.

LEDs are more energy efficient than fluorescent bulbs.

LEDs give greater contrast and better image quality than LCDs.

LEDs refer to the term Light Emitting Diode. LEDs are heavily doped p-n junctions which work under forward bias and emit spontaneous radiation. When the p-n junction is forward biased the excess minority chargers accumulate at the junction boundary on either side. When they recombine, energy is released in the form of photons, having energy equal to or lesser than the band gap energy. The intensity of light emitted is directly proportional to the forward current.

The reverse breakdown voltage is low (around 5 V).

Laser Diodes are compact transistor-like packages with two or more electrical leads. -Inside the package is a small semiconductor chip, containing the laser cavity. The chip contains a stack of layers with different doping and compositions that provide optical and electrical confinement. Lasing occurs when stimulated emission causes the amplification of photons confined to the lasing mode. Photons bounce back and forth between the front and back mirror. Hence, a diverging beam emerges from the laser diode package. They have applications in the telecommunications industry and in testing instrumentation.

CONDUCTIVITY OF A SEMICONDUCTOR

- With each hole - electron pair created, two charges - carrying particles are formed
- One is negative (free e^-) of mobility $\boldsymbol{\mu_n}$, and the other is positive (hole) of mobility μ_p.
- The current density J is given by,

$$J=(n\,\mu_n + p\,\mu_p)\,q\,\varepsilon = \sigma\,\varepsilon\,\varepsilon$$

Where n = magnitude of free electron (negative) concentration,

p = magnitude of hole (positive) Concentration,

σ = conductivity, ε = electric field and

q = electron charge

Hence $\sigma=(n \mu_n + p \mu_p) q$

The resistivity **ρ** is inversely proportional to the conductivity and is given by,

$$\rho = 1/\sigma = 1 / (n \mu_n + p \mu_p) q$$

- For a pure (called intrinsic) semiconductor considered here,

$n = p = n_i$ Where, n_i is the intrinsic concentration

- In pure germanium at room temperature there is about one hole – electron pair for every 2×10^9 germanium atoms
- With increasing temperature, the density of hole – electron pair increases and correspondingly, the conductivity increases
- The intrinsic concentration $\mathbf{n_i}$ varies with temperature in accordance with the relationship,

$$n_i^2 = A_0 T^3 e^{-E_{GO}/KT}$$

Where A_0 = material constant

T = temperature in degree Kelvin

E_{GO} = energy gap at 0K in eV

K = Boltzmann constant in eV/K

- The conductivity of Germanium (Silicon) increases approximately 6(8) percent per degree increase in temperature
- The resistivity (reciprocal of conductivity) of a semiconductor decreases exponentially where in metals the resistivity increases almost linearly

- Semiconductor has a negative temperature coefficient of resistance where as that of a metal is positive and of much smaller magnitude
- For most metals the resistance increase about 0.4 percent /^{o}C increase in temperature
- The constants $\mathbf{E_{GO}}$, $\boldsymbol{\mu_n}$, $\boldsymbol{\mu_p}$and many other important physical quantities for Germanium and Silicon are given in Table. Note that germanium has of the order of 10^{22} atoms/cm^3, whereas at room temperature (300K), ni = 10^{13}/cm^4. Hence only 1 atom in about 10^9 contributes a free electron (and a hole) to the crystal because of broken covalent bonds. For silicon this ratio is even smaller, about 1 atom in 10^{12}

THECHARGE DENSITIES IN A SEMICONDUCTOR

- Let $\mathbf{N_D}$ equal the concentration of donor atoms, these are practically all ionized, $\mathbf{N_D}$ positive charges per cubic meter are contributed by the donor ions
- Hence the total positive charge density is $\mathbf{N_D + p}$Similarly, if $\mathbf{N_A}$is the concentration of acceptor ions, these contribute $\mathbf{N_A}$ negative charges per cubic meter
- The total negative charge density is $\mathbf{N_A + n}$
- Since the semiconductor is electrically neutral, the magnitude of the positive charge density must equal that of the negative concentration, or

$$N_D + p = N_A + n \quad \text{---------- (1)}$$

- Consider an n – type material having $N_A = 0$. Since the number of electrons is much greater than the number of holes in an n – type semiconductor (n >> p) then equation (1) reduces to

$$n \simeq N_D \text{ or } \quad n_n \simeq N_D$$

- In a n – type material the free electron concentration n_n is approximately equal to the density of donor atoms
- The concentration $\mathbf{p_n}$of holes in the n – type semiconductor is obtained from, $n_n p_n = n_i^2$

Thus, $p_n = n_i^2 / N_D$

$$n_p p_p = n_i^2 \quad ; \quad p_p \simeq N_A \quad n_p = n_i^2 / N_A$$

- Similarly, for a p - type semiconductor
- According to the law of mass action, the product of the number of electrons in the conduction band and the number of holes in the valence band must be constant

#1. Consider an n – type silicon in which dopant concentration is $10^{17}/cm^3$. Find electron and hole concentration at 350 K, (intrinsic carrier concentration at 350 K is $4.18 \times 10^{11}/cm^3$).

SOLUTION: Electron concentration n = dopant concentration = $10^{17}/cm^3$& hole concentration

$$p = \frac{n_i^2}{n}$$

$$= \frac{(4.18 \times 10^{11})^2}{10^{17}} = 1.747 \times 10^6/cm^3$$

#2. A silicon bar is doped with 10^{17} arsenic atoms/ cm^3. What is the equilibrium hole concentration at 300 K? Where is the Fermi level (E_F) of sample located relative to intrinsic Fermi level (E_i)? ($n_i = 1.5 \times 10^{10}/cm^3$)

SOLUTION: Electron n = $N_D = 10^{17}/cm^3$

Hole concentration $p = \frac{n_i^2}{n}$

$$= \frac{1.5 \times 10^{10}}{10^{17}} = \frac{2.25 \times 10^{20}}{10^{17}} = 2.25 \times 10^3/cm^3$$

For n – type material $N_D = n_i e^{-(E_{Fi} - E_F)/KT}$

$$\Rightarrow 10^{17} = 1.5 \times 10^{10}\, e^{-(E_{Fi} - E_F)/KT}$$

$$\Rightarrow \frac{E_F - E_{Fi}}{KT} = 15.7$$

$$\Rightarrow E_F - E_{Fi} = \frac{15.7 \times 1.38 \times 10^{-23} \times 300}{1.6 \times 10^{-19}}$$

$$= 0.4 \text{ eV}$$

So Fermi level move up by 0.4 eV relative to intrinsic Fermi level

- The Conductivity associated with the conduction electrons could be written in the form, $\sigma_n = n\, \mu_n\, q$
  Where μ_n = mobility of the electrons

  q = electron charge

  Similarly for hole conduction,

  $\sigma_p = p\, \mu_p\, q$
  Where μ_p = mobility of holes

- The current density associated with the drift of the electrons due to the applied field would be given by, $J_n = n\, \mu_n\, q\varepsilon$

Similarly, $J_p = p\ \mu_p\ q\varepsilon$

- However, an electron current may flow in a semiconductor even in the absence of an electric field, i.e., if there exists a gradient of the electron density
- Consequently, one deals in semiconductors frequently with two kinds of current: a drift current (due to the electric field) and diffusion current (due to a gradient of the carrier concentration).
- These concepts apply, of course, to electrons as well as to holes
- The diffusion current density for electrons is $\mathbf{J_n = q\ D_n \frac{dn}{dx}}$ D_n = Diffusion constant of the electrons in m^2/sec
- Similarly, diffusion current density for holes is $\mathbf{J_p = \_\ q\ D_p \frac{dp}{dx}}$

  D_p = diffusion constant of the holes in m^2/sec
- The hole current in any point **x** may be written as the sum of two contributions, one from the field and one from the diffusion process: $\mathbf{J_p = p\ \mu_p\ q\varepsilon - q\ \frac{D_p}{dx}\ dp}$
- Similarly, the total electron current density:

$$\mathbf{J_n = n\ \mu_n\ q\varepsilon + q\ \frac{D_n}{dx}\ dn}$$

- There exists an important relationship between the diffusion coefficient and the mobility of the carriers, which is known as the Einstein relation

For holes, $D_p = (kT/q)\ \mu_p$

For electrons, $D_n = (kT/q)\ \mu_n$

Hence, the diffusion constant is proportional to the mobility,

$$\mathbf{\frac{Dp}{\mu_p} = \frac{Dn}{\mu_n} = V_T}$$

Where $V_T = kT/q = T/11{,}600$

#3. Find the resistivity of (a) intrinsic silicon (b) p – type silicon with $N_A = 10^{16}/cm^3$. Use $n_i = 1.5 \times 10^{10}/cm^3$ and assume for intrinsic silicon μ_n = 1350 cm^2/ V-S and μ_p = 480 cm^2/ V-S and for doped silicon μ_n = 1110 cm^2/ V-S and μ_p = 400 cm^2/ V-S.

SOLUTION:

(a) For intrinsic silicon resistivity $\rho = \frac{1}{q\ (\mu_n\ n + \mu_p p)}$

For intrinsic silicon $n = p = n_i$;

$\Longrightarrow \rho = \frac{1}{qn_i(\mu_n + \mu_p)}$

$$= \frac{1}{1.6 \times 10^{-19} \times 1.5 \times 10^{10}(1350 + 480)}$$

$= 2.28 \times 10^5$ohm-cm.

(b) For doped silicon $\rho = \frac{1}{q\,(\mu_n\, n + \mu_p\, p)}$

Hole concentration $p = N_A = 10^{16}/cm^3$

Electron concentration $n = \frac{n_i^2}{p} = \frac{(1.5 \times 10^{10})^2}{10^{16}}$

$$= 2.25 \times 10^4/cm^3$$

$$\therefore \rho = \frac{1}{1.6 \times 10^{-19}(2.25 \times 10^4 \times 1110 + 10^{16} \times 400)}$$

$$= 1.56 \text{ ohm} - \text{cm}.$$

#4. Find the ratio of maximum resistivity to intrinsic resistivity (e_{max}/e_i)

Intrinsic conductivity $\sigma i = q\, n_i\, (\mu_n + \mu_p)$

Extrinsic conductivity $\sigma i = q\, (n\mu_n + P\mu_p)$

$$= q\left[n\,\mu_n + \frac{n_i^2}{n}\,\mu_p\right]$$

For maximum resistivity σ should be minimum

$\therefore \frac{d\sigma}{dn} = 0$: $n = \sqrt[ni]{\frac{\mu_p}{\mu_n}}$ And $P = \sqrt[ni]{\frac{\mu_p}{\mu_n}}$

$\sigma_{min} = q\sqrt{\mu_n\mu_p} + q\,ni\sqrt{\mu_n\mu}$ $p = 2\,q\,ni\sqrt{\mu_n\mu_p}$

ni

$$\therefore \frac{e_{max}}{e} = \frac{\mu_n + \mu_p}{\sqrt[2]{\mu_n + \mu_p}}$$

THECURRENTCOMPONENTS IN A P-N DIODE:

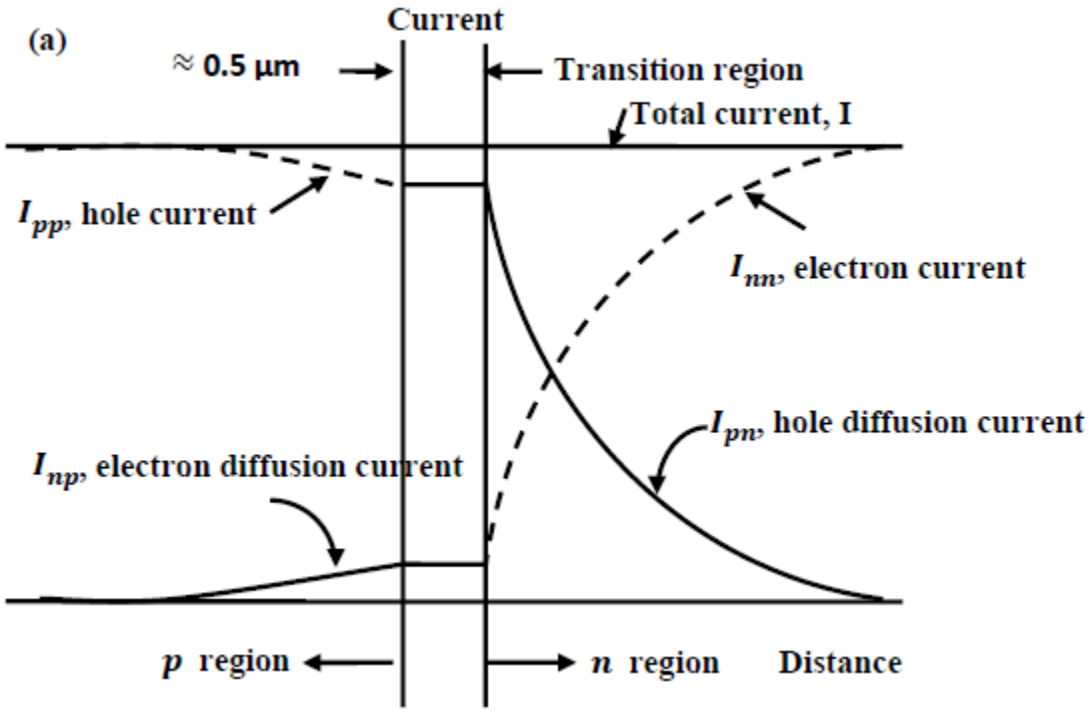


Fig - 3(a): The hole and electron-current components vs, distance in a p-n junction diode. It is assumed that no recombination takes place in the very narrow depletion region.

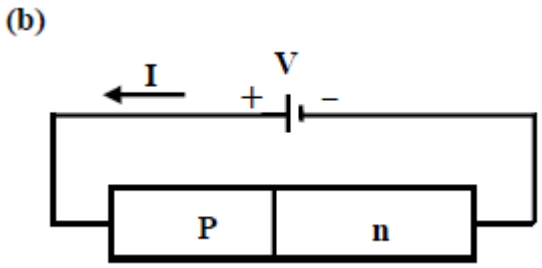


Fig -3(b) p-n junction diode in forward bias

When a forward bias is applied to a diode, holes are injected into the n-side and electrons into the p side

- The number of these injected minority carriers falls off exponentially with distance from the junction as shown in fig.(3)(a)

- The symbol **$I_{pn}(x)$** represents the hole current in the n material, and **$I_{np}(x)$** indicates the electron current in the p-side as a function of **x**

- Electrons crossing the junction at **x = 0** from right to left constitute a current in the same direction as holes crossing the junction from left to right
  Hence the total current **I** at **x = 0** is $\mathbf{I = I_{pn}(0) + I_{np}(0)}$

- Consequently, in the p-side, there must be a second component of current $\mathbf{I_{pp}}$ which, when added to $\mathbf{I_{np}}$, gives the total current **I.** Hence this hole current in the p-side I_{pp}(a majority carrier current) is given by $\mathbf{I_{pp(x)} = I - I_{np(x)}}$

- This current is plotted as a function of distance as shown in fig.(3) as is also the corresponding electron current **Inn** in the n material

- For an un symmetrically doped diode, Ipn ≠ Inp

- Current in a **p-n** diode is bipolar in character since it is made up of both positive and negative carriers of electricity

- The total current is constant throughout the device, but the proportion due to holes and that due to electrons varies with distance.

-

QUANTITATIVETHEORY OF THE PN DIODE CURRENTS:

If the forward bias is applied to the diode, holes are injected from the **p** side into the **n** material. The concentration $\mathbf{p_n}$of holes in the n-side is increased above its thermal equilibrium value $\mathbf{p_{no}}$and, is

–x/L p

given by $\mathbf{p_n(x) = p_{no} + p_n(0)e}$ …… (6)

Where the parameter $\mathbf{L_p}$is called the diffusion length for holes in the **n** material

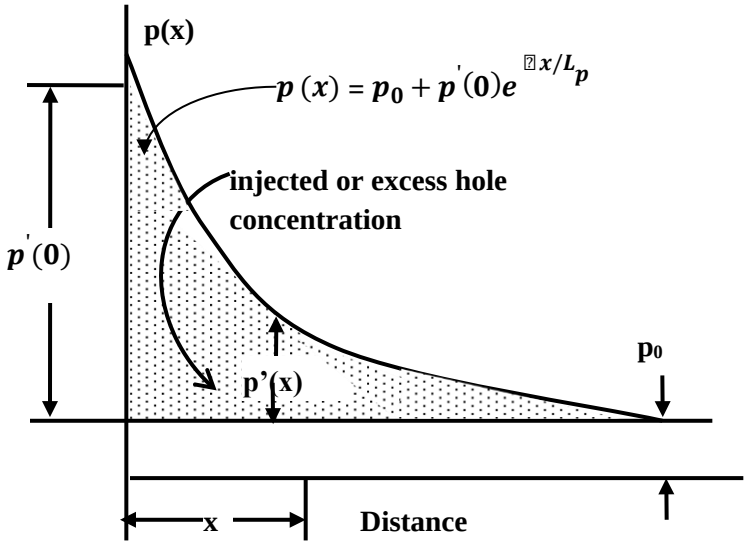


Fig – 4: The hole concentration p(x) in n _ side as a function of distance x from the junction.

The injected or excess concentration at **x = 0** is $p_n(0) = p_n(0) - p_{no}$ The diffusion hole current in the n-side is given by

$$I_{pn} = -qAD_p \frac{dp_n}{dx} \quad \text{..... (7)}$$

Taking the derivative of equation (6) and substituting in equation (7) we obtain

$$I_{pn}(x) = \frac{AqD_p p_n(0)}{L_p} e^{-\frac{x}{L_p}} \quad \text{..... (8)}$$

This equation verifies that the hole current decreases exponentially with distance.

THE LAW OF THE JUNCTION

- If the barrier potential across the depletion layer is V_B, then $p_p = p_n e^{V_B/V_T}$ ..... (9)

This is the Boltzmann relationship of kinetic gas theory

- If we apply above equation to the case of an open-circuited p-n junction, then $p_P = p_{po}$, $p_n = p_{n0}$ **and** $V_B = V_0$
- Consider now a junction biased in the forward direction by an applied voltage **V**

- Then the barrier voltage $\mathbf{V_B}$ is decreased from its equilibrium value $\mathbf{V_0}$ by the amount **V,**

$V_B = V_0 - V$

Where, V_0 = equilibrium value

At the edge of the depletion layer, $\mathbf{x = 0, p_n = p_n(0),}$ then the above equation (9) is

$$p_0 = p_n(0)e^{(V_0 - V)/V_T} \quad \ldots\ldots\ (10)$$

Combining this equation with the above said equation (5), i.e., $p_{p0}=p_{n0}\ e^{V_0/V_T}$ we obtain

$$\boxed{p_n(0)=p_{n0}e^{V/V_T}} \qquad \ldots\ldots\ (11)$$

This boundary condition is called the "law of the junction". It indicates that, for a forward bias **(V > 0)**, the hole concentration $\mathbf{p_n(0)}$ at the junction is greater than the thermal-equilibrium value $\mathbf{p}_{n0}$.

A similar equation, valid for electrons, is obtained by interchanging **p** and **n** in above equation (11).

The hole concentration $\mathbf{p_n(0)}$ injected into the **n** side at the junction is given by,

$$p_n(0)=p_{n0}(e^{V/V_T}-1) \qquad \ldots\ldots\ (12)$$

THE FORWARD CURRENTS:

- The hole current $\mathbf{I_{pn}(0)}$ crossing the junction into the n-side at **x = 0** is given by,

$$I_{pn}(0) = \frac{AqD_p p_{no}}{L_p}(e^{V/V_T}-1)$$

- The electron current $\mathbf{I_{np}(0)}$ crossing the junction into the p-side is obtained from above equation by

$$I_{np}(0) = \frac{AqD_n n_{po}}{L_n}(e^{V/V_T}-1)$$

interchanging **n** and **p,** or $\mathbf{I_{np}}$

The total diode current **I** is the sum of $\mathbf{I_{pn}(0)}$ and $\mathbf{I_{np}(0)}$, or $\mathbf{I = I_0\left(e^{V/V_T} - 1\right)}$

Where $\mathbf{I_0 = \frac{AqD_p p_{n0}}{L_p} + \frac{AqD_n n_{p0}}{L_n}}$

Hence $\mathbf{I_0}$ is called the "reverse saturation current" and depends on doping concentration

$$I_0 = Aq\left[\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right] n_i^2 \text{ Where } n_i^2 = A_0 T^3 e^{-E_{GO}/KT}$$

In other form, $I_0 = Aqn_i^2 V_T\left[\frac{\mu_p}{L_p N_D} + \frac{\mu_n}{L_n N_A}\right]$

From Einstein equation, $D_p/\mu_p = D_n/\mu_n = V_T$

$$I_0 = Aq^2 n_i^2 V_T \mu_n \mu_p\left[\frac{1}{L_p \sigma_n} + \frac{1}{L_n \sigma_p}\right]$$

Where, $\sigma_n = N_D \mu_n q$ and $\sigma_p = N_A \mu_p q$

$\mathbf{E_{GO}}$ is a voltage which is numerically equal to the forbidden gap energy in electron volts. If we consider the recombination of carriers, then the total current **I, I = $\mathbf{I_0}$ e** $\mathbf{^{(V/\eta V_T)} - 1}$ **…….. (13)**

Where, $\eta \approx 2$ for small (rated) currents and $\eta \approx 1$ for large currents

- $\mathbf{I_0}$depends on material and it is fixed for a given device. But varies with temperature,

$$\mathbf{I_{02} = I_{01} \times 2^{(T2 - T1)/10}} \quad \text{……. (14)}$$

- Where $\mathbf{I_{01}(I_{02})}$ is the reverse saturation current at a temperature $\mathbf{T_1(T_2)}$
- $\mathbf{I_0}$ doubles for every **10°C** rise in temperature. That is, it increases 7%/°C.
- $\mathbf{I_0}$ is in the range of microamperes for a germanium diode and nano amperes for a silicon diode.
- Since**η= 2** for small currents in silicon, the current increases as $e^{V/2V_T}$for the first several tenths of a volt and increases as e^{V/V_T} only at higher voltages

UNIT – II

Contents:

1. **The PN junction as a Rectifier**
2. **Half wave Rectifier**
3. **Full wave Rectifier**
4. **Bridge Rectifier**
5. **Filters**
6. **Voltage regulation using Zener Diode**

UNIT II
RECTIFIERS & FILTERS:

2.0 INTRODUCTION

For the operation of most of the electronics devices and circuits, a d.c. source is required. So it is advantageous to convert domestic a.c. supply into d.c. voltages. The process of converting a.c. voltage into d.c. voltage is called as rectification. This is achieved with i) Step-down Transformer, ii) Rectifier, iii) Filter and iv) Voltage regulator circuits.

These elements constitute d.c. regulated power supply shown in the fig 1 below.

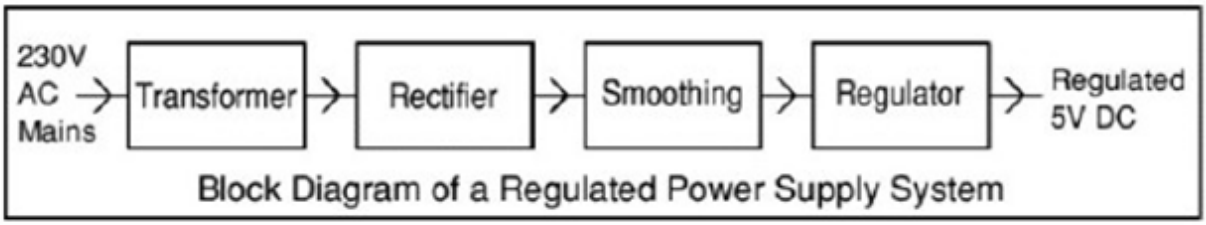


fig1 . Block diagram of Regulated D.C. Power Supply

- Transformer – steps down 230V AC mains to low voltage AC.
- Rectifier – converts AC to DC, but the DC output is varying.
- Smoothing – smooth the DC from varying greatly to a small ripple.
- Regulator – eliminates ripple by setting DC output to a fixed voltage.

The block diagram of a regulated D.C. power supply consists of step-down transformer, rectifier, filter, voltage regulator and load. An ideal regulated power supply is an electronics circuit designed to provide a predetermined d.c. voltage Vo which is independent of the load current and variations in the input voltage ad temperature. If the output of a regulator circuit is a AC voltage then it is termed as voltage stabilizer, whereas if the output is a DC voltage then it is termed as voltage regulator.

2.1 RECTIFIER:

Any electrical device which offers a low resistance to the current in one direction but a high resistance to the current in the opposite direction is called rectifier. Such a device is capable of converting a sinusoidal input waveform, whose average value is zero, into a unidirectional Waveform, with a non-zero average component. A rectifier is a device, which converts a.c. voltage (bi-directional) to pulsating d.c. voltage (Unidirectional).

Characteristics of a Rectifier Circuit:

Any electrical device which offers a low resistance to the current in one direction but a high resistance to the current in the opposite direction is called rectifier. Such a device is capable of converting a sinusoidal input waveform, whose average value is zero, into a unidirectional waveform, with a non-zero average component.

A rectifier is a device, which converts a.c. voltage (bi-directional) to pulsating d.c..Load currents: They are two types of output current. They are average or d.c. current and RMS currents.

Average or DC current: The average current of a periodic function is defined as the area of one cycle of the curve divided by the base.

It is expressed mathematically as

i. Average value/dc value/mean value= $\frac{Area\ over\ one\ period}{Total\ time\ period}$

$$V_{dc} = \frac{1}{T}\int_0^T V d(wt)$$

ii) Effective (or) R.M.S current:

The effective (or) R.M.S. current squared ofa periodic function of time is given by the area of one cycle of the curve, which represents the square of the function divided by the base.

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T V^2 d(wt)}$$

iii) Peak factor:

It is the ratio of peak value to Rms value

$$\text{Peak factor} = \frac{peakvalue}{rmsvalue}$$

iv) Form factor:

It is the ratio of Rms value to average value

$$\text{Form factor} = \frac{Rmsvalue}{averagevalue}$$

v) Ripple Factor (Γ): It is defined as ration of R.M.S. value of a.c. component to the d.c. component in the output is known as "Ripple Factor".

$$\Gamma = \frac{V_{ac}}{V_{dc}}$$

$$V_{ac} = \sqrt{V_{rms}^2 - V_{dc}^2}$$

vi) Efficiency (η):

It is the ratio of d.c output power to the a.c. input power. It signifies, how efficiently the rectifier circuit converts a.c. power into d.c. power.

$$\eta = \frac{o/p\ power}{i/p\ power}$$

vii) Peak Inverse Voltage (PIV):

It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction.

viii) Transformer Utilization Factor (TUF):

The d.c. power to be delivered to the load in a rectifier circuit decides the rating of the Transformer used in the circuit. So, transformer utilization factor is defined as

$$TUF = \frac{P_{dc}}{p_{ac(rated)}}$$

ix) % Regulation:

The variation of the d.c. output voltage as a function of d.c. load current is called regulation. The percentage regulation is defined as

$$\%\,\mathrm{Re}\,gulation = \frac{V_{NL} - V_{FL}}{V_{FL}} * 100$$

For an ideal power supply, % Regulation is zero.

2.2 CLASSIFICATION OF RECTIFIERS:

Using one or more diodes in the circuit, following rectifier circuits can be designed.

1) Half - Wave Rectifier
2) Full – Wave Rectifier
3) Bridge Rectifier

2.2.1) HALF-WAVE RECTIFIER:

A Half – wave rectifier as shown in **fig 2** is one, which converts a.c. voltage into a pulsating voltage using only one half cycle of the applied a.c. voltage.

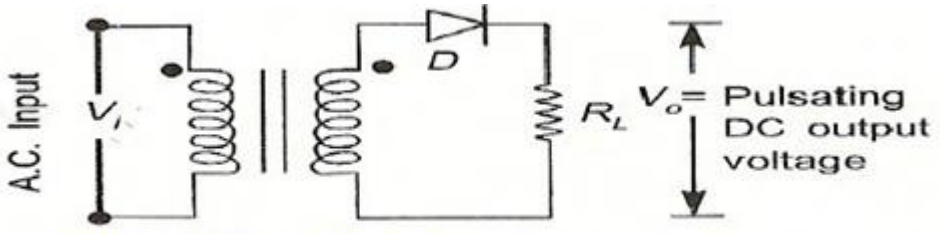


fig 2 Basic structure of Half-Wave Rectifier

The a.c. voltage is applied to the rectifier circuit using step-down transformer-rectifying element i.e., p-n junction diode and the source of a.c. voltage, all connected is series. The a.c. voltage is applied to the rectifier circuit using step-down transformer

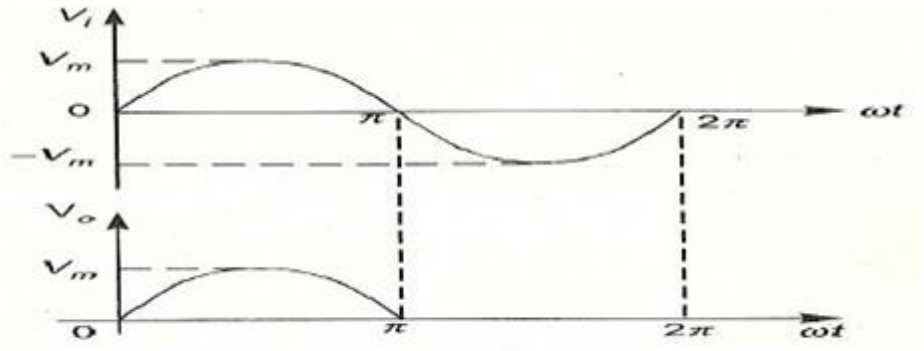


fig 3 Input and output waveforms of a Half wave rectifier

$V=V_m \sin(wt)$

The input to the rectifier circuit, Where V_m is the peak value of secondary a.c. voltage.

Operation:

For the positive half-cycle of input a.c. voltage, the diode D is forward biased and hence it conducts. Now a current flows in the circuit and there is a voltage drop across RL. The waveform of the diode current (or) load current is shown in **fig 3**.

For the negative half-cycle of input, the diode D is reverse biased and hence it does not

Conduct. Now no current flows in the circuit i.e., i=0 and Vo=0. Thus for the negative half- cycle no power is delivered to the load.

Analysis:

In the analysis of a HWR, the following parameters are to be analyzed.

1. DC output current
2. DC Output voltage
3. R.M.S. Current
4. R.M.S. voltage
5. Rectifier Efficiency (η)
6. Ripple factor (γ)
7. Peak Factor
8. % Regulation
9. Transformer Utilization Factor (TUF)
10. form factor
11. o/p frequency

Let a sinusoidal voltage Vi be applied to the input of the rectifier.
Then $V=V_m \sin(wt)$ Where V_m is the maximum value of the secondary voltage. Let the diode be idealized to piece-wise linear approximation with resistance Rf in the forward direction i.e., in the ON state and Rr (=∞) in the reverse direction i.e., in the OFF state. Now the current 'i' in the diode (or) in the load resistance RL is given by $V=V_m \sin(wt)$

i) AVERAGE VOLTAGE

$$V_{dc} = \frac{1}{T}\int_0^T V d(wt)$$

$$V_{dc} = \frac{1}{T}\int_0^{2\Pi} V(\alpha) d\alpha$$

$$V_{dc} = \frac{1}{2\Pi}\int_{\Pi}^{2\Pi} V(\alpha) d\alpha$$

$$V_{dc} = \frac{1}{2\Pi}\int_0 V_m \sin(wt)$$

$$V_{dc} = \frac{V_m}{\Pi}$$

ii).AVERAGE CURRENT:

$$I_{dc} = \frac{I_m}{\Pi}$$

iii) <u>RMS VOLTAGE</u>:

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T V^2 d(wt)}$$

$$V_{rms} = \sqrt{\frac{1}{2\Pi}\int_0^{2\Pi} (V_m sim(wt))^2 d(wt)}$$

$$V_{rms} = \frac{V_m}{2}$$

$$I_{rms} = \frac{I_m}{\Pi}$$

IV) RMS CURRENT

V) PEAK FACTOR

$$\textbf{Peak factor} = \frac{peakvalue}{rmsvalue}$$

$$\textbf{Peak Factor} = \frac{V_m}{(V_m/2)}$$

Peak Factor =2

vi) FORM FACTOR

$$\text{Form factor} = \frac{Rmsvalue}{averagevalue}$$

$$\text{Form factor} = \frac{(V_m/2)}{V_m/\Pi}$$

Form Factor =1.57

vii) Ripple Factor:

$$\Gamma = \frac{V_{ac}}{V_{dc}}$$

$$V_{ac} = \sqrt{V_{rms}^2 - V_{dc}^2}$$

$$\Gamma = \frac{\sqrt{V_{rms}^2 - V_{dc}^2}}{V_{ac}}$$

$$\Gamma = \sqrt{\frac{V_{rms}^2}{V_{dc}^2} - 1}$$

$$\Gamma = 1.21$$

viii) Efficiency (η):

$$\eta = \frac{o/ppower}{i/ppower} * 100$$

$$\eta = \frac{p_{ac}}{P_{dc}} * 100$$

$$\eta = 40.8$$

ix) Transformer Utilization Factor (TUF):

The d.c. power to be delivered to the load in a rectifier circuit decides the rating of the transformer used in the circuit. Therefore, transformer utilization factor is defined as

$$TUF = \frac{p_{dc}}{P_{ac(rated)}}$$

$$TUF = 0.286.$$

The value of TUF is low which shows that in half-wave circuit, the transformer is not fully utilized.
If the transformer rating is 1 KVA (1000VA) then the half-wave rectifier can deliver

1000 X 0.287 = 287 watts to resistance load.

x) Peak Inverse Voltage (PIV):

It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction. The peak inverse voltage across a diode is the peak of the negative half- cycle. For half-wave rectifier, PIV is Vm.

DISADVANTAGES OF HALF-WAVE RECTIFIER:

1. The ripple factor is high.
2. The efficiency is low.
3. The Transformer Utilization factor is low.

Because of all these disadvantages, the half-wave rectifier circuit is normally not used as a power rectifier circuit.

2.2.2) FULL WAVE RECTIFIER:

A full-wave rectifier converts an ac voltage into a pulsating dc voltage using both half cycles of the applied ac voltage. In order to rectify both the half cycles of ac input, two diodes are used in this circuit. The diodes feed a common load RL with the help of a center-tap transformer. A center-tap transformer is the one, which produces two sinusoidal waveforms of same magnitude and frequency but out of phase with respect to the ground in the secondary winding of the transformer. The full wave rectifier is shown in the **fig 4** below

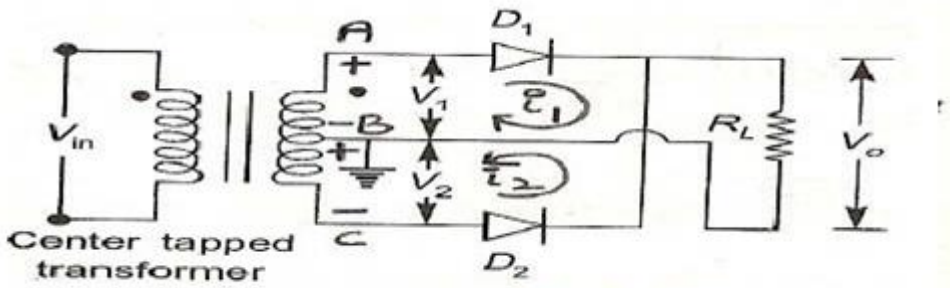


fig 4 Full-Wave Rectifier

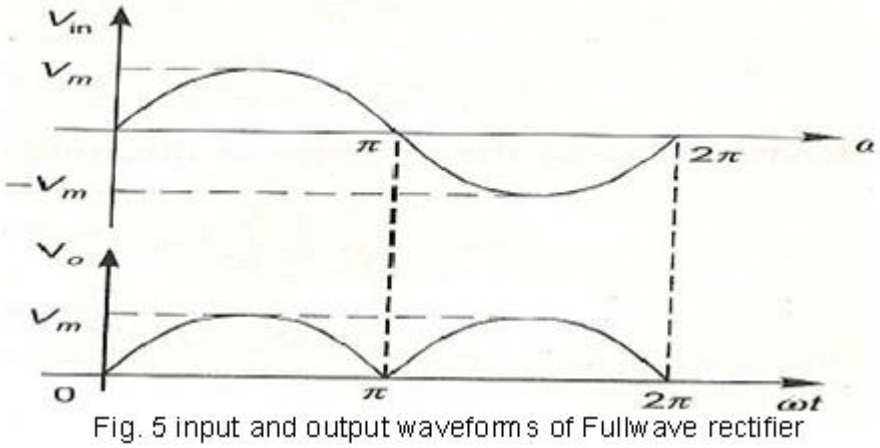


Fig. 5 input and output waveforms of Fullwave rectifier

Fig. 5 shows the input and output wave forms of the ckt.

During positive half of the input signal, anode of diode D1 becomes positive and at the same time the anode of diode D2 becomes negative. Hence D1 conducts and D2 does not conduct. The load current flows through D1 and the voltage drop across RL will be equal to the input voltage.

During the negative half cycle of the input, the anode of D1 becomes negative and the anode of D2 becomes positive. Hence, D1 does not conduct and D2 conducts. The load current flows through D2 and

the voltage drop across RL will be equal to the input voltage. It is noted that the load current flows in the both the half cycles of ac voltage and in the same direction through the load resistance.

i. **AVERAGEVOLTAGE**

$$V_{dc} = I_{dc}.R_L. = \frac{2I_m}{\pi}.R_L \quad \text{We know } I_m = \frac{V_m}{R_S + R_f + R_L}$$

$$\therefore V_{dc} = \frac{2.V_m.R_L}{\pi(R_S + R_f + R_L}$$

$$If(R_s + R_f) << R_L$$

$$V_{dc} = \frac{2V_m}{\pi} = 0.637V_m.$$

ii. **AVERAGE CURRENT**

$$\frac{1}{2\pi}\int_0^{4\pi} id\theta = \frac{1}{2\pi}\int_0^{4\pi} I_m \sin\theta dt$$

$$I_{dc} = \frac{I_m}{2\pi}\left[\int_0^{\pi} \sin\theta d\theta - \int_{\pi}^{2\pi} \sin\theta d\theta\right.$$

$$= \frac{I_m}{2\pi}[(-2)(-2)]$$

$$= \frac{I_m}{2\pi}.4 = \frac{2I_m}{\pi} = 0.637I_m.$$

$$\boxed{I_{dc} = 0.637I_m.}$$

$$\therefore I_{DC}\ FWR = 2\ I_{DC}\ HWR.$$

iii) RMS VOLTAGE:

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T V^2 d(wt)}$$

$$V_{rms} = \sqrt{\frac{1}{2\Pi}\int_0^{2\Pi} (V_m sim(wt))^2 d(wt)}$$

$$\boxed{V_{rms} = \frac{V_m}{\sqrt{2}}}$$

$$I_{rms} = \frac{2I_m}{\Pi}$$

IV) RMS CURRENT

V) PEAK FACTOR

$$\text{Peak factor} = \frac{peakvalue}{rmsvalue}$$

$$\text{Peak Factor} = \frac{V_m}{(V_m/2)}$$

Peak Factor =2

vi) FORM FACTOR

$$\text{Form factor} = \frac{Rms\ value}{average\ value}$$

$$\text{Form factor} = \frac{(V_m/\sqrt{2})}{2V_m/\Pi}$$

Form Factor =1.11

vii) Ripple Factor:

$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

for FWR,

$$I_{rms} = \frac{I_m}{\sqrt{2}} \quad \& \quad I_{DC} = \frac{2I_m}{\pi}$$

$$\therefore \gamma_{FWR} = \sqrt{\left(\frac{I_m}{\sqrt{2}} / \frac{2I_m}{\pi}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{3.1416}{2\times 1.414}\right)^2 - 1} = 0.483$$

viii) Efficiency (η):

$$\eta = \frac{o/ppower}{i/ppower} * 100$$

$$\eta = \frac{P_{dc}}{P_{ac}} \times 100\%$$

For FWR, $p_{dc} = I_{dc}^2 . R_L = \left(\frac{2}{\pi} . I_m\right)^2 . R_L$

$P_{ac} = I^2_{rms} (R_f + R_S + R_L)$

$$\left(\frac{I_m}{\sqrt{2}}\right)^2 (R_f + R_S + R_L)$$

$$\eta = \frac{\frac{I^2{}_m 4}{\pi^2} . R_L}{\frac{I^2 m^2}{2} . (R_f + R_s + R_L)}$$

$$If\ (R_f + R_S) << R_L$$

$$\eta = \frac{4}{\pi^2} . \frac{2}{1} = \frac{8}{\pi^2} = 0.812 = 81.2\%$$

ix) Transformer Utilization Factor (TUF):

The d.c. power to be delivered to the load in a rectifier circuit decides the rating of the transformer used in the circuit. So, transformer utilization factor is defined as

$$TUF = \frac{p_{dc}}{P_{ac(rated)}}$$

a) $\text{TUF (Secondary)} = \dfrac{P_{dc}\ delivered\ to\ load}{AC\ power\ rating\ of\ transformer\ secondary}$

b) Since both the windings are used $\text{TUF}_{FWR} = 2\ \text{TUF}_{HWR}$
$= 2 \times 0.287 = 0.574$

c) TUF primary = Rated efficiency = $\frac{P_{dc}}{P_{ac}} \times 100 = 81.2\%$

d) Average = $\frac{0.812 + 0.574}{2} = 0.693$

x) Peak Inverse Voltage (PIV):

It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction. The peak inverse voltage across a diode is the peak of the negative half- cycle. For half- wave rectifier, PIV is 2Vm

xi) % Regulation

$$\text{Voltage regulation} = \frac{I_{dc}(R_s + R_f)}{\frac{2V_m}{\pi} - I_{DC}(R_f + R_S)}$$

.

Advantages

1) Ripple factor = 0.482 (against 1.21 for HWR)
2) Rectification efficiency is 0.812 (against 0.405 for HWR)
3) Better TUF (secondary) is 0.574 (0.287 for HWR)
4) No core saturation problem

Disadvantages:

1. Requires centre tapped transformer.

2.2.3) BRIDGE RECTIFIER.

Another type of circuit that produces the same output waveform as the full wave rectifier circuit above, is that of the **Full Wave Bridge Rectifier**. This type of single phase rectifier uses four individual rectifying diodes connected in a closed loop "bridge" configuration to produce the desired output. The main advantage of this bridge circuit is that it does not require a special centre tapped transformer, thereby reducing its size and cost. The single secondary winding is connected to one side of the diode bridge network and the load to the other side as shown below.

The Diode Bridge Rectifier

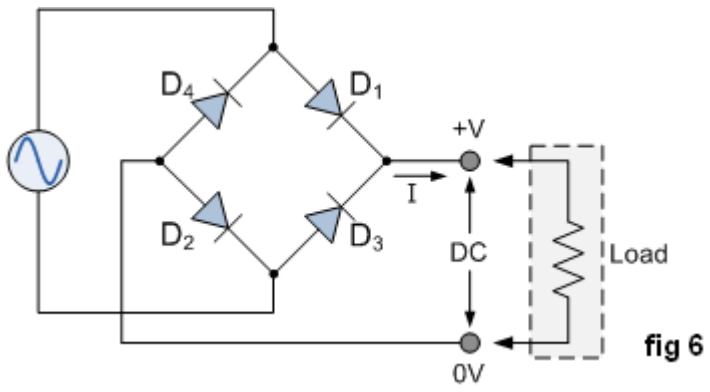
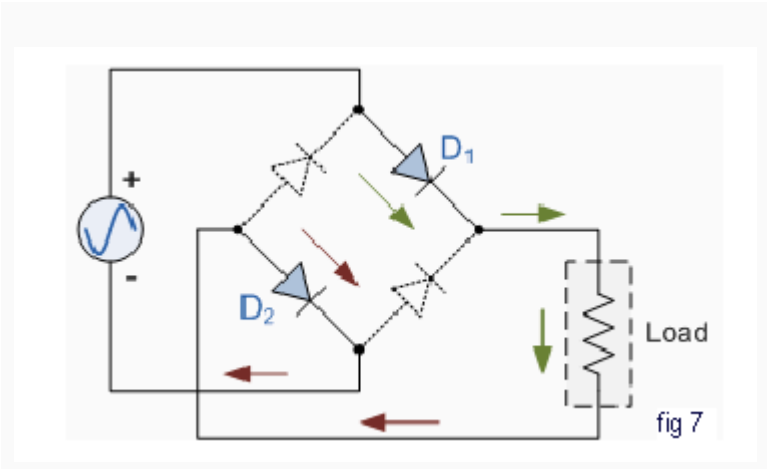


fig 6

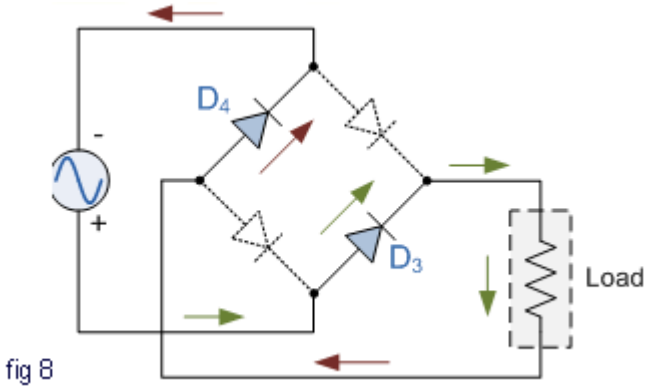
The four diodes labelled D_1 to D_4 are arranged in "series pairs" with only two diodes conducting current during each half cycle. During the positive half cycle of the supply, diodes D1 and D2 conduct in series while diodes D3 and D4 are reverse biased and the current flows through the load as shown below (fig 7).

The Positive Half-cycle



The Negative Half-cycle

During the negative half cycle of the supply, diodes D3 and D4 conduct in series (fig 8), but diodes D1 and D2 switch "OFF" as they are now reverse biased. The current flowing through the load is the same direction as before.



As the current flowing through the load is unidirectional, so the voltage developed across the load is also unidirectional the same as for the previous two diode full-wave rectifier, therefore the average DC voltage across the load is $0.637V_{max}$. However in reality, during each half cycle the current flows through two diodes instead of just one so the amplitude of the output voltage is two voltage drops (2 x 0.7 = 1.4V) less than the input V_{MAX} amplitude. The ripple frequency is now twice the supply frequency (e.g. 100Hz for a 50Hz supply)

Therefore, the following expressions are same as that of full wave rectifier.

a) Average current $I_{dc} = \frac{2I_m}{\pi}$

b) RMS current $I_{rms} = \frac{I_m}{\sqrt{2}}$

c) DC output voltage (no.load) V_{DC} $\frac{2V_m}{\pi}$

d) Ripple factor γ=0.482

e) Rectification efficiency = $\eta = 0.812$

f) DC output voltage full load.

= $V_{DCFL} = \frac{2V_m}{\pi} - I_{dc}(R_S + 2R_f)$; i.e., less by one diode loss.

TUF of both primary & secondary are 0.812 therefore TUF overall is 0.812 (better than FWR with 0.693)

Comparison:

Sl. No.	Parameter	HWR	FWR	BR
1	No. of diodes	1	2	4
2	PIV of diodes	V_m	2 V_m	V_m
3	Secondary voltage (rms)	V	V-0-V	V
4	DC output voltage at no load	$\frac{V_m}{\pi}$=0.318 V_m	$\frac{2V_m}{\pi}$=0.636 V_m	$\frac{2V_m}{\pi}$=0.636 V_m
5	Ripple factor γ	1.21	0.482	0.482
6	Ripple frequency	f	2f	2f
7	Rectification efficiency η	0.406	0.812	0.812
8	TUF	0.287	0.693	0.812

2.3 FILTERS

The output of a rectifier contains dc component as well as ac component. Filters are used to minimize the undesirable ac i.e., ripple leaving only the dc component to appear at the output.

Some important filters are:

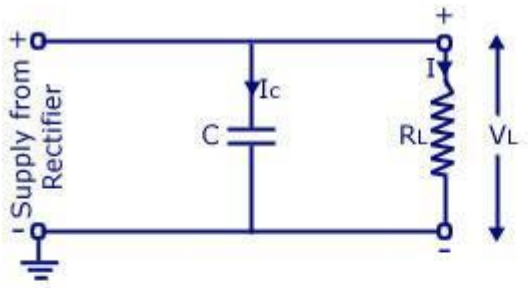
1. Inductor filter
2. Capacitor filter
3. LC or L section filter
4. CLC or Π-type filter

2.3.1 CAPACITOR FILTER

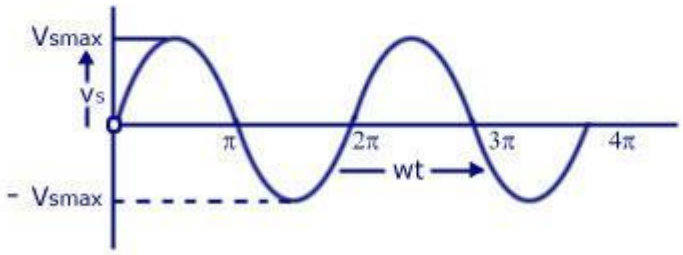
This is the most simple form of the **filter circuit** and in this arrangement a high value capacitor C is placed directly across the output terminals, as shown in figure. During the conduction period it gets charged and stores up energy to it during non-conduction period. Through this process, the time duration during which Ft is to be noted here that the capacitor C gets charged to the peak because there is no resistance (except the negligible forward resistance of diode) in the charging path. But the discharging time is quite large (roughly 100 times more than the charging time depending upon the value of RL) because it discharges through load resistance RL.

The function of the capacitor filter may be viewed in terms of impedances. The large value capacitor C offers a low impedance shunt path to the ac components or ripples but offers high impedance to the dc component. Thus ripples get bypassed through capacitor C and only dc component flows through the load resistance RL

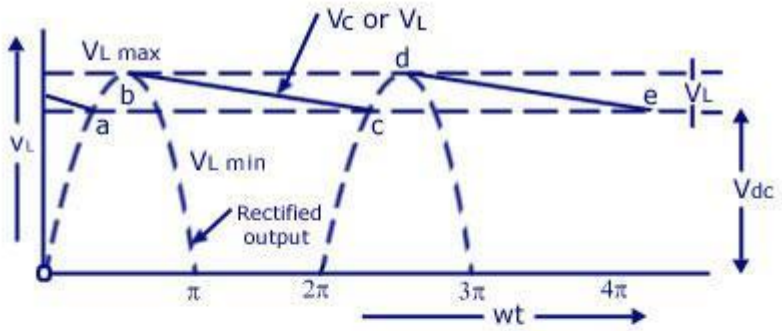
Capacitor filter is very popular because of its low cost, small size, light weight and good characteristics.



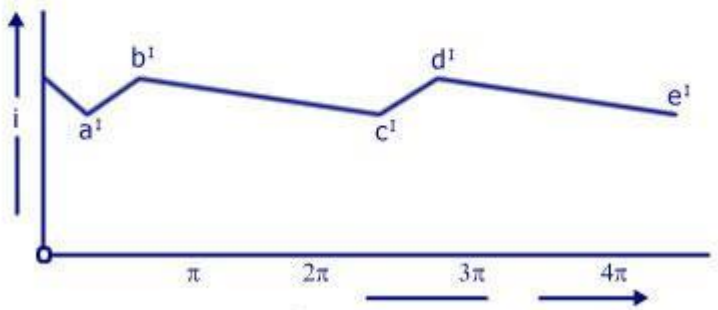
Circuit Diagram



Input voltage Waveform to Rectifier



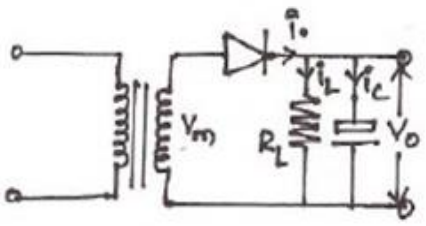
Rectified and filtered Output Voltage Waveform



Load Current Waveform
Half-wave Rectifier With Shunt Capacitor Filter

www.CircuitsToday.com

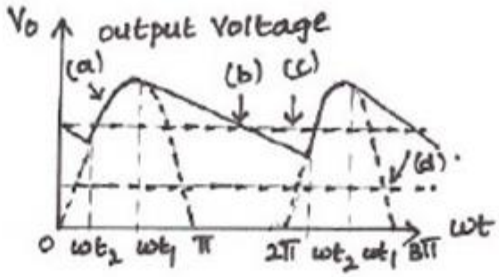
CAPACITOR FILTER WITH HWR



Cut In angle – wt_2

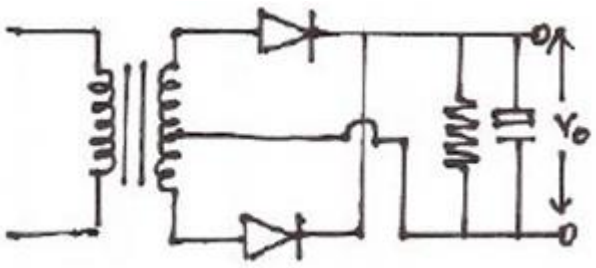
Cut out angle = Wt_1

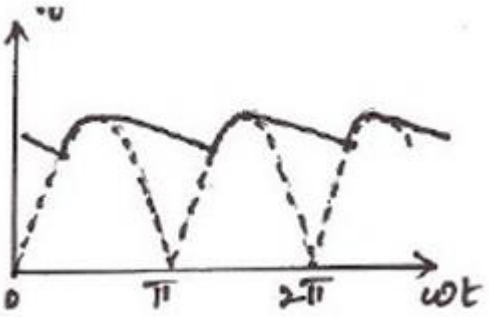
$Wt_1 = \pi - \tan^{-1} WCR_L$



(a) Capacitor charging through diode ($Wt_2 - Wt_1$)
(b) Capacitor discharging through R_L (Wt_1 to Wt_2)
(c) Average (DC) voltage with fitter
(d) Average (DC) voltage without fitter.

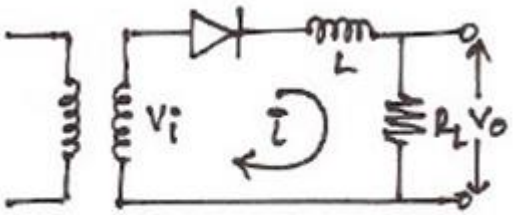
CAPACITOR FILTER WITH FWR

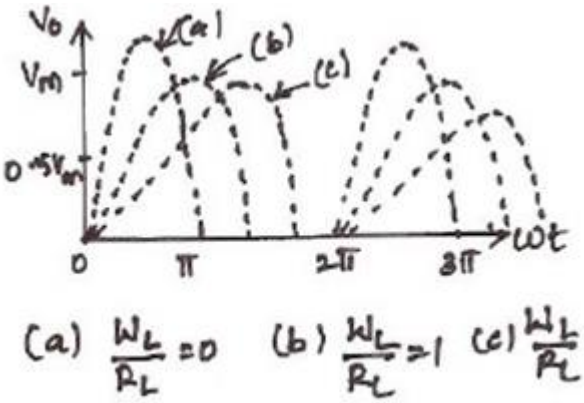




$$\text{Ripple factor } r = \frac{1}{4\sqrt{3}fCR_L}$$

Ripple freq $_{FWR}$ = 2 ripple freq $_{HWR}$.



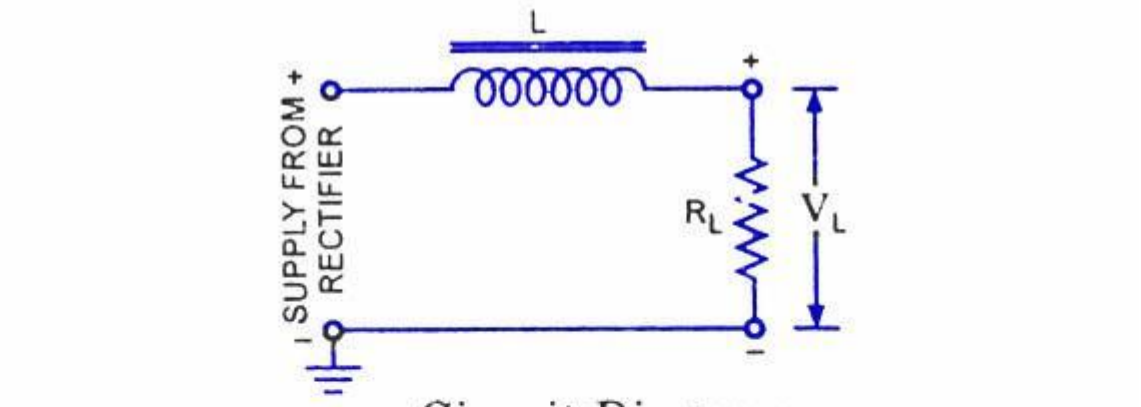


The worth noting points about shunt capacitor filter are:

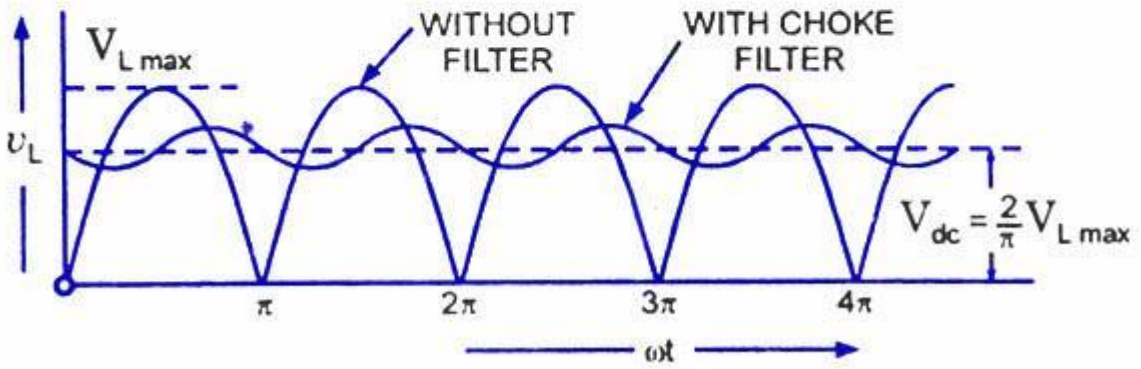
1. For a fixed-value filter capacitance larger the load resistance RL larger will be the discharge time constant CRL and therefore, lower the ripples and more the output voltage. On the other hand lower the load resistance (or more the load current), lower will be the output voltage.

2. Similarly smaller the filter capacitor, the less charge it can hold and more it will discharge. Thus the peak-to-peak value of the ripple will increase, and the average dc level will decrease. Larger the filter capacitor, the more charge it can hold and the less it will discharge. Hence the peak-to-peak value of the ripple will be less, and the average dc level will increase. But, the maximum value of the capacitance that can be employed is limited by another factor. The larger the capacitance value, the greater is the current required to charge the capacitor to a given voltage. The maximum current that can be handled by a diode is limited by the figure quoted by the manufacturer. Thus the maximum value of the capacitance that can be used in the shunt filter capacitor is limited.

2.3.2 Series Inductor Filter.



Circuit Diagram



Output Voltage Waveforms
Full-Wave Rectifier With Series Inductor Filter

In this arrangement a high value inductor or choke L is connected in series with the rectifier element and the load, as illustrated in figure. The filtering action of an inductor filter depends upon its property of opposing any change in the current flowing through it. When the output current of the rectifier increases above a certain value, energy is stored in it in the form of magnetic field and this energy is given up when the output current falls below the average value. Thus by placing a choke coil in series with the rectifier output and load, any sudden change in current that might have occurred in the circuit without an inductor is smoothed out by the presence of the inductor L.

The function of the inductor filter may be viewed in terms of impedances. The choke offers high impedance to the ac components but offers almost zero resistance to the desired dc components. Thus ripples are removed to a large extent. Nature of the output voltage without filter and with choke filter is shown in figure.

For dc (zero frequency), the choke resistance R_c in series with the load resistance R_L forms a voltage divider and dc voltage across the load is given as where V_{dc} is dc voltage output from a full-wave rectifier. Usually choke coil resistance Rc, is much small than R_L and, therefore, almost entire of the dc voltage is available across the load resistance R_L.

Since the reactance of inductor increases with the increase in frequency, better filtering of the higher harmonic components takes place, so effect of third and higher harmonic voltages can be neglected.

As obvious from equation , if choke coil resistance R_c is negligible in comparison to load resistance R_L, then the entire dc component of rectifier output is available across 2 R_L and is equal to — $V_{L\ max}$. The ac voltage partly drops across X_L and partly over R_L.

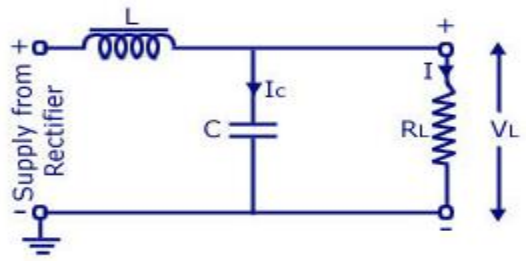
2.3.3 L-SECTION FILTER:

A simple series inductor reduces both the peak and effective values of the output current and output voltage. On the other hand a simple **shunt capacitor filter** reduces the ripple voltage but increases the diode current. The diode may get damaged due to large current and at the same time it causes greater heating of supply transformer resulting in reduced efficiency.

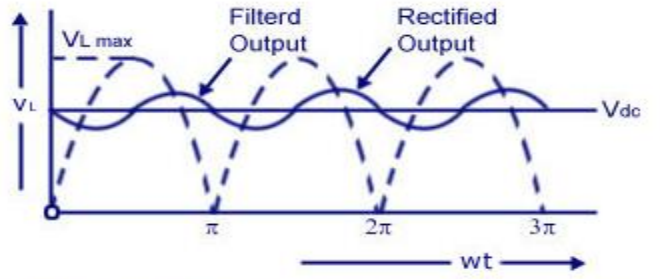
In an inductor filter, ripple factor increases with the increase in load resistance RL while in a capacitor filter it varies inversely with load resistance RL.

From economical point of view also, neither series inductor nor shunt capacitor type filters are suitable.

Practical **filter-circuits** are derived by combining the voltage stabilizing action of shunt capacitor with the current smoothing action of series choke coil. By using combination of inductor and capacitor ripple factor can be lowered, diode current can be restricted and simultaneously ripple factor can be made almost independent of load resistance (or load current). Two types of most commonly used combinations are choke-input or L-section filter-and capacitor-input or Pi-Filter.



Circuit Digram

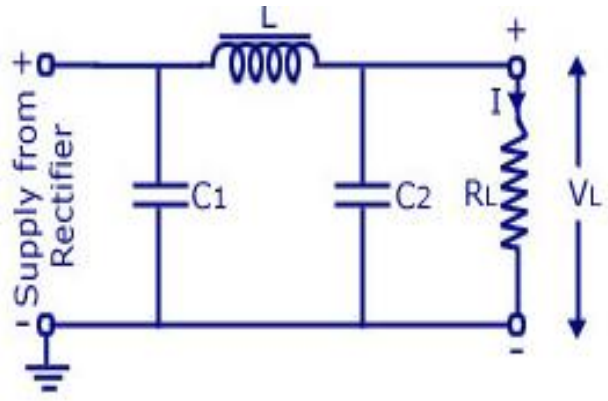


Rectified and Filtered Output Voltage Waveform
Full-wave Rectifier With Choke-Input Filter

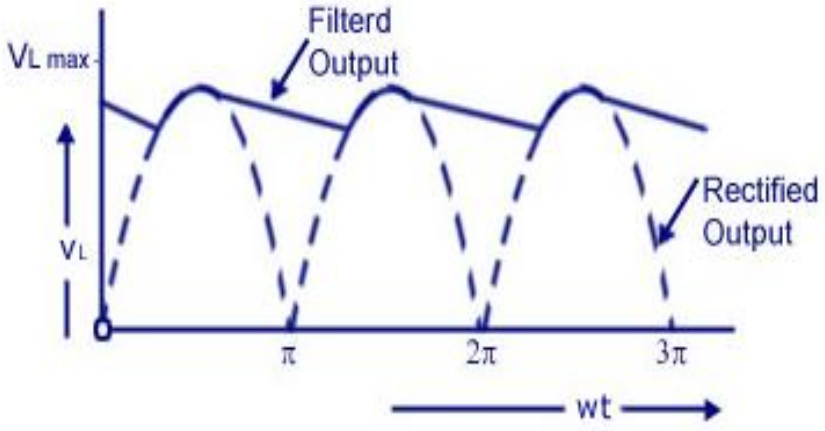
Choke-input filter is explained below:

Choke-input filter consists of a choke L connected in series with the rectifier and a capacitor C connected across the load . This is also sometimes called the L-section filter because in this arrangement inductor and capacitor are connected, as an inverted L. ln figure only one filter section is shown. But several identical sections are often employed to improve the smoothing action. (The choke L on the input side of the filter readily allows dc to pass but opposes the flow of ac components because its dc resistance is negligibly small but ac impedance is large. Any fluctuation that remains in the current even after passing through the choke are largely by-passed around the load by the shunt capacitor because Xc is much smaller than RL. Ripples can be reduced effectively by making XL greater than Xc at ripple frequency. However, a small ripple still remains in the filtered output and this is considered negligible if it than l%. The rectified and filtered output voltage waveforms from a full-wave re with choke-input filter are shown in figure.

2.3.4 II-SECTION FILTER:



Circuit Digram



Rectified and Filtered Output Voltage Waveform
Full-wave Rectifier With capacitor Input Filter

Capacitor-Input or Pi-Filter.

Such a filter consists of a shunt capacitor C1 at the input followed by an L-section filter formed by series inductor L and shunt capacitor C_2. This is also called the *n-filter* because the shape of the circuit diagram for this filter appears like Greek letter *n (pi)*. Since the rectifier feeds directly into the capacitor so it is also called *capacitor input filter.*

As the rectified output is fed directly into a capacitor C1. Such a filter can be used with a half-wave rectifier (series inductor and L-section filters cannot be used with half-wave rectifiers). Usually electrolytic capacitors are used even though their capacitances are large but they occupy minimum space. Usually both capacitors C1 and C_2 are enclosed in one metal container. The metal container serves as, the common ground for the two capacitors.

A capacitor-input or *pi*- filter is characterized by a high voltage output at low current drains. Such a filter is used, if, for a given transformer, higher voltage than that can be obtained from an L-section filter is required and if low ripple than that can be obtained from a shunt capacitor filter or L-section filter is desired. In this filter, the input capacitor C1 is selected to offer very low reactance to the ripple frequency. Hence major part of filtering is accomplished by the input capacitor *C1*. Most of the remaining ripple is removed by the L-section filter consisting of a choke L and capacitor C_2.)

The action of this filter can *best* be understood by considering the action of L-section filter, formed by L and C_2, upon the triangular output voltage wave from the input capacitor C_1 The charging and discharging action of input capacitor C1 has already been discussed. The output voltage is roughly the same as across input capacitor C1 less the dc voltage drop in inductor. The ripples contained in this output are reduced further by L-section filter. The output voltage of pi-filter falls off rapidly with the increase in load-current and, therefore, the voltage regulation with this filter is very poor.

SALIENT FEATURES OF L-SECTION AND PI-FILTERS.

1. In pi-filter the dc output voltage is much larger than that can be had from an L-section filter with the same input voltage.

2. In pi-filter ripples are less in comparison to those in shunt capacitor or L-section filter. So smaller valued choke is required in a pi-filter in comparison to that required in L-section filter.

3.In pi-filter, the capacitor is to be charged to the peak value hence the rms current in supply transformer is larger as compared in case of L-section filter.

4.Voltage regulation in case of pi-filter is very poor, as already mentioned. So n-filters are suitable for fixed loads whereas L-section filters can work satisfactorily with varying loads provided a minimum current is maintained.

5.In case of a pi-filter PIV is larger than that in case of an L-section filter.

COMPARISON OF FILTERS

1) A capacitor filter provides Vm volts at less load current. But regulation is poor.
2) An Inductor filter gives high ripple voltage for low load currents. It is used for high load currents
3) L – Section filter gives a ripple factor independent of load current. Voltage Regulation can be improved by use of bleeder resistance
4) Multiple L – Section filter or π filters give much less ripple than the single L – Section Filter.

UNIT-III

Contents:

1. **The Junction Transistor**
2. **Transistor Current Components**
3. **Transistor as an amplifier**
4. **Transistor Configurations**
5. **Limits of operation**
6. **BJT hybrid model**
7. **UJT characteristics**

UNIT III

BIPOLAR JUNCTION TRANSISTOR

3.1 INTRODUCTION

A bipolar junction transistor (BJT) is a three terminal device in which operation depends on the interaction of both majority and minority carriers and hence the name bipolar. The BJT is analogus to vacuum triode and is comparatively smaller in size. It is used i amplifier and oscillator circuits, and as a switch in digital circuits. It has wide applications in computers, satellites and other modern communication systems.

3.2 CONSTRUCTION OF BJT AND ITS SYMBOLS

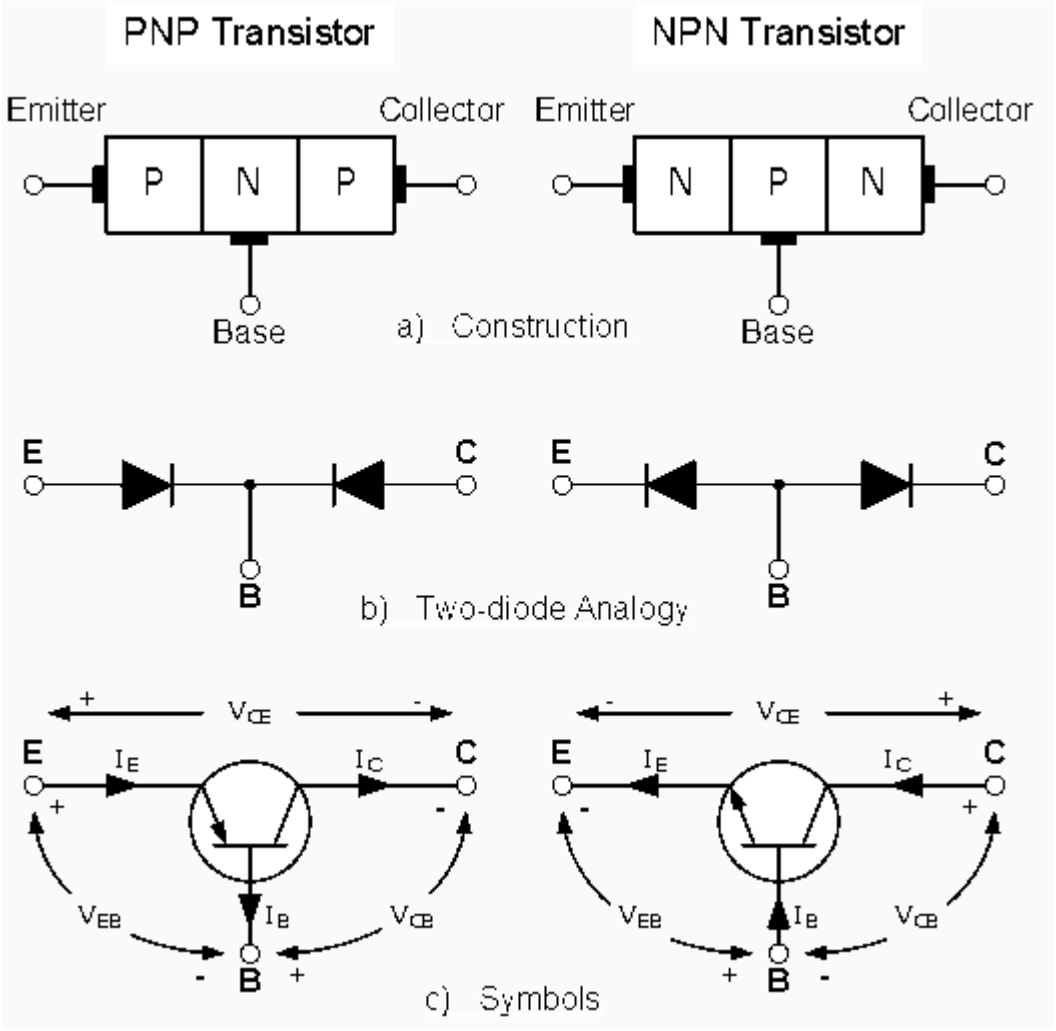
The **Bipolar Transistor** basic construction consists of two PN-junctions producing three connecting terminals with each terminal being given a name to identify it from the other two. These three terminals are known and labelled as the Emitter (E), the Base (B) and the Collector (C) respectively. There are two basic types of bipolar transistor construction, PNP and NPN, which basically describes the physical arrangement of the P-type and N-type semiconductor materials from which they are made.

Transistors are three terminal active devices made from different semiconductor materials that can act as either an insulator or a conductor by the application of a small signal voltage. The transistor's ability to change between these two states enables it to have two basic functions: "switching" (digital electronics) or "amplification" (analogue electronics). Then bipolar transistors have the ability to operate within three different regions:

- 1. Active Region - the transistor operates as an amplifier and Ic = β.Ib
- 2. Saturation - the transistor is "fully-ON" operating as a switch and Ic = I(saturation)
- 3. Cut-off - the transistor is "fully-OFF" operating as a switch and Ic = 0

Bipolar Transistors are current regulating devices that control the amount of current flowing through them in proportion to the amount of biasing voltage applied to their base terminal acting like a current-controlled switch. The principle of operation of the two transistor types PNP and NPN, is exactly the same the only difference being in their biasing and the polarity of the power supply for each type(fig 1).

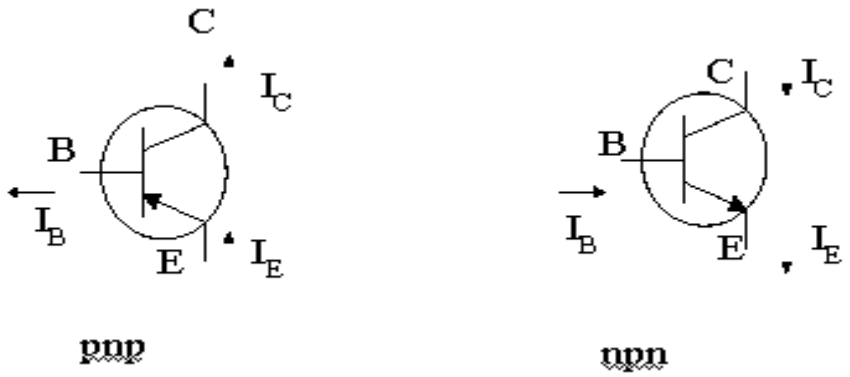
Bipolar Transistor Construction



- **Fig:1**

The construction and circuit symbols for both the PNP and NPN bipolar transistor are given above with the arrow in the circuit symbol always showing the direction of "conventional current flow" between the base terminal and its emitter terminal. The direction of the arrow always points from the positive P-type region to the negative N-type region for both transistor types, exactly the same as for the standard diode symbol.

3.3 TRANSISTOR CURRENT COMPONENTS:

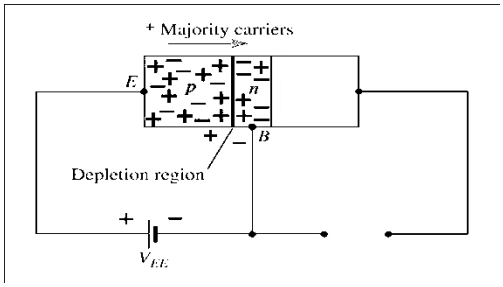


The above fig 2 shows the various current components, which flow across the forward biased emitter junction and reverse- biased collector junction. The emitter current I_E consists of hole current I_{PE} (holes crossing from emitter into base) and electron current I_{nE} (electrons crossing from base into emitter).The ratio of hole to electron currents, I_{pE} / I_{nE} , crossing the emitter junction is proportional to the ratio of the conductivity of the p material to that of the n material. In a transistor, the doping of that of the emitter is made much larger than the doping of the base. This feature ensures (in p-n-p transistor) that the emitter current consists an almost entirely of holes. Such a situation is desired since the current which result from electrons crossing the emitter junction from base to emitter does not contribute carriers, which can reach the collector.

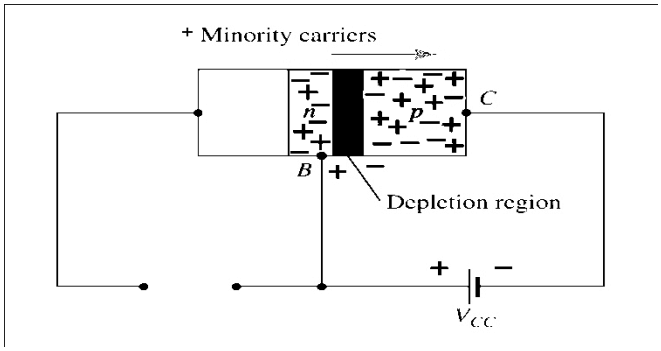
Not all the holes crossing the emitter junction J_E reach the the collector junction J_C
Because some of them combine with the electrons in n-type base. If I_{pC} is hole current at junction J_C there must be a bulk recombination current (I_{PE}- I_{pC}) leaving the base.

Actually, electrons enter the base region through the base lead to supply those charges, which have been lost by recombination with the holes injected in to the base across J_E If the emitter were open circuited so that I_E=0 then I_{pC} would be zero. Under these circumstances, the base and collector current I_C would equal the reverse saturation current I_{CO}. If $I_E \neq 0$ then
$I_C = I_{CO} - I_{pC}$
For a p-n-p transistor, I_{CO} consists of holes moving across J_C from left to right (base to collector) and electrons crossing J_C in opposite direction. Assumed referenced direction for I_{CO} i.e. from right to left, then for a p-n-p transistor, I_{CO} is negative. For an n-p-n transistor, I_{CO} is positive.The basic operation will be described using the pnp transistor. The operation of the pnp transistor is exactly the same if the roles played by the electron and hole are interchanged.

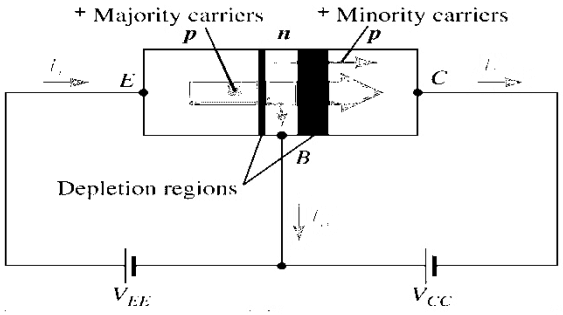
One p-n junction of a transistor is reverse-biased, whereas the other is forward-biased.



Forward-biased junction of a pnp transistor



Reverse-biased junction of a pnp transistor



Both biasing potentials have been applied to a pnp transistor and resulting majority and minority carrier flows indicated.

Majority carriers (+) will diffuse across the forward-biased p-n junction into the n-type material.

A very small number of carriers (+) will through n-type material to the base terminal. Resulting IB is typically in order of microamperes.

The large number of majority carriers will diffuse across the reverse-biased junction into the p-type material connected to the collector terminal

Applying KCL to the transistor:

$$I_E = I_C + I_B$$

The comprises of two components – the majority and minority carriers

$$I_C = I_{Cmajority} + I_{COminority}$$

I_{co} – I_c current with emitter terminal open and is called leakage current

Various parameters which relate the current components is given below

Emitter efficiency:

$$\gamma = \frac{currentofinjectedcarriersatJ_E}{totalemittercurrent}$$

$$\gamma = \frac{I_{PE}}{I_{pE} + I_{nE}} = \frac{I_{pE}}{I_{nE}}$$

Transport Factor:

$$\beta^* = \frac{injectedcarriercurrentreachingJ_C}{injectedcarrierncurrentatJ_E}$$

$$\beta^* = \frac{I_{pC}}{I_{nE}}$$

Large signal current gain:

The ratio of the negative of collector current increment to the emitter current change from zero (cut-off)to I_E the large signal current gain of a common base transistor.

$$\alpha = \frac{-(I_C - I_{CO})}{I_E}$$

Since I_C and I_E have opposite signs, then α, as defined, is always positive. Typically numerical values of α lies in the range of 0.90 to 0.995

$$\alpha = \frac{I_{pC}}{I_E} = \frac{I_{pC}}{I_{nE}} * \frac{I_{pE}}{I_E} \quad \alpha = \beta * \gamma$$

The transistor alpha is the product of the transport factor and the emitter efficiency. This statement assumes that the collector multiplication ratio α^* is unity. α^* is the ratio of total current crossing J_C to hole arriving at the junction.

3.4 Bipolar Transistor Configurations

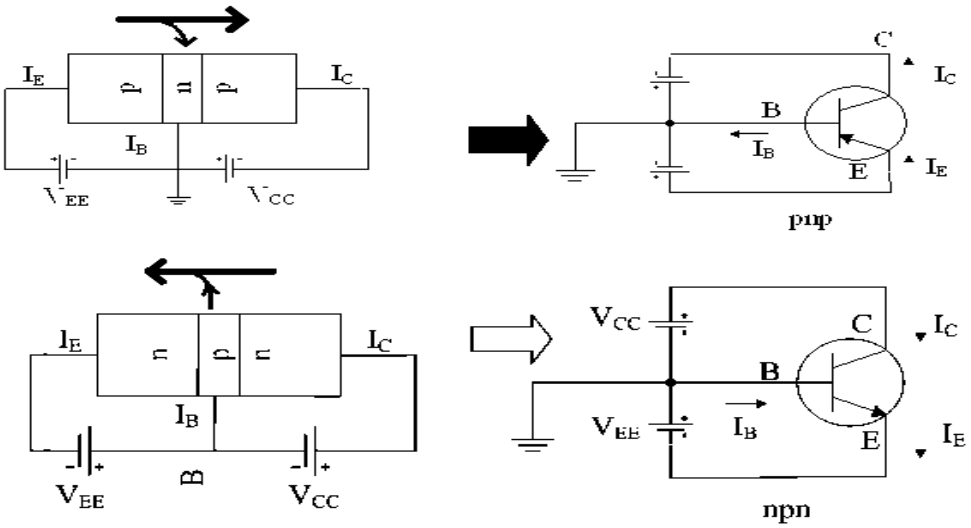
As the **Bipolar Transistor** is a three terminal device, there are basically three possible ways to connect it within an electronic circuit with one terminal being common to both the input and output. Each method of connection responding differently to its input signal within a circuit as the static characteristics of the transistor vary with each circuit arrangement.

- 1. Common Base Configuration - has Voltage Gain but no Current Gain.
- 2 Common Emitter Configuration - has both Current and Voltage Gain.
- 3. Common Collector Configuration - has Current Gain but no Voltage Gain.

3.5 COMMON-BASE CONFIGURATION

Common-base terminology is derived from the fact that the : base is common to both input and output of t configuration. base is usually the terminal closest to or at ground potential. Majority carriers can cross the reverse-biased junction because the injected majority carriers will appear as minority carriers in the n-type material. All current directions will refer to conventional (hole) flow and the arrows in all electronic symbols have a direction defined by this convention.

Note that the applied biasing (voltage sources) are such as to establish current in the direction indicated for each branch.

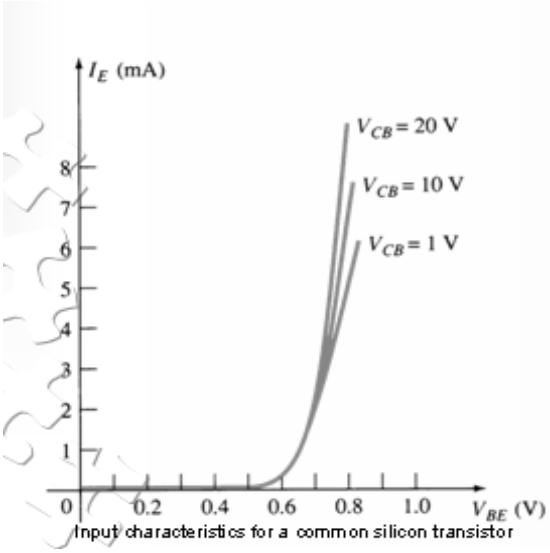


To describe the behaviour of common-base amplifiers requires two set of characteristics:

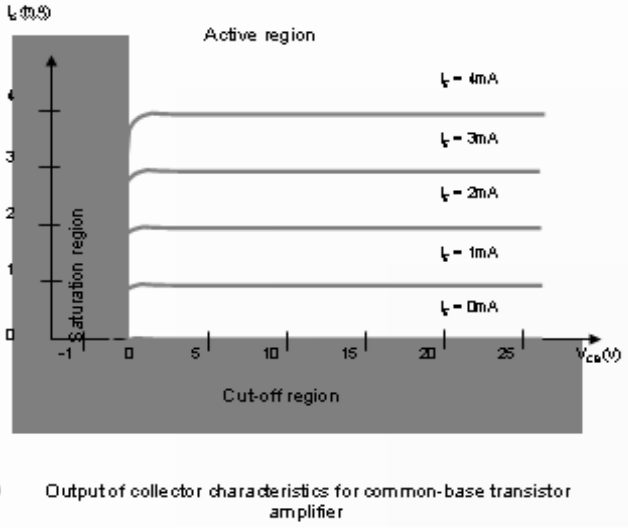
1. Input or driving point characteristics.
2. Output or collector characteristics

The output characteristics have 3 basic regions:

- Active region –defined by the biasing arrangements
- Cut off region – region where the collector current is 0A
- Saturation region- region of the characteristics to the left of $V_{CB} = 0V$



Input characteristics for a common silicon transistor



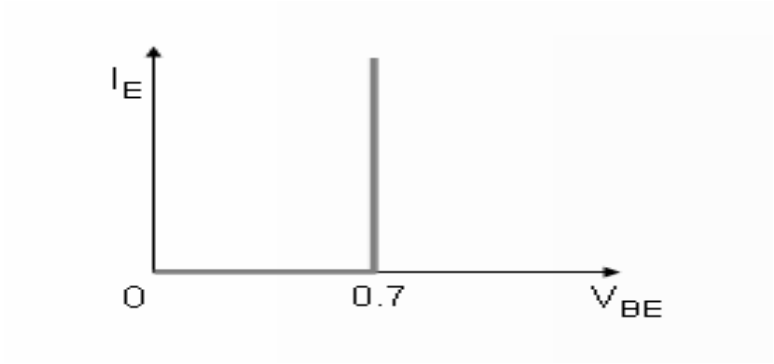
Output of collector characteristics for common-base transistor amplifier

Active region	Saturation region	Cut-off region
•I_E increased, Ic increased •BE junction forward bias and CB junction reverse bias •Refer to the graf, Ic ≈ I_E •Ic not depends on V_{CB} •Suitable region for the transistor working as amplifier	• BE and CB junction is forward bias • Small changes in V_{CB} will cause big different to Ic • The allocation for this region is to the left of V_{CB}= 0 V.	• Region below the line of I_E=0 A • BE and CB is reverse bias • no current flow at collector, only leakage current

The curves (output characteristics) clearly indicate that a first approximation to the relationship between IE and IC in the active region is given by

$I_c \approx IE$

Once a transistor is in the 'on' state, the base-emitter voltage will be assumed to beV_{BE} = 0.7V



In the dc mode the level of I_c and I_E due to the majority carriers are related by a quantity called alpha □= α_{dc}

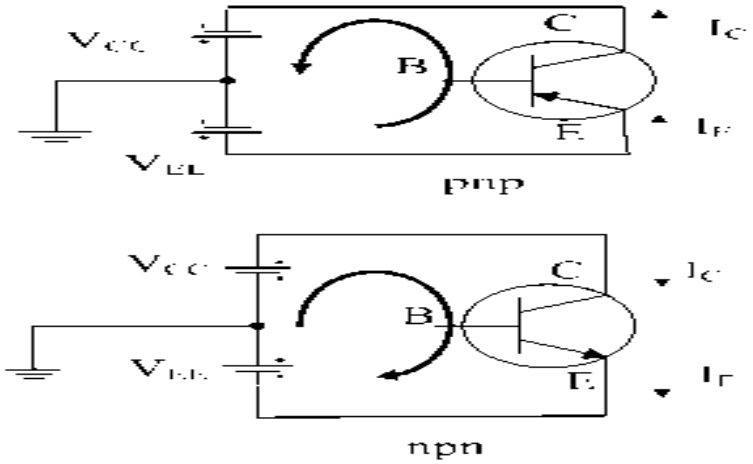
I_c = □I_E + I_{CBO}

It can then be summarize to I_c = □I_E (ignore I_{CBO} due to small value)

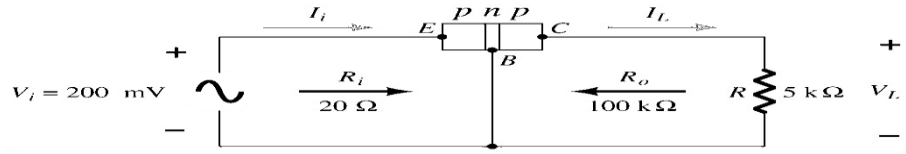
For ac situations where the point of operation moves on the characteristics curve, an ac alpha defined by α_{ac}

Common base current gain factor shows the efficiency by calculating the current percent from current flow from emitter to collector. The value of □ is typical from 0.9 ~ 0.998.

Biasing: Proper biasing CB configuration in active region by approximation $I_c \approx I_E$ ($I_B \approx$ 0 uA)



3.6 **TRANSISTOR AS AN AMPLIFIER**



3.7

Common-Emitter Configuration

It is called common-emitter configuration since : emitter is common or reference to both input and output terminals. Emitter is usually the terminal closest to or at ground potential.

Almost amplifier design is using connection of CE due to the high gain for current and voltage.

Two set of characteristics are necessary to describe the behaviour for CE ;input (base terminal) and output (collector terminal) parameters.

Proper Biasing common-emitter configuration in active region

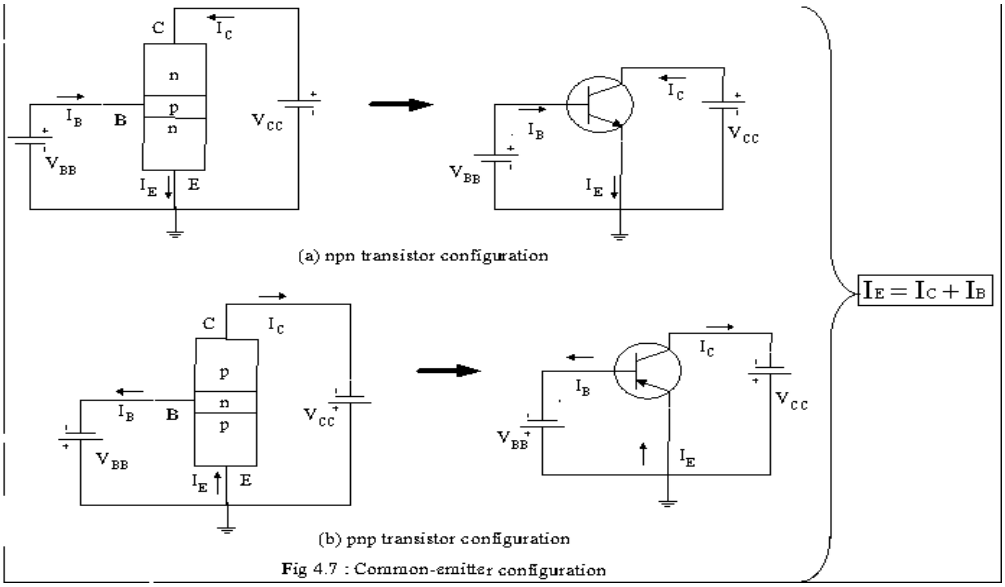


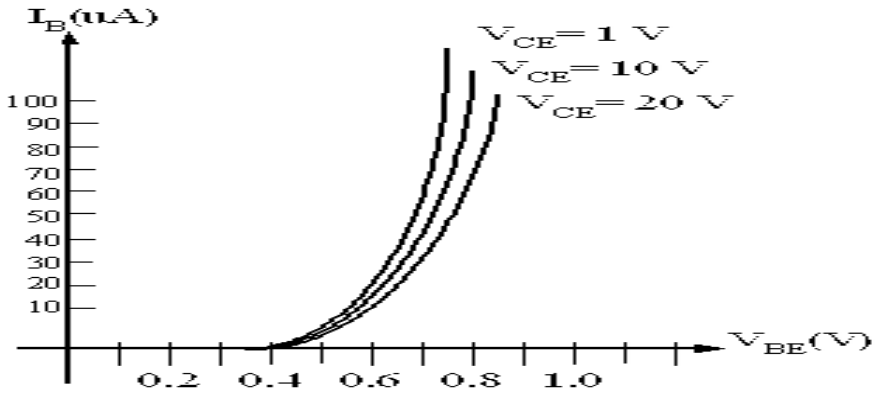
Fig 4.7 : Common-emitter configuration

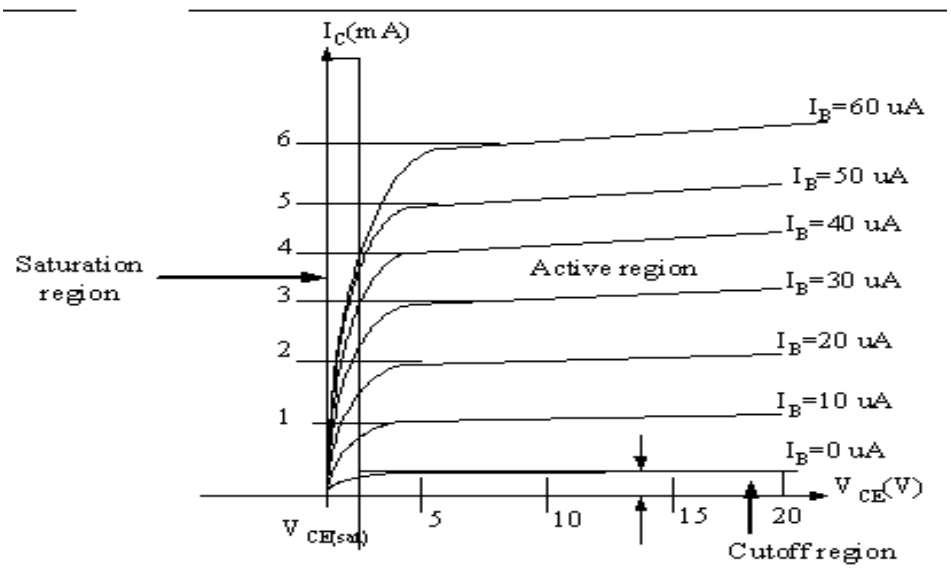
I_B is microamperes compared to miliamperes of I_C.

I_B will flow when V_{BE} > 0.7V for silicon and 0.3V for germanium

Before this value I_B is very small and no I_B.

Base-emitter junction is forward bias Increasing V_{CE} will reduce I_B for different values.





Output characteristics for a common-emitter npn transistor

For small V_{CE} ($V_{CE} < V_{CESAT}$, I_C increase linearly with increasing of V_{CE}

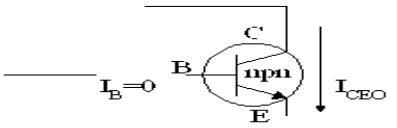
$V_{CE} > V_{CESAT}$ I_C not totally depends on V_{CE} → constant I_C

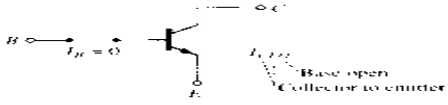
I_B(uA) is very small compare to I_C (mA). Small increase in I_B cause big increase in I_C

I_B=0 A → I_{CEO} occur.

Noticing the value when I_C=0A. There is still some value of current flows.

Active region	Saturation region	Cut-off region
• B-E junction is forward bias • C-B junction is reverse bias • can be employed for voltage, current and power amplification	• B-E and C-B junction is forward bias, thus the values of I_B and I_C is too big. • The value of V_{CE} is so small. • Suitable region when the transistor as a logic switch. • NOT and avoid this region when the transistor as an amplifier.	• region below I_B=0μA is to be avoided if an undistorted o/p signal is required • B-E junction and C-B junction is reverse bias • I_B=0, I_C not zero, during this condition $I_C = I_{CEO}$ where is this current flow when B-E is reverse bias.



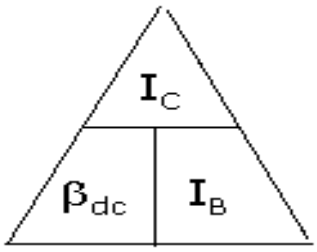


Beta (□) or amplification factor

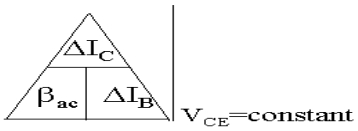
The ratio of dc collector current (IC) to the dc base current (IB) is dc beta (□dc) which is dc current gain where IC and IB are determined at a particular operating point, Q-point (quiescent point). It's define by the following equation:

$30 < \beta_{dc} < 300 \rightarrow$ 2N3904

On data sheet, $\beta_{dc}=hfe$ with *h* is derived from ac hybrid equivalent cct. FE are derived from forward-current amplification and common-emitter configuration respectively.



For ac conditions, an ac beta has been defined as the changes of collector current (I_C) compared to the changes of base current (I_B) where I_C and I_B are determined at operating point. On data sheet, $\beta_{ac}=hfe$ It can defined by the following equation:



From output characteristics of common emitter configuration, find β_{ac} and β_{dc} with an

Operating point at I_B=25 μA and V_{CE} =7.5V

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B}\Big|_{V_{ce}\ =\ \text{constant}}$$

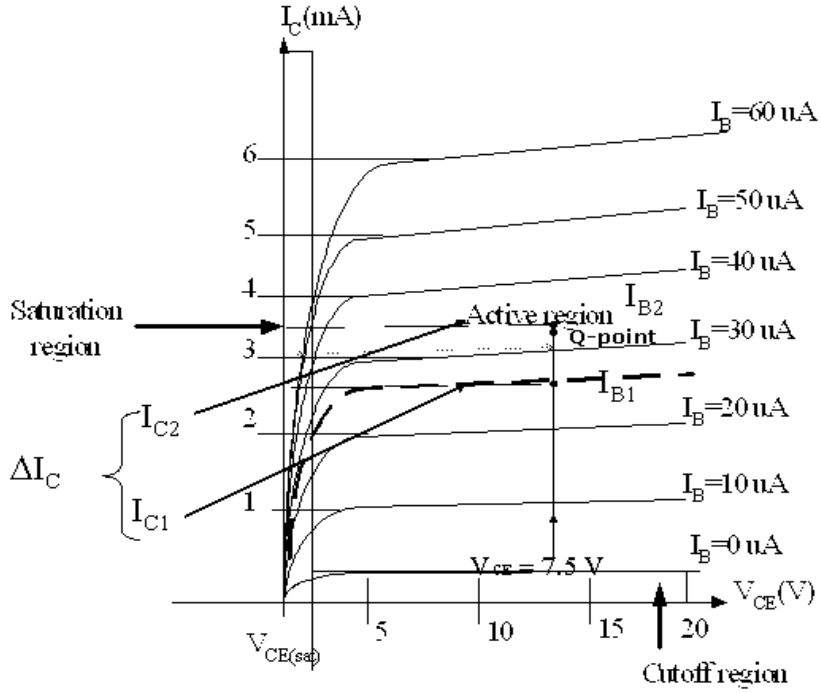
$$= \frac{I_{C2} - I_{C1}}{I_{B2} - I_{B1}} = \frac{3.2\,m - 2.2\,m}{30\,\mu - 20\,\mu}$$

$$= \frac{1\,m}{10\,\mu} = 100$$

$$\beta_{dc} = \frac{I_C}{I_B}$$

$$= \frac{2.7\,m}{25\,\mu}$$

$$= \underline{\underline{108}}$$



Relationship analysis between α and β

CASE 1

$I_E = I_C + I_B$ (1)

subtitute equ. $I_C = \beta I_B$ into (1) we get

$$I_E = (\beta + 1) I_B$$

CASE 2

known : $\alpha = \frac{I_C}{I_E} \Rightarrow I_E = \frac{I_C}{\alpha}$ (2)

known : $\beta = \frac{I_C}{I_B} \Rightarrow I_B = \frac{I_C}{\beta}$ (3)

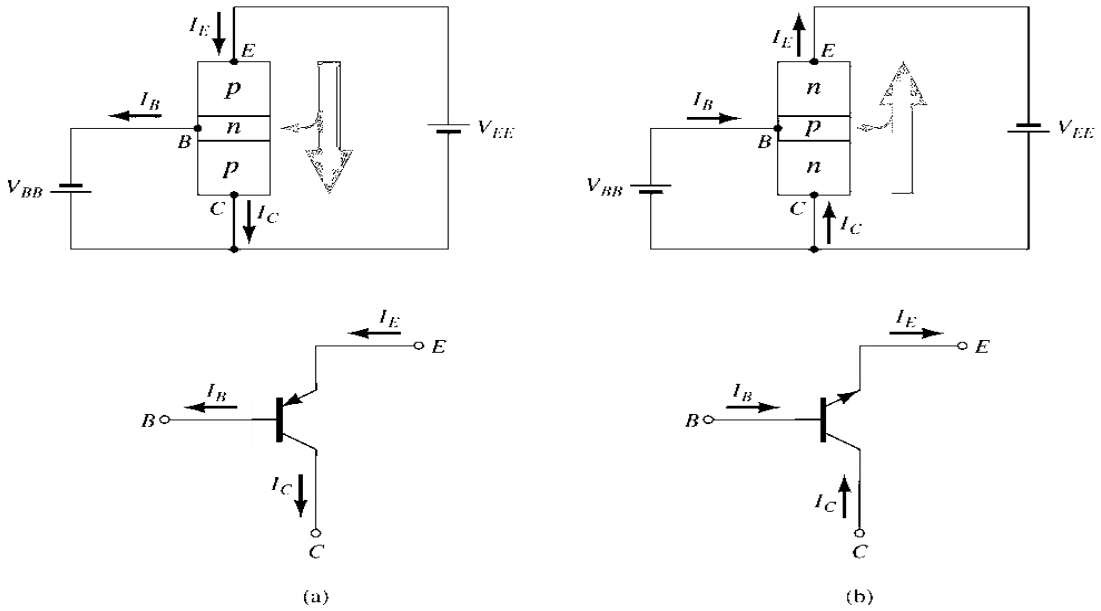
subtitute (2) and (3) into (1) we get,

$$\alpha = \frac{\beta}{\beta + 1} \quad \text{and} \quad \beta = \frac{\alpha}{1 - \alpha}$$

3.7 COMMON – COLLECTOR CONFIGURATION

Also called emitter-follower (EF). It is called common-emitter configuration since both the signal source and the load share the collector terminal as a common connection point. The output voltage is obtained at emitter terminal. The input characteristic of common-collector configuration is similar with common-emitter configuration. Common-collector circuit configuration is provided with the load

resistor connected from emitter to ground. It is used primarily for impedance-matching purpose since it has high input impedance and low output impedance.



For the common-collector configuration, the output characteristics are a plot of I_E vs V_{CE} for a range of values of I_B.

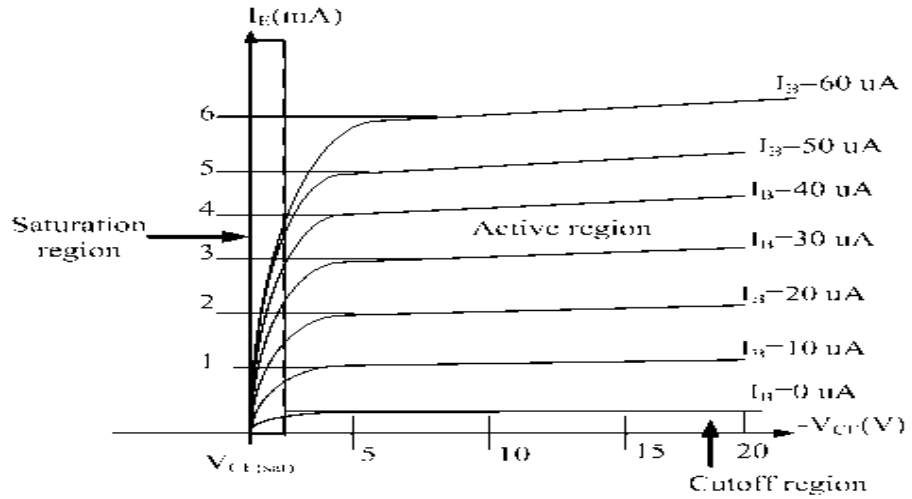


Fig 4.9 : Output characteristic in CC configuration for npn transistor

Limits of operation

Many BJT transistors used as an amplifier. Thus it is important to notice the limits of operations. At least 3 maximum values is mentioned in data sheet.

There are:

a) Maximum power dissipation at collector: P_{Cmax} or P_D

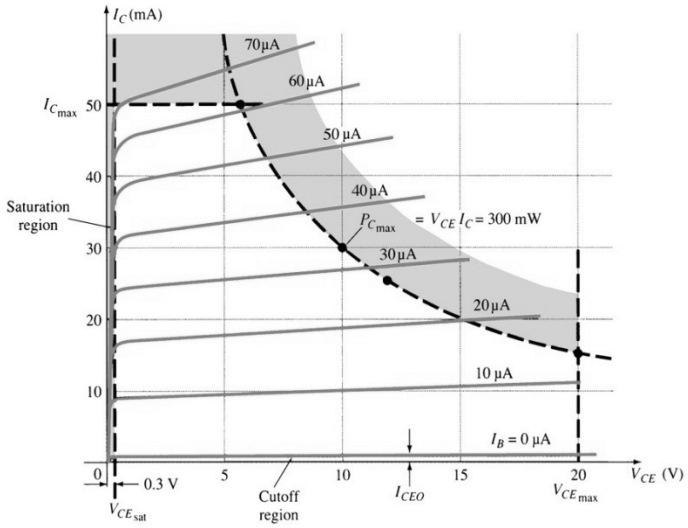
b) Maximum collector-emitter voltage: V_{CEmax} sometimes named as $V_{BR(CEO)}$) or V_{CEO}.

c) Maximum collector current: ICmax

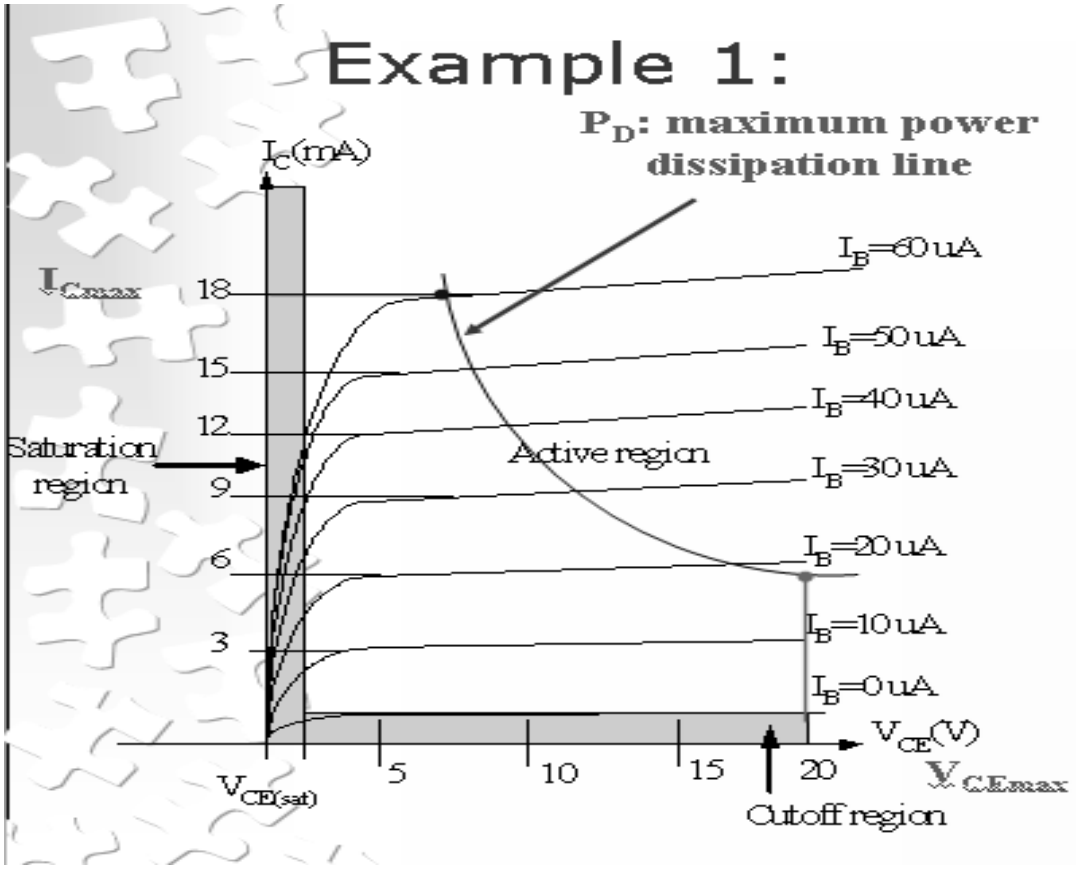
There are few rules that need to be followed for BJT transistor used as an amplifier. The rules are: transistor needs to be operated in active region!

$I_C < I_{Cmax}$

$P_C < P_{Cmax}$



Note: V_{CE} is at maximum and I_C is at minimum ($I_{CMAX}=I_{CEO}$) in the cutoff region. I_C is at maximum and V_{CE} is at minimum (V_{CE} max = V_{cesat} = V_{CEO}) in the saturation region. The transistor operates in the active region between saturation and cutoff.



Refer to the fig. Example; A derating factor of 2mW/°C indicates the power dissipation is reduced 2mW each degree centigrade increase of temperature.

Step1:

The maximum collector power dissipation,

$\mathbf{P_D = I_{CMAX} \times V_{CEmax}}$ = 18m x 20 = 360 mW

Step 2:

At any point on the characteristics the product of and must be equal to 360 mW.

Ex. 1. If choose I_{Cmax} = 5 mA, substitute into the (1), we get

$V_{CEmax} I_{Cmax}$ = 360 mW

V_{CEmax}(5 m)=360/5=7.2 V

Ex.2. If choose V_{CEmax}=18 V, substitute into (1), we get

$V_{CEmax} I_{Cmax}$ = 360 mW

(10) I_{CMAX}=360m/18=20 mA

Derating P_{Dmax}

P_{DMAX} is usually specified at 25°C.

The higher temperature goes, the less is P_{DMAX}

Example;A derating factor of 2mW/°C indicates the power dissipation is reduced 2mW each degree centigrade increase of temperature.

UNIT – IV

Contents:

1. **Operating point, DC & AC load lines**
2. **Need for biasing**
3. **Biasing methods**
4. **Bias stability**
5. **Thermal Runaway**

TRANSISTOR BIASING AND STABILIZATION

4.1 NEED FOR TRANSISTOR BIASING:

If the o/p signal must be a faithful reproduction of the i/p signal, the transistor must be operated in active region. That means an operating point has to be established in this region . To establish an operating point (proper values of collector current I_c and collector to emitter voltage V_{CE}) appropriate supply voltages and resistances must be suitably chosen in the ckt. This process of selecting proper supply voltages and resistance for obtaining desired operating point or Q point is called as biasing and the ckt used for transistor biasing is called as biasing ckt.

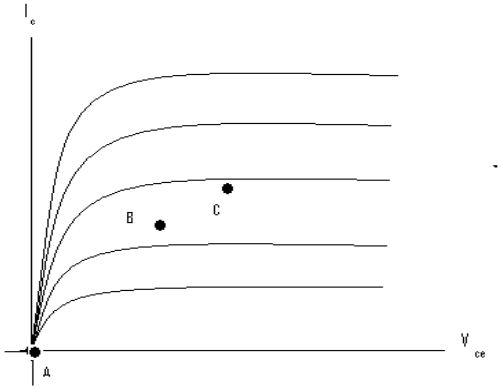
There are four conditions to be met by a transistor so that it acts as a faithful ampr:

1. Emitter base junction must be forward biased (V_{BE}=0.7Vfor Si, 0.2V for Ge) and collector base junction must be reverse biased for all levels of i/p signal.
2. V_{ce} voltage should not fall below $V_{CE\,(sat)}$ (0.3V for Si, 0.1V for Ge) for any part of the i/p signal. For V_{CE} less than $V_{CE\,(sat)}$ the collector base junction is not probably reverse biased.
3. The value of the signal I_c when no signal is applied should be at least equal to the max. Collector current t due to signal alone.
4. Max. Rating of the transistor $I_{c(max)}$, $V_{CE\,(max)}$ and $P_{D(max)}$ should not be exceeded at any value of i/p signal.

Consider the fig shown in fig1. If operating point is selected at A, A represents a condition when no bias is applied to the transistor i.e, I_c=0, V_{CE} =0. It does not satisfy the above said conditions necessary for faithful amplification.

Point C is too close to $P_{D(max)}$ curve of the transistor. Therefore the o/p voltage swing in the positive direction is limited.

Point B is located in the middle of active region .It will allow both positive and negative half cycles in the o/p signal. It also provides linear gain and larger possible o/p voltages and currents hence operating point for a transistor amplifier is selected to be in the middle of active region.



4.2 DC LOAD LINE:

Referring to the biasing circuit of fig 4.2a, the values of V_{CC} and R_C are fixed and Ic and V_{CE} are dependent on R_B.

Applying Kirchhoff's voltage law to the collector circuit in fig. 4.2a, we get

$$Vcc = IcRc + Vce$$

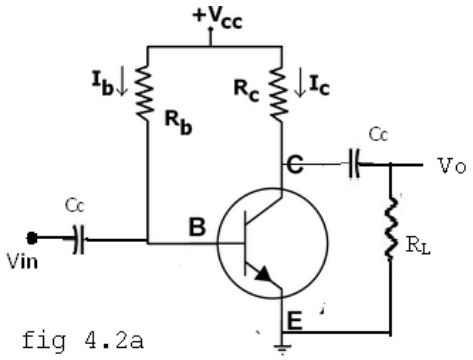


fig 4.2a

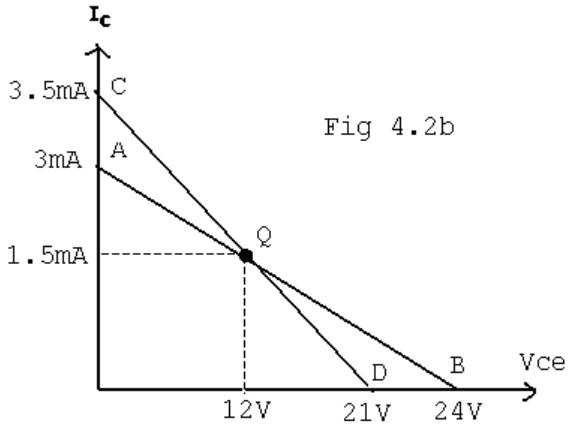


Fig 4.2b

The straight line represented by AB in fig4.2b is called the dc load line. The coordinates of the end point A are obtained by substituting V_{CE} =0 in the above equation. Then $Ic = \frac{Vcc}{Rc} Ic = \frac{Vcc}{Rc}$. Therefore The coordinates of A are V_{CE} =0 and $Ic = \frac{Vcc}{Rc} Ic = \frac{Vcc}{Rc}$.

The coordinates of B are obtained by substituting Ic=0 in the above equation. Then Vce = Vcc. Therefore the coordinates of B are V_{CE} =Vcc and Ic=0. Thus the dc load line AB can be drawn if the values of Rc and Vcc are known.

As shown in the fig4.2b, the optimum POINT IS LOCATED AT THE MID POINT OF THE MIDWAY BETWEEN a AND b. In order to get faithful amplification, the Q point must be well within the active region of the transistor.

Even though the Q point is fixed properly, it is very important to ensure that the operating point remains stable where it is originally fixed. If the Q point shifts nearer to either A or B, the output voltage and current get clipped, thereby o/p signal is distorted.

In practice, the Q-point tends to shift its position due to any or all of the following three main factors.

1. Reverse saturation current, Ico, which doubles for every 10°C raise in temperature
2. Base emitter Voltage ,VBE, which decreases by 2.5 mV per °C
3. Transistor current gain, h_{FE} or β which increases with temperature.

If base current I_B is kept constant since I_B is approximately equal to Vcc/RB. If the transistor is replaced by another one of the same type, one cannot ensure that the new transistor will have identical parameters as that of the first one. Parameters such as β vary over a range. This results in the variation of collector current Ic for a given I_B. Hence, in the o/p characteristics, the spacing between the curves might increase or decrease which leads to the shifting of the Q-point to a location which might be completely unsatisfactory.

4.3 AC LOAD LINE:

After drawing the dc load line, the operating point Q is properly located at the centre of the dc load line. This operating point is chosen under zero input signal condition of the circuit. Hence the ac load line should also pas through the operating point Q. The effective ac load resistance R_{ac}, is a combination of R_C parallel to R_L i.e. $R_{ac} = R_L R_{ac} = R_{L||} R_C R_C$. So the slope of the ac load line CQD will be $\left(\frac{-1}{R_{ac}}\right)\left(\frac{-1}{R_{ac}}\right)$. To draw the ac load line, two end points, I.e. $V_{CE(max)}$ and $I_{C(max)}$ when the signal is applied are required.

$V_{CE(\max)} = V_{CEQ} + I_{CQ} R_{ac}\, V_{CE(\max)} = V_{CEQ} + I_{CQ} R_{ac}$, which locates point D on the Vce axis.

$I_{c(\max))} = I_{CQ} + \frac{V_{CEQ}}{R_{ac}} I_{c(\max))} = I_{CQ} + \frac{V_{CEQ}}{R_{ac}}$, which locates the point C on the I_C axis.

By joining points c and D, ac load line CD is constructed. As $R_C > R_{ac}$, The dc load line is less steep than ac load line.

4.4 STABILITY FACTOR (S):

The rise of temperature results in increase in the value of transistor gain β and the leakage current Ico. So, I_C also increases which results in a shift in operating point. Therefore, The biasing network should be provided with thermal stability. Maintenance of the operating point is specified by S, which indicates the degree of change in operating point due to change in temperature.

The extent to which I_C is stabilized with varying I_C is measured by a stability factor S

$$S = \frac{\partial I_C}{\partial I_{CO}} S = \frac{\partial I_C}{\partial I_{CO}} \approx \frac{dI_C}{dI_{CO}} \approx \frac{\Delta I_C}{\Delta I_{CO}} \approx \frac{dI_C}{dI_{CO}} \approx \frac{\Delta I_C}{\Delta I_{CO}}, \beta \text{ and } I_B \text{ constant } \beta \text{ and } I_B \text{ constant}$$

For CE configuration $I_C = \beta I_B + (1+\beta) I_{CO} I_C = \beta I_B + (1+\beta) I_{CO}$

Differentiate the above equation w.r.t I_C , We get

$$1 = \beta \frac{dI_B}{dI_C} + (1+\beta) \frac{dI_{CO}}{dI_C}$$

$$\therefore \left(1 - \beta \frac{dI_B}{dI_C}\right) = \frac{(\beta+1)}{S}$$

$$\therefore \quad S = \frac{1+\beta}{1-\beta\frac{dI_B}{dI_C}}$$

S should be small to have better thermal stability.

Stability factor S' and S'':

S' is defined as the rate of change of I_C with V_{BE}, keeping I_C and V_{BE} constant. $S' = \frac{\partial I_c}{\partial V_{BE}}$

S'' is defined as the rate of change of I_C with β, keeping I_{CO} and V_{BE} constant. $S'' = \frac{\partial I_c}{\partial \beta}$

4.5 METHODS OF TRANSISTOR BIASING:

1) Fixed bias (base bias)

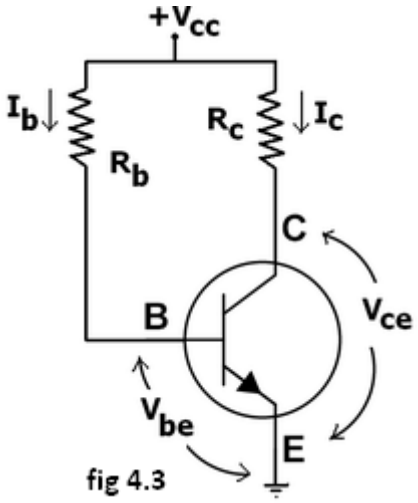


fig 4.3

This form of biasing is also called *base bias*. In the fig 4.3 shown, the single power source (for example, a battery) is used for both collector and base of a transistor, although separate batteries can also be used.

In the given circuit,

$V_{cc} = I_B R_B + V_{be}$

Therefore, $I_B = (V_{cc} - V_{be})/R_B$

Since the equation is independent of current $I_C R$, $dI_B/dI_C R = 0$ and the stability factor is given by the

Equation reduces to S=1+β

Since β is a large quantity, this is very poor biasing circuit. Therefore in practice the circuit is not used for biasing.

For a given transistor, V_{be} does not vary significantly during use. As V_{cc} is of fixed value, on selection of R_B, the base current I_B is fixed. Therefore this type is called *fixed bias* type of circuit.

Also for given circuit, $V_{cc} = I_C R_C + V_{ce}$

Therefore, $V_{ce} = V_{cc} - I_C R_C$

Merits:

- It is simple to shift the operating point anywhere in the active region by merely changing the base resistor (R_B).
- A very small number of components are required.

Demerits:

- The collector current does not remain constant with variation in temperature or power supply voltage. Therefore the operating point is unstable.
- Changes in V_{be} will change I_B and thus cause R_E to change. This in turn will alter the gain of the stage.
- When the transistor is replaced with another one, considerable change in the value of β can be expected. Due to this change the operating point will shift.

2) EMITTER-FEEDBACK BIAS:

The emitter feedback bias circuit is shown in the fig 4.4. The fixed bias circuit is modified by attaching an external resistor to the emitter. This resistor introduces negative feedback that stabilizes the Q-point. From Kirchhoff's voltage law, the voltage across the base resistor is

$V_{Rb} = V_{CC} - I_e R_e - V_{be}$.

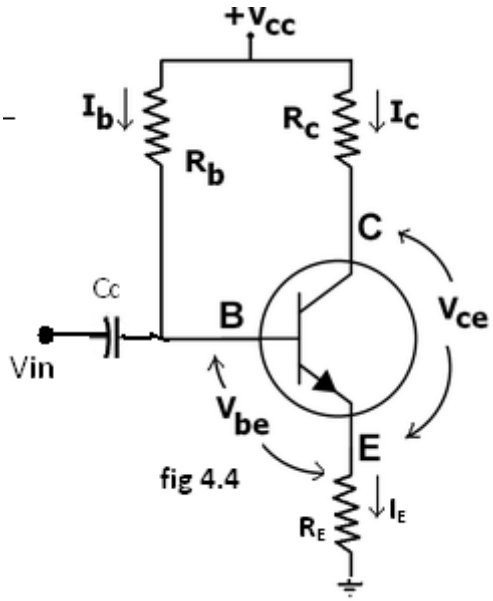


fig 4.4

From Ohm's law, the base current is

$I_b = V_{Rb} / R_b$.

The way feedback controls the bias point is as follows. If V_{be} is held constant and temperature increases, emitter current increases. However, a larger I_e increases the emitter voltage $V_e = I_eR_e$, which in turn reduces the voltage V_{Rb} across the base resistor. A lower base-resistor voltage drop reduces the base current, which results in less collector current because $I_c = ß\ I_B$. Collector current and emitter current are related by $I_c = \alpha\ I_e$ with $\alpha \approx 1$, so increase in emitter current with temperature is opposed, and operating point is kept stable.

Similarly, if the transistor is replaced by another, there may be a change in I_C (corresponding to change in β-value, for example). By similar process as above, the change is negated and operating point kept stable.

For the given circuit,

$I_B = (V_{CC} - V_{be})/(R_B + (\beta+1)R_E)$.

Merits:

The circuit has the tendency to stabilize operating point against changes in temperature and β-value.

Demerits:

- In this circuit, to keep I_C independent of β the following condition must be met:

$$I_C = \beta I_B = \frac{\beta(V_{CC} - V_{be})}{R_B + (\beta + 1)R_E} \approx \frac{(V_{CC} - V_{be})}{R_E}$$

Which is approximately the case if $(\beta + 1)R_E >> R_B$.

- As β-value is fixed for a given transistor, this relation can be satisfied either by keeping R_E very large, or making R_B very low.
- If R_E is of large value, high V_{CC} is necessary. This increases cost as well as precautions necessary while handling.
- If R_B is low, a separate low voltage supply should be used in the base circuit. Using two supplies of different voltages is impractical.
- In addition to the above, R_E causes ac feedback which reduces the voltage gain of the amplifier.

3. COLLECTOR TO BASE BIAS OR COLLECTOR FEED-BACK BIAS:

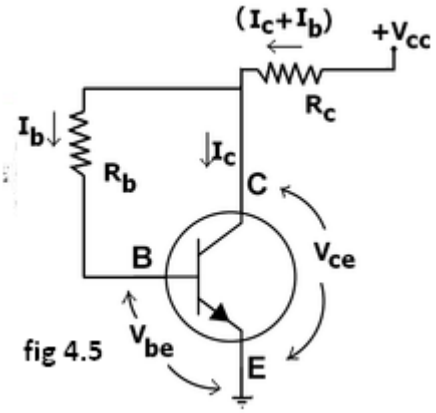


fig 4.5

This configuration shown in fig 4.5 employs negative feedback to prevent thermal runaway and stabilize the operating point. In this form of biasing, the base resistor R_B is connected to the collector instead of connecting it to the DC source V_{cc}. So any thermal runaway will induce a voltage drop across the R_C resistor that will throttle the transistor's base current.

From Kirchhoff's voltage law, the voltage V_{R_b}across the base resistor R_b is

$$V_{R_b} = V_{cc} - \overbrace{(I_c + I_b)R_c}^{\text{Voltage drop across } R_c} - \overbrace{V_{be}}^{\text{Voltage at base}}.$$

By the Ebers–Moll model, $I_c = \beta I_b$, and so

$$V_{R_b} = V_{cc} - (\overbrace{\beta I_b}^{I_c} + I_b)R_c - V_{be} = V_{cc} - I_b(\beta + 1)R_c - V_{be}.$$

From Ohm's law, the base current $I_b = V_{R_b}/R_b$, and so

$$\overbrace{I_b R_b}^{V_{R_b}} = V_{cc} - I_b(\beta + 1)R_c - V_{be}.$$

Hence, the base current I_b is

$$I_b = \frac{V_{cc} - V_{be}}{R_b + (\beta + 1)R_c}$$

If V_{be} is held constant and temperature increases, then the collector current I_c increases. However, a larger I_c causes the voltage drop across resistor R_c to increase, which in turn reduces the voltage V_{R_b}across the base resistor R_b. A lower base-resistor voltage drop reduces the base current I_b, which results in less collector current I_c. Because an increase in collector current with temperature is opposed, the operating point is kept stable.

Merits:

- Circuit stabilizes the operating point against variations in temperature and β (i.e. replacement of transistor)

Demerits:

- In this circuit, to keep I_c independent of β, the following condition must be met:

$$I_c = \beta I_b = \frac{\beta(V_{cc} - V_{be})}{R_b + R_c + \beta R_c} \approx \frac{(V_{cc} - V_{be})}{R_c}$$

which is the case when

$$\beta R_c \gg R_b.$$

- As β-value is fixed (and generally unknown) for a given transistor, this relation can be satisfied either by keeping R_c fairly large or making R_b very low.
- If R_c is large, a high V_{cc} is necessary, which increases cost as well as precautions necessary while handling.
- If R_b is low, the reverse bias of the collector–base region is small, which limits the range of collector voltage swing that leaves the transistor in active mode.
- The resistor R_b causes an AC feedback, reducing the voltage gain of the amplifier. This undesirable effect is a trade-off for greater Q-point stability.

Usage: The feedback also decreases the input impedance of the amplifier as seen from the base, which can be advantageous. Due to the gain reduction from feedback, this biasing form is used only when the trade-off for stability is warranted.

4. COLLECTOR –EMITTER FEEDBACK BIAS:

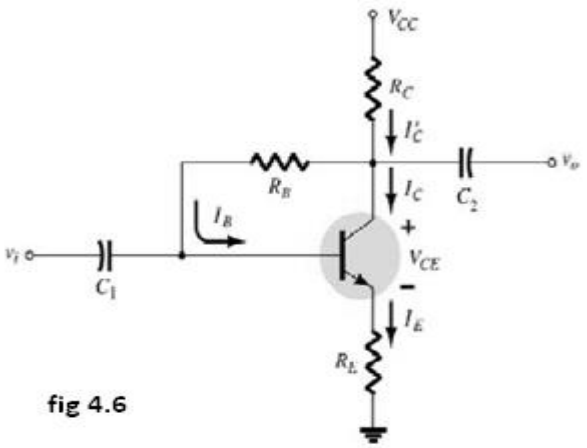


fig 4.6

The above fig4.6 shows the collector –emitter feedback bias circuit that can be obtained by applying both the collector feedback and emitter feedback. Here the collector feedback is provided by connecting a resistance RB from the collector to the base and emitter feedback is provided by connecting an emitter Re from emitter to ground. Both feed backs are used to control collector current and base current IB in the opposite direction to increase the stability as compared to the previous biasing circuits.

5. VOLTAGE DIVIDER BIAS OR SELF BIAS OR EMITTER BIAS:

The voltage divider as shown in the fig 4.7 is formed using external resistors R_1 and R_2. The voltage across R_2 forward biases the emitter junction. By proper selection of resistors R_1 and R_2, the operating point of the transistor can be made independent of β. In this circuit, the voltage divider holds the base voltage fixed independent of base current provided the divider current is large compared to the base current. However, even with a fixed base voltage, collector current varies with temperature (for example) so an emitter resistor is added to stabilize the Q-point, similar to the above circuits with emitter resistor.

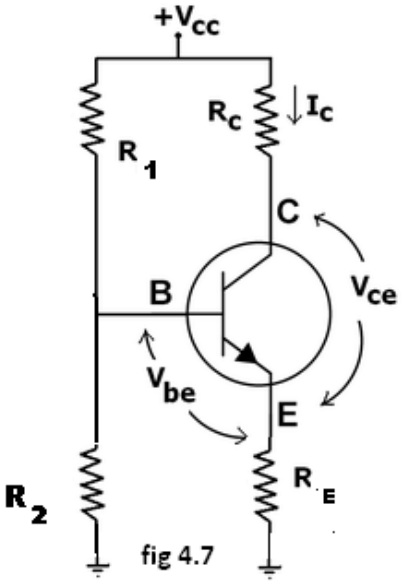


fig 4.7

In this circuit the base voltage is given by:

$$V_B = \text{voltage across } R_2 = V_{cc}\frac{R_2}{(R_1+R_2)} - I_B\frac{R_1R_2}{(R_1+R_2)}$$

$$\approx V_{cc}\frac{R_2}{(R_1+R_2)} \text{ provided } I_B << I_2 = V_B/R_2.$$

Also $V_B = V_{be} + I_E R_E$

For the given circuit,

$$I_B = \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{(\beta+1)R_E + R_1 \parallel R_2}.$$

Let the current in resistor R1 is I1 and this is divided into two parts – current through base and resistor R2. Since the base current is very small so for all practical purpose it is assumed that I1 also flows through R2, so we have

$$I_1 = \frac{V_{CC}}{R_1+R_2}$$

$$V_2 = \frac{V_{CC}}{R_1+R_2}\cdot R_2$$

Applying KVL in the circuit, we have

$$V_2 = V_{BE} + V_E$$

$$V_2 = V_{BE} + I_E R_E$$

$$I_E = \frac{V_2 - V_{BE}}{R_E}$$

$$I_C = \frac{V_2 - V_{BE}}{R_E} \quad \because I_C \cong I_E$$

$$I_C = \frac{\frac{V_{CC}}{R_1 + R_2} \cdot R_2 - V_{BE}}{R_E}$$

It is apparent from above expression that the collector current is independent of? Thus the stability is excellent. In all practical cases the value of VBE is quite small in comparison to the V2, so it can be ignored in the above expression so the collector current is almost independent of the transistor parameters thus this arrangement provides excellent stability.

Again applying KVL in collector circuit, we have

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$\because I_C \cong I_E$$

$$\therefore V_{CC} = I_C R_C + V_{CE} + I_C R_E$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

The resistor RE provides stability to the circuit. If the current through the collector rises, the voltage across the resistor RE also rises. This will cause VCE to increase as the voltage V2 is independent of collector current. This decreases the base current, thus collector current increases to its former value.

Stability factor for such circuit arrangement is given by

$$S = \frac{(1+\beta)(R_{eq} + R_E)}{R_{eq} + R_E(1+\beta)}$$

$$R_{eq} = R_1 || R_2$$

$$S = \frac{(1+\beta)\left(1 + \frac{R_{eq}}{R_E}\right)}{\frac{R_{eq}}{R_E} + 1 + \beta}$$

If Req/RE is very small compared to 1, it can be ignored in the above expression thus we have

$$S = \frac{1+\beta}{1+\beta} = 1$$

Which is excellent since it is the smallest possible value for the stability. In actual practice the value of stability factor is around 8-10, since Req/RE cannot be ignored as compared to 1.

Merits:

- Unlike above circuits, only one dc supply is necessary.

- Operating point is almost independent of β variation.
- Operating point stabilized against shift in temperature.

Demerits:

- In this circuit, to keep I_C independent of β the following condition must be met:

$$I_C = \beta I_B = \beta \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{(\beta+1)R_E + R_1 \parallel R_2} \approx \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{R_E},$$

which is approximately the case if $(\beta+1)R_E >> R_1 \parallel R_2$

where $R_1 \parallel R_2$ denotes the equivalent resistance of R_1 and R_2 connected in parallel.

- As β-value is fixed for a given transistor, this relation can be satisfied either by keeping R_E fairly large, or making $R_1 \| R_2$ very low.
- If R_E is of large value, high V_{CC} is necessary. This increases cost as well as precautions necessary while handling.
- If $R_1 \parallel R_2$ is low, either R_1 is low, or R_2 is low, or both are low. A low R_1 raises V_B closer to V_C, reducing the available swing in collector voltage, and limiting how large R_C can be made without driving the transistor out of active mode. A low R_2 lowers V_{be}, reducing the allowed collector current. Lowering both resistor values draws more current from the power supply and lowers the input resistance of the amplifier as seen from the base.
- AC as well as DC feedback is caused by R_E, which reduces the AC voltage gain of the amplifier. A method to avoid AC feedback while retaining DC feedback is discussed below.

Usage: The circuit's stability and merits as above make it widely used for linear circuits.

4.6 BIAS COMPENSATION USING DIODE AND TRANSISTOR:

The various biasing circuits considered use some type of negative feedback to stabilize the operation point. Also, diodes, thermistors and sensistors can be used to compensate for variations in current.

DIODE COMPENSATION:

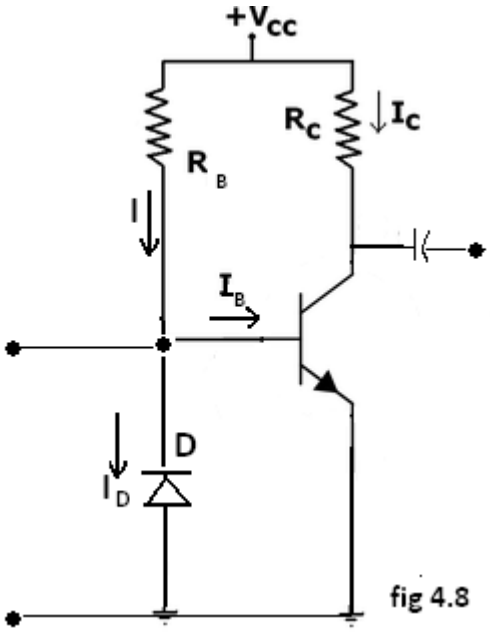


fig 4.8

The following fig4.8 shows a transistor amplifier with a diode D connected across the base-emitter junction for compensation of change in collector saturation current I_{CO}. The diode is of the same material as the transistor and it is reverse biased by e the emitter-base junction voltage V_{BE}, allowing the diode reverse saturation current I_o to flow through diode D. The base current $I_B=I-I_o$.

As long as temperature is constant, diode D operates as a resistor. As the temperature increases, I_{CO} of the transistor increases. Hence, to compensate for this, the base current I_B should be decreased.

The increase in temperature will also cause the leakage current I_o through D to increase and thereby decrease the base current I_B. This is the required action to keep Ic constant.

This type of bias compensation does not need a change in Ic to effect the change in I_C, as both I_o and I_{CO} can track almost equally according to the change in temperature.

THERMISTOR COMPENSATION:

The following fig4.9 a thermistor R_T, having a negative temperature coefficient is connected in parallel with R_2. The resistance of thermistor decreases exponentially with increase of temperature. An increase of temperature will decrease the base voltage V_{BE}, reducing I_B and I_C.

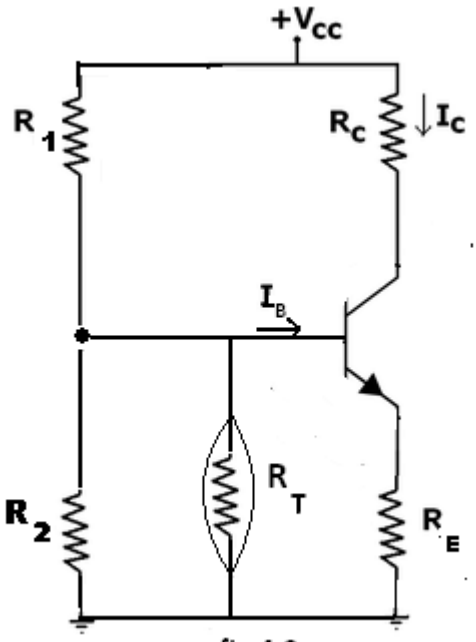


fig 4.9

SENSISTOR COMPENSATION:

In the following fig4.10 shown a sensistor Rs having a positive temperature coefficient is connected across R_1 or R_E. Rs increases with temperature. As the temperature increases, the equivalent resistance of the parallel combination of R1 and Rs also increases and hence V_{BE} decreases, reducing I_B and Ic. This reduced Ic compensates for increased Ic caused by the increase in V_{BE}, I_{CO} and β due to temperature.

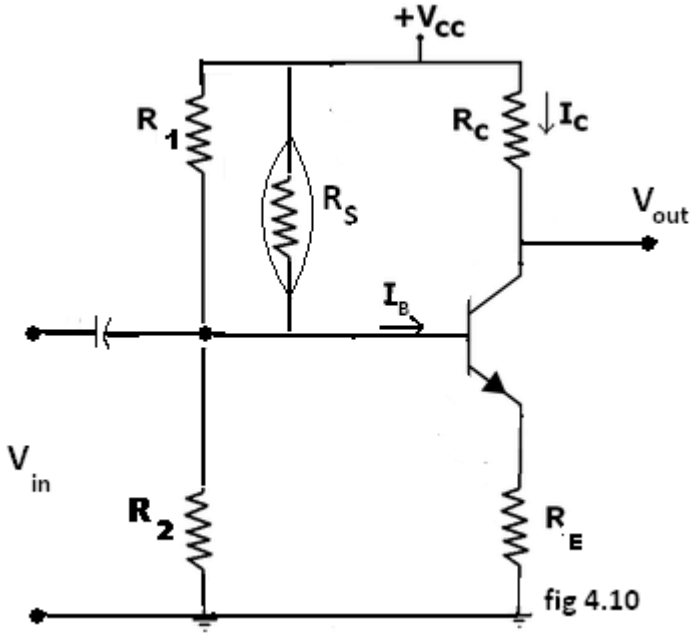


fig 4.10

4.7 THERMAL RUNAWAY AND THERMAL STABILITY:

THERMAL RUNAWAY:

The collector current for the CE circuit is given by $I_C = \beta I_B + (1+\beta) I_{CO}$. The three variables in the equation, β, I_B, and I_{CO} increases with rise in temperature. In particular, the reverse saturation current or leakage current I_{CO} changes greatly with temperature, specifically it doubles for every 10°C rise in temperature. The collector current I_C causes the collector base junction temperature to rise which in turn, increase I_{CO} , as a result I_C will increase still further, which will further rise the temperature at the collector base junction. This process will become cumulative leading at the collector base junction. This process will become cumulative leading to *"thermal runaway"*. Consequently, the ratings of the transistor are exceeded which may destroy the transistor itself.

The collector is made larger in size than the emitter in order to help the heat developed at the collector junction. However if the circuit is designed such that the base current $I_B I_B$ is made to decrease automatically with rise in temperature, then the decrease in βI_B will compensate for increase in the $(1+\beta) I_{CO}$, keeping I_C almost constant.

THERMAL RESISTANCE

Consider transistor used in a circuit where the ambient temperature of the air around the transistor is T_A°C and the temperature of the collector-base junction of the transistor is T_J°C.

Due to heating within the transistor T_J is higher than T_A. As the temperature difference T_J- T_A is greater, the power dissipated in the transistor, P_D will be greater, i.e, T_J- T_A $\propto\propto$ P_D

The equation can be written as T_J- T_A $== \Theta\Theta P_D$. , where $\Theta\Theta$ is the constant of proportionality and is called the Thermal resistance. Rearranging the above equation $\Theta\Theta$ = T_J- T_A /P_D. Hence $\Theta\Theta$ is measured in °C/W which may be as small as 0.2 °C/W for a high power transistor that has an efficient heat sink or up to 1000°C/W for small signal, low power transistor which have no cooling provision.

As Θ represents total thermal resistance from a transistor junction to the ambient temperature, it is referred to as Θ_{J-A}. However, for power transistors, thermal resistance is given form junction to case, Θ_{J-C}.

The amount resistance from junction to ambience is considered to consist of 2 parts.

$$\Theta_{J-A} = \Theta_{J-C} - \Theta_{C-A}.$$

Which indicates the heat dissipated in the junction must make its way to the surrounding air through two series paths from junction to case and from case to air? Hence the power dissipated.

$$P_D = (T_J - T_A)/\Theta_{J-A}$$

$$=(T_J - T_A)/(\Theta_{J-C} + \Theta_{C-A})$$

Θ_{J-C} is determined by the type of manufacture of the transistor and how it is located I the case, but Θ_{C-A} is determined by the surface area of the case or flange and its contact with air. If the effective surface area of

the transistor case could be increased, the resistance to heat flows, or could be increased $\Theta_{C\text{-}A}$, could be decreased. This can be achieved by the use of a heat sink.

The heat sink is a relatively large, finned, usually black metallic heat conducting device in close contact with transistor case or flange. Many versions of heat sink exist depending upon the shape and size of the transistor. Larger the heat sink smaller is the thermal resistance $\Theta_{HS\text{-}A}$.

This thermal resistance is not added to $\Theta_{C\text{-}A}$ in series, but is instead in parallel with it and if

$\Theta_{HS\text{-}A}$ is much less than $\Theta_{C\text{-}A}$, then $\Theta_{C\text{-}A}$ will be reduced significantly, thereby improving the dissipation capability of the transistor. Thus

$\Theta_{J\text{-}A} = \Theta_{J\text{-}C} + \Theta_{C\text{-}A} \| \Theta_{HS\text{-}A}$.

4.8 CONDITION FOR THERMAL STABILITY:

For preventing thermal runaway, the required condition I the rate at which the heat is released at the collector junction should not exceed the rate at which the heat can be dissipated under steady state condition.

Hence the condition to be satisfied to avoid thermal runaway is given by

$$\frac{\partial P_C}{\partial T_j} < \frac{1}{\Theta}$$

If the circuit is properly designed, then the transistor cannot runaway below a specified ambient temperature or even under any conditions.

In the self biased circuit the transistor is biased in the active region. The power generated at the junction without any signal is

$$P_C = I_C V_{CB} \approx I_C V_{CE}$$

Let us assume that the quiescent collector and the emitter currents are equal. Then

$$P_C = I_C V_{CC} - I_C^2(R_E + R_C) P_C = I_C V_{CC} - I_C^2(R_E + R_C) \quad \text{.....(1)}$$

The condition to prevent thermal runaway can be written as

$$\frac{\partial P_C}{\partial I_C}\frac{\partial I_C}{\partial T_j} < \frac{1}{\Theta} \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (2)$$

As Θ and $\frac{\partial I_C}{\partial T_j}\frac{\partial I_C}{\partial T_j}$ are positive, $\frac{\partial P_C}{\partial I_C}\frac{\partial P_C}{\partial I_C}$ should be negative in order to satisfy the above condition.

Differentiating equation (1) w.r.t $I_C I_C$ we get

$$\frac{\partial P_C}{\partial I_C} = V_{CC} - 2I_C(R_E + R_C) \dots\dots\dots\dots\dots\dots\dots (3)$$

Hence to avoid thermal runaway it is necessary that

$$I_C > \frac{V_{CC}}{2(R_E + R_C)} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4)$$

SinceVCE=VCC-IC(RE+RC) then eq(4) implies that VCE<VCC/2. IF the inequality of eq(4) is not satisfied and VCE<VCC/2, then from eq(3), $\frac{\partial P_C}{\partial I_C}\frac{\partial P_C}{\partial I_C}$ is positive., and the corresponding eq(2) should be satisfied. Other wise thermal runaway will occur.

UNIT – V

Contents:

- **The JFET**
- **MOSFET characteristics in Enhancement & Depletion mode**
- **FET common source amplifier**
- **Common drain FET amplifier**
- **Biasing of FET**
- **Comparison of BJT and FET**

UNIT V

The **Field Effect Transistor** or simply **FET** however, uses the voltage that is applied to their input terminal, called the Gate to control the current flowing through them resulting in the output current being proportional to the input voltage. As their operation relies on an electric field (hence the name field effect) generated by the input Gate voltage, this then makes the **Field Effect Transistor** a "VOLTAGE" operated device.

The **Field Effect Transistor** is a three terminal unipolar semiconductor device that has very similar characteristics to those of their *Bipolar Transistor* counterparts ie, high efficiency, instant operation, robust and cheap and can be used in most electronic circuit applications to replace their equivalent bipolar junction transistors (BJT). Field effect transistors can be made much smaller than an equivalent BJT transistor and along with their low power consumption and power dissipation makes them ideal for use in integrated circuits such as the CMOS range of digital logic chips. The field effect transistor is a three terminal device that is constructed with no PN-junctions within the main current carrying path between the Drain and the Source terminals, which correspond in function to the Collector and the Emitter respectively of the bipolar transistor. The current path between these two terminals is called the "channel" which may be made of either a P-type or an N-type semiconductor material. The control of current flowing in this channel is achieved by varying the voltage applied to the Gate. As their name implies, Bipolar Transistors are "Bipolar" devices because they operate with both types of charge carriers, Holes and Electrons. The Field Effect Transistor on the other hand is a "Unipolar" device that depends only on the conduction of electrons (N-channel) or holes (P-channel).

The **Field Effect Transistor** has one major advantage over its standard bipolar transistor, in that their input impedance, (R in) is very high, (thousands of Ohms), while the BJT is comparatively low. This very high input impedance makes them very sensitive to input voltage signals, but the price of this high sensitivity also means that they can be easily damaged by static electricity. There are two main types of Field Effect Transistor, the **Junction Field Effect Transistor** or **JFET** and the **Insulated-gate Field Effect Transistor** or **IGFET)**, which is more commonly known as the standard **Metal Oxide Semiconductor Field Effect Transistor** or **MOSFET** for short.

The Junction Field Effect Transistor

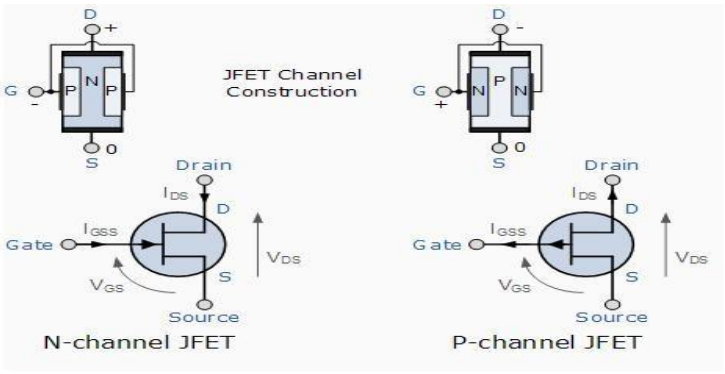
A bipolar junction transistor is constructed using two PN-junctions in the main current carrying path between the Emitter and the Collector terminals. The **Junction Field Effect Transistor** (JFET) has no PN-junctions but instead has a narrow piece of high-resistivity semiconductor material forming a "Channel" of either N-type or P-type silicon for the majority carriers to flow through with two ohmic electrical connections at either end commonly called the Drain and the Source respectively. There are two basic configurations of junction field effect transistor, the N-channel JFET and the P-channel JFET. The N-channel JFET's channel is doped with donor impurities meaning that the flow of current through the channel is negative (hence the term N-channel) in the form of electrons. Likewise, the P-channel JFET's channel is doped with acceptor impurities meaning that the flow of current through the channel is positive (hence

the term P-channel) in the form of holes. N-channel JFET's have a greater channel conductivity (lower resistance) than their equivalent P-channel types, since electrons have a higher mobility through a conductor compared to holes. This makes the N-channel JFET's a more efficient conductor compared to their P-channel counterparts. There are two ohmic electrical connections at either end of the channel called the Drain and the Source. But within this channel there is a third electrical connection which is called the Gate terminal and this can also be a P-type or N-type material forming a PN-junction with the main channel. The relationship between the connections of a junction field effect transistor and a bipolar junction transistor are compared below.

Comparison of connections between a JFET and a BJT?

Bipolar Transistor	Field Effect Transistor
Emitter - (E) >> Source - (S)	
Base - (B) >> Gate - (G)	
Collector - (C) >> Drain - (D)	

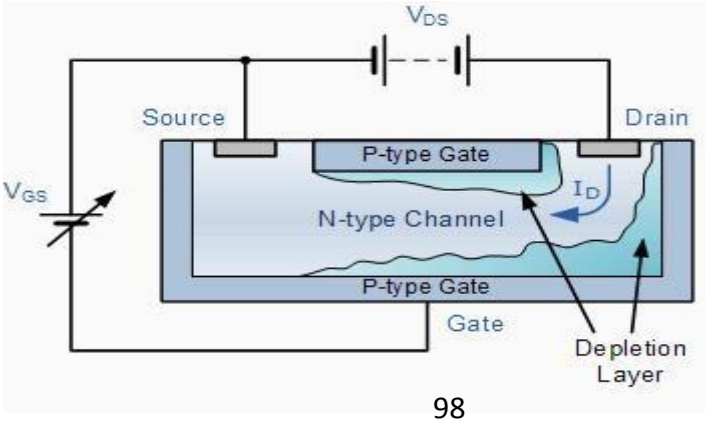
The symbols and basic construction for both configurations of JFETs are shown below.



The semiconductor "channel" of the **Junction Field Effect Transistor** is a resistive path through which a voltage V_{DS} causes a current I_D to flow. The JFET can conduct current equally well in either direction. A voltage gradient is thus formed down the length of the channel with this voltage becoming less positive as we go from the Drain terminal to the Source terminal. The PN-junction therefore has a high reverse bias at the Drain terminal and a lower reverse bias at the Source terminal. This bias causes a "depletion layer" to be formed within the channel and whose width increases with the bias. The magnitude of the current flowing through the channel between the Drain and the Source terminals is controlled by a voltage applied to the Gate terminal, which is a reverse-biased. In an N-channel JFET this Gate voltage is negative while for a P-channel JFET the Gate voltage is positive. The main difference between the JFET and a BJT device is that when the JFET junction is reverse-biased the Gate current is practically zero, whereas the

Base current of the BJT is always some value greater than zero.

Bias arrangement for an N-channel JFET and corresponding circuit symbols?



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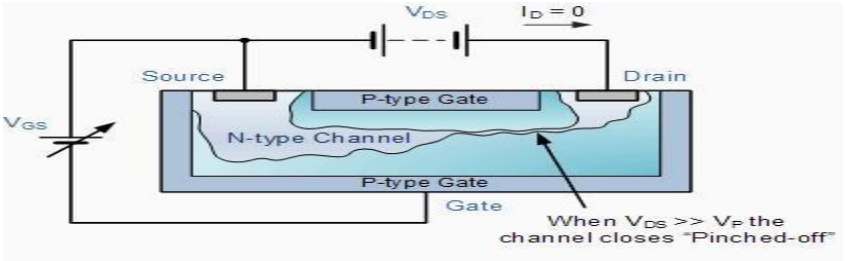
The cross sectional diagram above shows an N-type semiconductor channel with a P-type region called the Gate diffused into the N-type channel forming a reverse biased PN-junction and it is this junction which forms the *depletion region* around the Gate area when no external voltages are applied. JFETs are therefore known as depletion mode devices. This depletion region produces a potential gradient which is of varying thickness around the PN-junction and restrict the current flow through the channel by reducing its effective width and thus increasing the overall resistance of the channel itself. The most-depleted portion of the depletion region is in between the Gate and the Drain, while the least-depleted area is between the Gate and the Source. Then the JFET's channel conducts with zero bias voltage applied (i.e. the depletion region has near zero width).

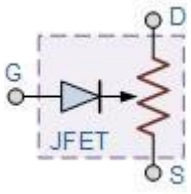
With no external Gate voltage ($V_G = 0$), and a small voltage (V_{DS}) applied between the Drain and the Source, maximum saturation current (I_{DSS}) will flow through the channel from the Drain to the Source restricted only by the small depletion region around the junctions.
If a small negative voltage ($-V_{GS}$) is now applied to the Gate the size of the depletion region begins to increase reducing the overall effective area of the channel and thus reducing the current flowing through it, a sort of "squeezing" effect takes place. So by applying a reverse bias voltage increases the width of the depletion region which in turn reduces the conduction of the channel. Since the PN-junction is reverse biased, little current will flow into the gate connection. As the Gate voltage ($-V_{GS}$) is made more negative, the width of the channel decreases until no more current flows between the Drain and the Source and the FET is said to be "pinched-off" (similar to the cut-off region for a BJT). The voltage at which the channel closes is called the "pinch-off voltage", (V_P).

JFET Channel Pinched-off



In this pinch-off region the Gate voltage, V_{GS} controls the channel current and V_{DS} has little or no effect.

JFET Model



The result is that the FET acts more like a voltage controlled resistor which has zero resistance when V_{GS} = 0 and maximum "ON" resistance (R_{DS}) when the Gate voltage is very negative. Under normal operating conditions, the JFET gate is always negatively biased relative to the source.

It is essential that the Gate voltage is never positive since if it is all the channel current will flow to the Gate and not to the Source, the result is damage to the JFET. Then to close the channel:

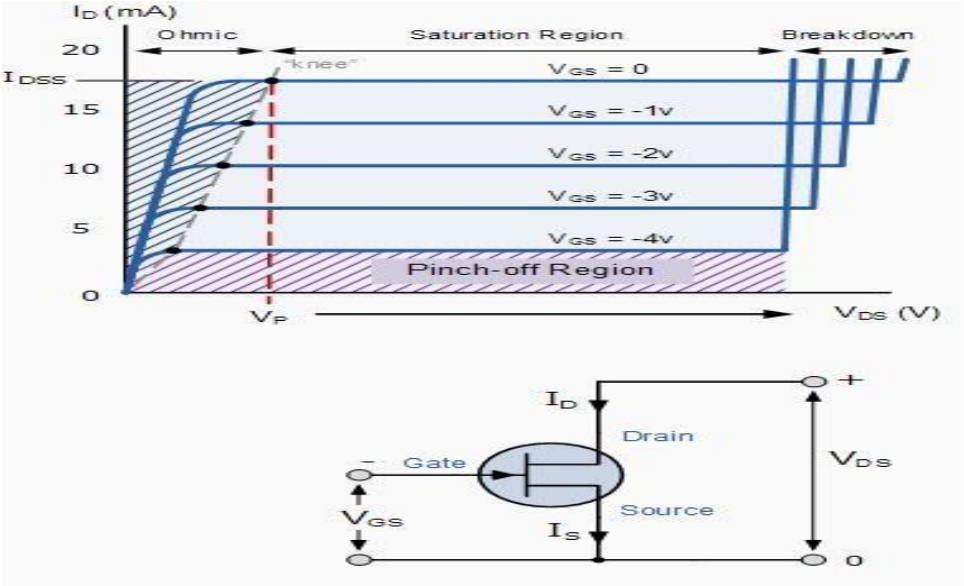
No Gate voltage (V_{GS}) and V_{DS} is increased from zero.

No V_{DS} and Gate control is decreased negatively from zero.

V_{DS} and V_{GS} varying.

The P-channel **Junction Field Effect Transistor** operates the same as the N-channel above, with the following exceptions: 1). Channel current is positive due to holes, 2). The polarity of the biasing voltage needs to be reversed.

The output characteristics of an N-channel JFET with the gate short-circuited to the source is given as



The Output characteristic V-I curves of a typical junction FET?

The voltage V_{GS} applied to the Gate controls the current flowing between the Drain and the Source terminals. V_{GS} refers to the voltage applied between the Gate and the Source while V_{DS}

refers to the voltage applied between the Drain and the Source. Because a **Junction Field Effect Transistor** is a voltage controlled device, "NO current flows into the gate!" then the Source current (I_S) flowing out of the device equals the Drain current flowing into it and therefore ($I_D = I_S$).

The characteristics curves for a P-channel junction field effect transistor are the same as those above, except that the Drain current I_D decreases with an increasing positive Gate-Source voltage, V_{GS}.

The Drain current is zero when $V_{GS} = V_P$. For normal operation, V_{GS} is biased to be somewhere between V_P and 0. Then we can calculate the Drain current, I_D for any given bias point in the saturation or active region as follows:

Drain current in the active region.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

Note that the value of the Drain current will be between zero (pinch-off) and I_{DSS} (maximum current). By knowing the Drain current I_D and the Drain-Source voltage V_{DS} the resistance of the channel (I_D) is given as:

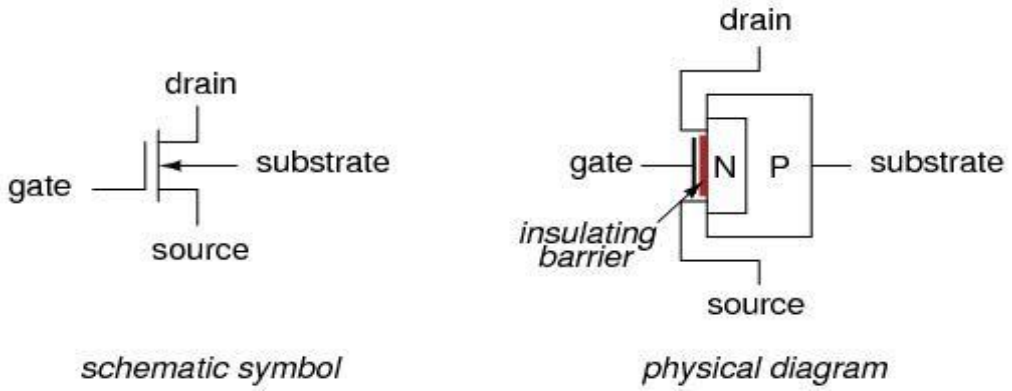
Where: g_m is the "trans conductance gain" since the JFET is a voltage controlled device and which represents the rate of change of the Drain current with respect to the change in Gate- Source voltage.

Working of Insulated Gate Field Effect transistor(IGFET) or MOSFET in depletion mode?

Insulated gate field-effect transistors are Unipolar devices just like JFETs: that is, the controlled current does not have to cross a PN junction. There is a PN junction inside the transistor, but its only purpose is to provide that non-conducting depletion region which is used to restrict current through the channel.

Here is a diagram of an N-channel IGFET of the "depletion" type:

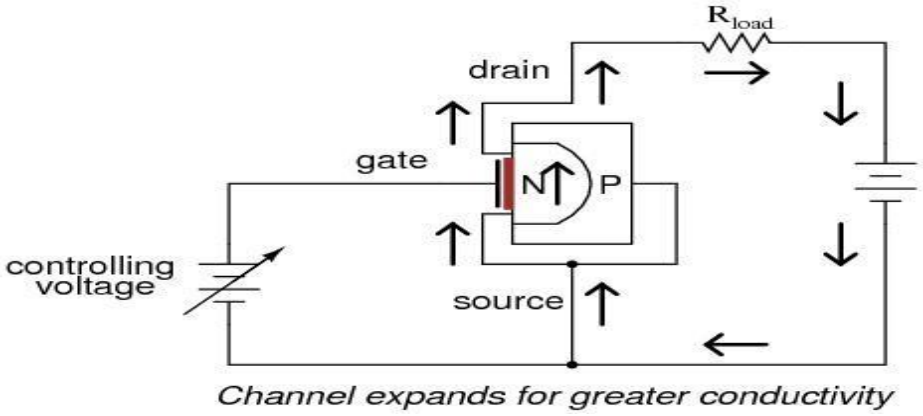
***N-channel, D-type* IGFET**



Notice how the source and drain leads connect to either end of the N channel, or how the gate lead attaches to a metal plate separated from the channel by a thin insulating barrier. That barrier is sometimes made from silicon dioxide (the primary chemical compound found in sand), which is a very good insulator. Due to this **M**etal (gate) - **O**xide (barrier) - **S**emiconductor (channel) construction, the IGFET is sometimes referred to as a MOSFET. There are other types of IGFET construction, though, and so "IGFET" is the better descriptor for this general class of transistors. Notice also how there is four connections to the IGFET. In practice, the *substrate* lead is directly connected to the *source* lead to make the two electrically common.

With source and substrate common to each other, the N and P layers of the IGFET end up being directly connected to each other through the outside wire. This connection prevents any voltage from being impressed across the PN junction. As a result, a depletion region exists between the two materials, but it can never be expanded or collapsed. JFET operation is based on the expansion of the PN junction's depletion region, but here in the IGFET that cannot happen, so IGFET operation must be based on a different effect. Indeed it is, for when a controlling voltage is applied between gate and source, the conductivity of the channel is changed as a result of the depletion region *moving* closer to or further away from the gate. In other words, the channel's effective width changes just as with the JFET, but this change in channel width is due to depletion region *displacement* rather than depletion region *expansion*.

In an N-channel IGFET, a controlling voltage applied positive (+) to the gate and negative (-) to the source has the effect of repelling the PN junction's depletion region, expanding the N-type channel and increasing conductivity:



Channel expands for greater conductivity

Reversing the controlling voltage's polarity has the opposite effect, attracting the depletion region and narrowing the channel, consequently reducing channel conductivity: The insulated gate allows for controlling voltages of any polarity without danger of forward-biasing a junction, as was the concern with JFETs. This type of IGFET, although it's called a "depletion-type," actually has the capability of having its channel *either* depleted (channel narrowed) *or* enhanced (channel expanded). Input voltage polarity determines which way the channel will be influenced.

If the IGFET is an N-channel and the input voltage is connected so that the positive (+) side is on the gate while the negative (-) side is on the source, the channel will be enhanced as extra electrons build up on the channel side of the dielectric barrier. Think, "negative (-) correlates with *N*-type, thus enhancing the channel with the right type of charge carrier (electrons) and making it more conductive." Conversely, if the input voltage is connected to an N-channel IGFET the other way, so that negative (-) connects to the gate while positive (+) connects to the source, free electrons will be "robbed" from the channel as the gate-channel capacitor charges, thus depleting the channel of majority charge carriers and making it less conductive.

For P-channel IGFETs, the input voltage polarity and channel effects follow the same rule. That is to say, it takes just the opposite polarity as an N-channel IGFET to either deplete or enhance:

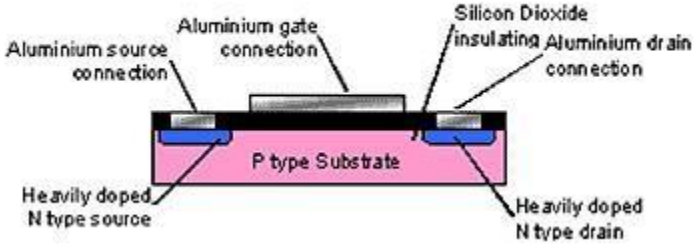
Explain about the Enhancement Mode MOSFET ?

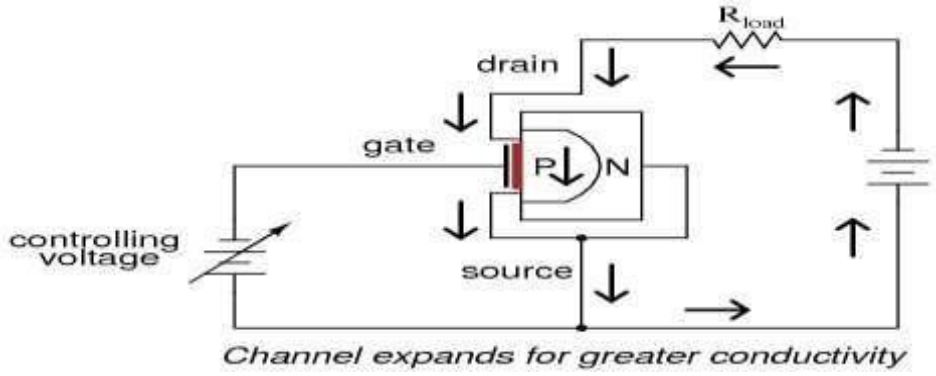
The Metal Oxide Silicon FET (MOSFET) or Metal Oxide Silicon Transistor (M.O.S.T.) has an even higher input resistance (typically 10^{12} to 10^{15} ohms) than that of the JFET. In this device the gate is completely insulated from the rest of the transistor by a very thin layer of metal oxide (Silicon dioxide SiO_2). Hence the general name applied to any device of this type, the IGFET or Insulated Gate FET.

Construction

The layers are laid down one by one, by diffusing various semiconductor materials with suitable doping levels and layers of insulation into the surface of the device under carefully controlled conditions at high temperatures. Parts of a layer may be removed by etching using photographic masks to make the required pattern of the electrodes etc. before the next layer is

added. The insulating layers are made by laying down very thin layers of silicon dioxide; conductors are created by evaporating a metal such as aluminum on to the surface. The transistors produced in this way have a much higher quality than is possible using other methods, and many transistors can be produced at one time on a single slice of silicon, before the silicon slice is cut up into individual transistors or integrated circuits.



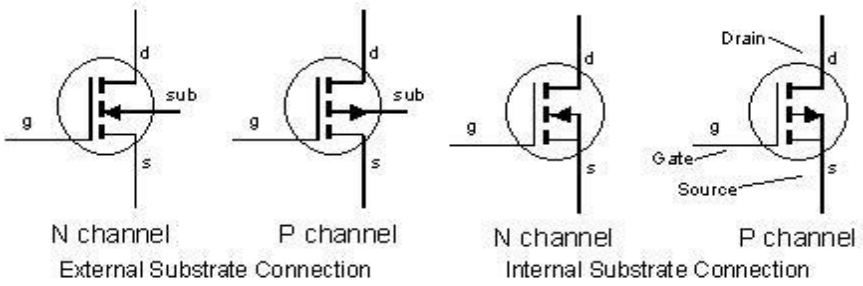


Construction of a N Channel Enhancement Mode MOSFET

The gate has a voltage applied to it that makes it positive with respect to the source. This causes holes in the P type layer close to the silicon dioxide layer beneath the gate to be repelled down into the P type substrate and at the same time this positive potential on the gate attracts free electrons from the surrounding substrate material. These free electrons form a thin layer of charge carriers beneath the gate electrode (they can't reach the gate because of the insulating silicon dioxide layer) bridging the gap between the heavily doped source and drain areas. This layer is sometimes called an "inversion layer" because applying the gate voltage has caused the P type material immediately under the gate to firstly become "intrinsic" (with hardly any charge carriers) and then an N type layer within the P type substrate.

Any further increase in the gate voltage attracts more charge carriers into the inversion layer, so reducing its resistance and increasing current flow between source and drain. Reducing the gate source voltage reduces current flow. When the power is switched off of course, the area beneath the gate reverts to P type once more. As well as the type described above, devices having N type substrates and P type (inversion layer)channels are also available. Operation is identical, but of course the polarity if the gate voltage is reversed.

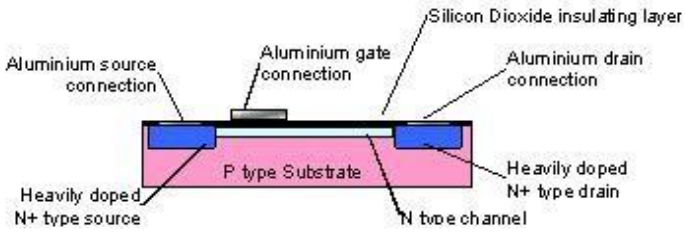
The method of operation described is called "ENHANCEMENT MODE" as the application of gate source voltage makes a conducting channel "grow", therefore it enhances the channel. Other devices are available in which the application of a bias voltage reduces or "depletes" the conducting channel.



Explain the operation of Depletion Mode MOSFET?

Reducing the Conduction Channel

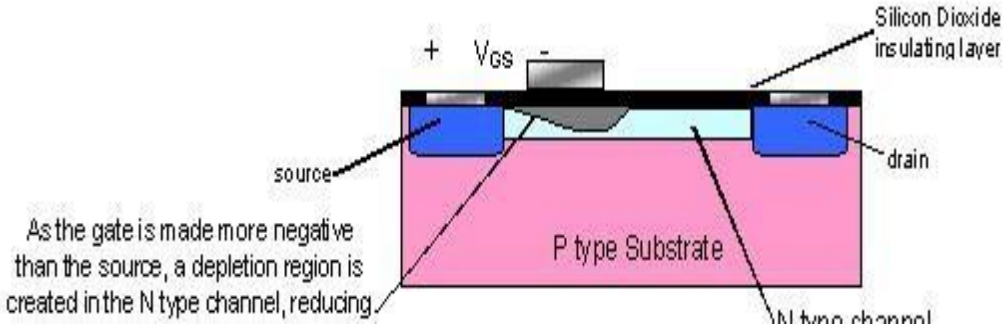
The depletion mode MOSFET shown as a N channel device (P channel is also available) in fig 5.1 is more usually made as a discrete component, i.e. a single transistor rather than IC form. In this device a thin layer of N type silicon is deposited just below the gate-insulating layer, and forms a conducting channel between source and drain. Thus when the gate source voltage VGS is zero, current (in the form of free electrons) can flow between source and drain. Note that the gate is totally insulated from the channel by the layer of silicon dioxide. Now that a conducting channel is present the gate does not need to cover the full width between source and



drain. Because the gate is totally insulated from the rest of the transistor this device, like other IGFETs, has a very high input resistance.

Depletion Mode N Channel MOSFET

In the N channel device, shown in Fig. 5.2 the gate is made negative with respect to the source, which has the effect creating a depletion area free from charge carriers, beneath the gate. This restricts the depth of the conducting channel, so increasing channel resistance and reducing current flow through the device.



Depletion mode MOSFETS are also available in which the gate extends the full width of the channel (from source to drain). In this case it is also possible to operate the transistor in enhancement mode. This is done by making the gate positive instead of negative. The positive voltage on the gate attracts more free electrons into the conducing channel while at the same time repelling holes down into the P type substrate. Thus the more positive the gate potential, the deeper, and lower resistance is the channel. Increasing positive bias thus increases current flow. This useful depletion/enhancement version has the disadvantage that, as the gate area is increased; the gate capacitance is also larger than true depletion types. This may present difficulties at higher frequencies.

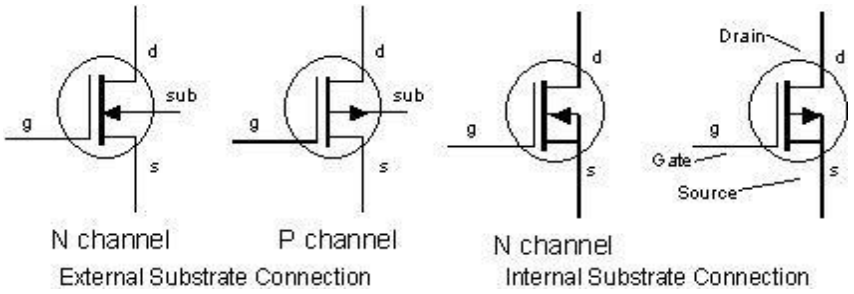


Fig 5.6 Circuit Symbols for Depletion Mode MOSFETs (IGFETs)

Notice the solid bar indicating the presence of a conducting channel between source and drain. Note: Making the gate more negative reduces conduction between source & drain In N channel devices, but increases conduction between source & drain In P channel devices.

Applications of FETs:

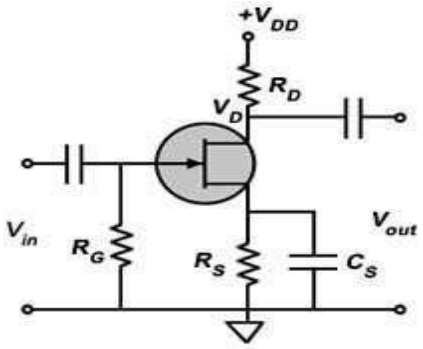
Although FETs have a lower gain than bipolar transistors their very high input impedance makes them suitable for applications where input signals may be severely reduced if applied to a bipolar transistor base, which needs base current to operate. A useful feature of FETs is that they tend to produce less background noise than Bipolar types and so are useful in the initial stages of systems such as amplifiers; radios etc. where signal levels are very small and could be swamped by excessive background noise.

MOSFET Vs JFET?

1) In JFET, the transverse electric field across the reverse biased P Njunction controls the conductivity of the channel. In FET Transverse electric field is induced across the insulating layer.
2) Input impedance of MOS FET is much higher (10^{10} to 10^{15} cmpared to that of JFET (10^{8}) because gate insulated from channel.
3) The output characteristics of JFET are flatter than that of MOS FET because drain resistance of JFET is much higher than MOS FET.
4) JFET is operated in depletion mode only where as MOSFET can be operated in
   depletion and enhancement mode.
5) MOSFET are easier to fabricate than JFET
6) MOSFETs are easily get damaged due to static change
7) In MOSFET source and drain can be interchanged
8) CMOSFETs dissipates very low power
9) MOS FETs are widely used in VLSI.

Common Source JFET Amplifier

Small signal amplifiers can also be made using **Field Effect Transistors** or **FET's** . These devices have the advantage over bipolar transistors of having extremely high input impedance along with a low noise output making them ideal for use in amplifier circuits that have very small input signals. The design of an amplifier circuit based around a junction field effect transistor or "JFET", (n-channel FET) or even a metal oxide silicon FET or "MOSFET" is exactly the same principle as that for the bipolar transistor circuit. Firstly, a suitable quiescent point or "Q-point" needs to be found for the correct biasing of the JFET amplifier circuit with single amplifier configurations of Common-source (CS), Common-drain (CD) or Source-follower (SF) and the Common-gate (CG) available for most FET devices. These three JFET amplifier configurations correspond to the common-emitter, emitter-follower and the common-base configurations using bipolar transistors. The **Common Source JFET Amplifier** as this is the most widely used JFET amplifier design. The common source JFET amplifier circuit is shown below.



Common Sorce JFET Amplifier

The amplifier circuit consists of an N-channel JFET, connected in a common source configuration. The JFET gate voltage Vg is biased through the potential divider network set up by resistors R1 and R2 and is biased to operate within its saturation region which is equivalent to the active region of the bipolar junction transistor. Unlike a bipolar transistor circuit, the junction FET takes virtually no input gate current allowing the gate to be treated as an open circuit. Then no input characteristics curves are required. Since the N-Channel JFET is a depletion mode device and is normally "ON", a negative gate voltage with respect to the source is required to modulate or control the drain current. This negative voltage can be provided by biasing from a separate power supply voltage or by a self biasing arrangement as long as a steady current flow through the JFET even when there is no input signal present and Vg maintains a reverse bias of the gate- source pn junction.

Any suitable pair of resistor values in the correct proportions would produce the correct biasing voltage so the DC gate biasing voltage Vg is given as:

$$V_G = \frac{V_{DD} R_2}{R_1 + R_2} = V_{DD}\left(\frac{R_2}{R_1 + R_2}\right)$$

The input signal, (Vin) of the common source JFET amplifier is applied between the Gate terminal and the zero volts rail, (0v). With a constant value of gate voltage Vg applied the JFET operates within its "Ohmic region" acting like a linear resistive device. The drain circuit contains the load resistor, Rd. The output voltage, Vout is developed across this load resistance. The efficiency of the common source JFET amplifier can be improved by the addition of a resistor, Rs included in the source lead with the same drain current flowing through this resistor. Resistor, Rs is also used to set the JFET amplifiers "Q-point".

When the JFET is switched fully "ON" a voltage drop equal to Rs x Id is developed across this resistor raising the potential of the source terminal above 0v or ground level. This voltage drop across Rs due to the drain current provides the necessary reverse biasing condition across the gate resistor, R2 effectively generating negative feedback. In order to keep the gate-source junction reverse biased, the source voltage, Vs needs to be higher than the gate voltage, Vg. This source voltage is therefore given as:

$$V_S = I_D \times R_S = V_G - V_{GS}$$

Then the Drain current, Id is also equal to the Source current, Is as "No Current" enters the Gate terminal and this can be given as:

$$I_D = \frac{V_S}{R_S} = \frac{V_{DD}}{R_D + R_S}$$

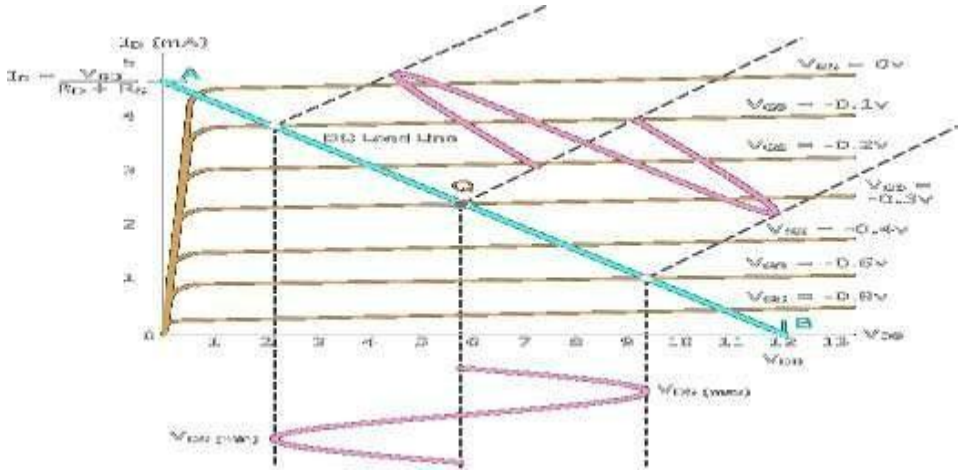
This potential divider biasing circuit improves the stability of the common source JFET amplifier circuit when being fed from a single DC supply compared to that of a fixed voltage biasing circuit. Both resistor, Rs and the source by-pass capacitor, Cs serve basically the same function as the emitter resistor and capacitor in the common emitter bipolar transistor amplifier circuit, namely to provide good stability and prevent a reduction in the loss of the voltage gain. However, the price paid for a stabilized quiescent gate voltage is that more of the supply voltage is dropped across Rs.

The basic circuit and characteristics of a **Common Source JFET Amplifier** are very similar to that of the common emitter amplifier.

Common Source JFET Amplifier Characteristics Curves

As with the common emitter bipolar circuit, the DC load line for the common source JFET amplifier produces a straight line equation whose gradient is given as: -1/(Rd + Rs) and that it crosses the vertical Id axis at point A equal to Vdd/(Rd + Rs). The other end of the load line crosses the horizontal axis at point B which is equal to the supply voltage, Vdd. The actual position of the Q-point on the DC load line is generally positioned at the mid centre point of the load line (for class-A operation) and is determined by the mean value of Vg which is biased negatively as the JFET is a depletion-mode device. Like the bipolar common emitter amplifier the output of the **Common Source JFET Amplifier** is 180^o out of phase with the input signal.

One of the main disadvantages of using Depletion-mode JFET is that they need to be negatively biased. Should this bias fail for any reason the gate-source voltage may rise and become positive causing an increase in drain current resulting in failure of the drain voltage, Vd. Also the high channel resistance, Rds(on) of the junction FET, coupled with high quiescent steady state drain current makes these devices run hot so additional heatsink is required. However, most of the problems associated with using JFET's can be greatly reduced by using enhancement-mode MOSFET devices instead.



MOSFETs or Metal Oxide Semiconductor FET's have much higher input impedances and low channel resistances compared to the equivalent JFET. Also the biasing arrangements for MOSFETs are different and unless we bias them positively for N-channel devices and negatively for P-channel devices no drain current will flow

Common Gate amplifier

A **common-gate** amplifier is one of three basic single-stage field-effect transistor (FET) amplifier topologies, typically used as a current buffer or voltage amplifier. In this circuit the source terminal of the transistor serves as the input, the drain is the output and the gate is common to both, hence its name. The analogous bipolar junction transistor circuit is the common-base amplifier.

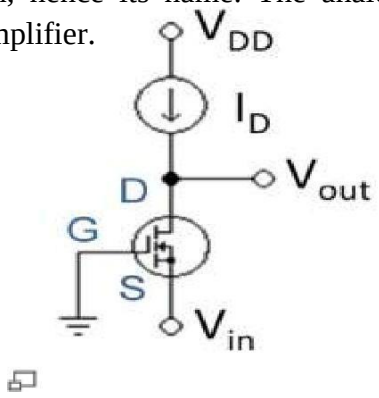


Figure 1: Basic N-channel common-gate circuit (neglecting biasing details); current source I_D represents an active load; signal is applied at node V_{in} and output is taken from node V_{out}; output can be current or voltage

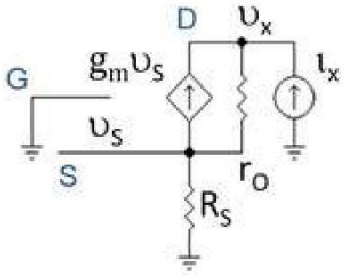


Figure 2: Hybrid pi model with test source i_x at output to find output resistance

The amplifier characteristics are summarized below in Table 1. The approximate expressions use the assumptions (usually accurate) $r_O >> R_L$ and $g_m r_O >> 1$.

In general the overall voltage/current gain may be substantially less than the open/short circuit

gains listed above (depending on the source and load resistances) due to the loading effect.
Closed circuit voltage gain Taking input and output loading into consideration, the closed circuit voltage gain (that is, the gain with load R_L and source with resistance R_S both attached) of the common gate can be written as:

$$A_{\mathrm{v}} \approx \frac{g_m R_{\mathrm{L}}}{1+g_m R_S},$$

Which has the simple limiting forms

$$A_{\mathrm{v}} = \frac{R_L}{R_S} \quad \text{or} \quad A_{\mathrm{v}} = g_m R_L,$$

Depending upon whether $g_m R_S$ is much larger or much smaller than one.
In the second case $R_S << 1/g_m$ and the Thévenin representation of the source is useful, producing the second form for the gain, typical of voltage amplifiers. Because the input impedance of the common-gate amplifier is very low, the cascode amplifier often is used instead. The cascode places a common-source amplifier between the voltage driver and the common-gate circuit to permit voltage amplification using a driver with $R_S >> 1/g_m$.

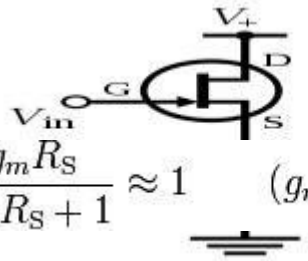
Common Drain amplifier or Source Follower.

A **common-drain** amplifier, also known as a **source follower**, is one of three basic single-stage field effect transistor (FET) amplifier topologies, typically used as a voltage buffer. In this circuit the gate terminal of the transistor serves as the input, the source is the output, and the drain is common to both (input and output), hence its name. The analogous bipolar junction transistor circuit is the common-collector amplifier. This circuit is used to transform impedances.

Basic N-channel JFET source follower circuit (neglecting biasing details).

At low frequencies, the source follower has the following small signal characteristics

Voltage gain:



$$A_{\mathrm{v}} = \frac{v_{\mathrm{out}}}{v_{\mathrm{in}}} = \frac{g_m R_{\mathrm{S}}}{g_m R_{\mathrm{S}} + 1} \approx 1 \qquad (g_m R_{\mathrm{S}} \gg 1)$$

Current gain:

Input impedance:

$$A_{\mathrm{i}} = \infty$$

$$r_{\mathrm{in}} = \infty$$

Output impedance:

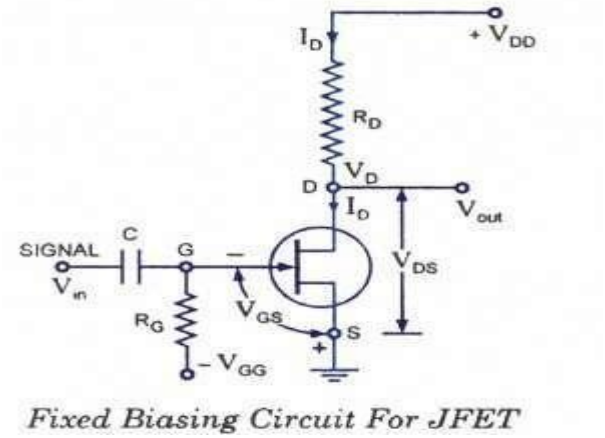
$$r_{\mathrm{out}} = R_{\mathrm{S}} \| \frac{1}{g_m} = \frac{\frac{R_{\mathrm{S}}}{g_m}}{R_{\mathrm{S}} + \frac{1}{g_m}} = \frac{R_{\mathrm{S}}}{g_m R_{\mathrm{S}} + 1} \approx \frac{1}{g_m} \qquad (g_m R_S \gg 1)$$

The variable g_m that is not listed in Figure 1 is the trans conductance of the device (usually given in units of Siemens.

FET Biasing methods:

Unlike BJTs, thermal runaway does not occur with FETs. However, the wide differences in maximum and minimum **transfer characteristics** make I_D levels unpredictable with simple fixed-gate bias voltage. To obtain reasonable limits on quiescent drain currents I_D and drain- source voltage V_{DS}, source resistor and potential divider bias techniques must be used. With few exceptions, MOSFET bias circuits are similar to those used for **JFET**s. Various FET biasing circuits are discussed below

Fixed Bias:



Fixed Biasing Circuit For JFET

DC bias of a FET device needs setting of gate-source voltage V_{GS} to give desired drain current I_D . For a JFET drain current is limited by the saturation current I_{DS}.

FET has such a high input impedance that no gate current flows and the dc voltage of the gate set by a voltage divider or a fixed battery voltage is not affected or loaded by the FET.

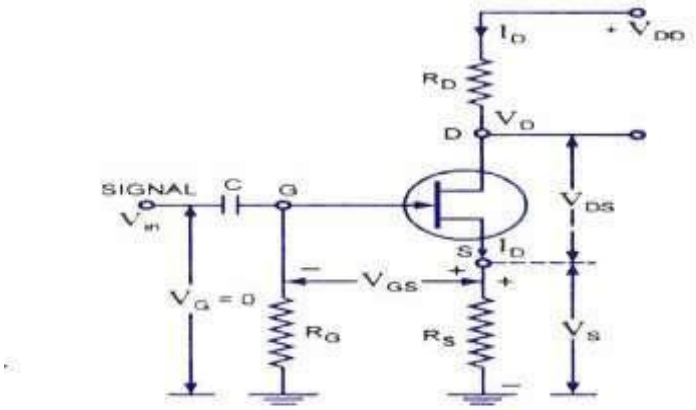
Fixed dc bias is obtained using a battery V_{QG}. This battery ensures that the gate is always negative with respect to source and no current flows through resistor R_G and gate terminal that is I_G =0. The battery provides a voltage V_{GS} to bias the N-channel JFET, but no resulting current is drawn from the battery V_{GG}. Resistor R_G is included to allow any ac signal applied through capacitor C to develop across R_G. While any ac signal will develop across R_G, the dc voltage drop across R_G is equal to $I_G R_G$ *i.e.* 0 volt.

The gate-source voltage V_{GS} is then

V_{GS} = - V_G – V_S = – V_{GG} – 0 = – V_{GG}The drain -source current I_D is then fixed by the gate-source voltage as determined by equation.

This current then causes a voltage drop across the drain resistor R_D and is given as $V_{RD} = I_D R_D$ and output voltage , Vout = $V_{DD} – I_D R_D$

Self-Bias.



Self-Bias Circuit For N-Channel JFET

This is the most common method for biasing a JFET. Self-bias circuit for N-channel JFET is shown in figure.

Since no gate current flows through the reverse-biased gate-source, the gate current $I_G = 0$ and, therefore, $v_G = i_G R_G = 0$ With a drain current I_D the voltage at the S is $V_s = I_D R_s$

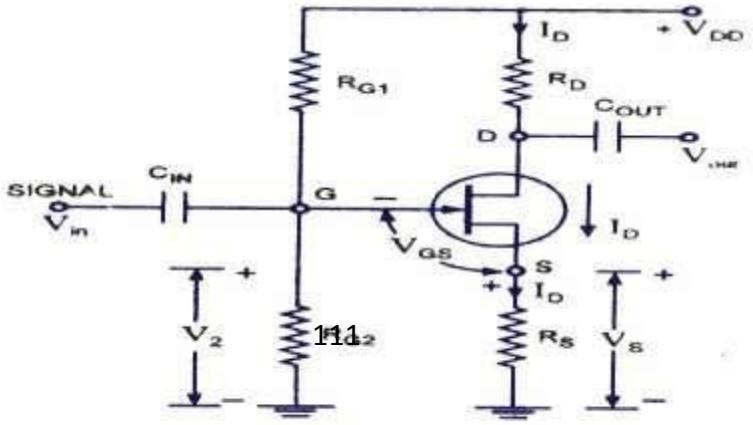
The gate-source voltage is then $V_{Gs} = V_G - V_s = 0 – I_D R_s = – I_D R_s$

So voltage drop across resistance R_s provides the biasing voltage V_{Gg} and no external source is required for biasing and this is the reason that it is called self-biasing.

The operating point (i.e zero signal I_D and V_{DS}) can easily be determined from equation and equation given below
VDS = VDD – ID **(**RD + RS)

Thus dc conditions of JFET amplifier are fully specified. Self biasing of a JFET stabilizes its quiescent operating point against any change in its parameters like trans conductance. Let the given JFET be replaced by another JFET having the double conductance then drain current will also try to be double but since any increase in voltage drop across R_s, therefore, gate-source voltage, V_{GS} becomes more negative and thus increase in drain current is reduced.

Potential-Divider Biasing.



Potential-Divider Bias Circuit For N-Channel JFET

A slightly modified form of dc bias is provided by the circuit shown in figure. The resistors R_{Gl} and R_{G2} form a potential divider across drain supply V_{DD}. The voltage V_2 across R_{G2} provides the necessary bias. The additional gate resistor R_{Gl} from gate to supply voltage facilitates in larger adjustment of the dc bias point and permits use of larger valued R_S.

The gate is reverse biased so that $I_G = 0$ and gate voltage

$V_G = V_2 = (V_{DD}/R_{G1} + R_{G2}) * R_{G2}$ And $V_{GS} = V_G - V_S = V_G - I_D R_S$

The circuit is so designed that ID, Rs is greater than VD so that VGS is negative. This provides correct bias voltage.

The operating point can be determined as

$I_D = (V_2 - V_{GS})/ R_S$

And

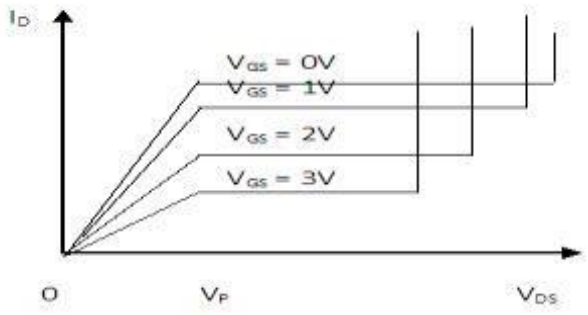
$V_{DS} = V_{DD} - I_D (R_D + R_S)$

FET AS A VOLTAGE –VARIABLE RESISTOR (VVR):

FET is operated in the constant current portion of its output characteristics for the linear applications .In the region before pinch off , where Vds is small the drain to source resistance rd can be controlled by the bias voltage Vgs.The FET is useful as a voltage variable resistor (VVR) or Voltage Dependent resistor.

In JFET the drain source conductance gd = Id/Vds for small values of Vds which may be expressed as gd = gdo [1-(VgsVp)$^{1/2}$] where gdo is the value of drain conductance when the bias voltage Vgs is zero.Small signal FET drain resistance rd varies with applied gate voltage Vgs and FET act like a VARIABLE PASSIVE RESISTOR.

When $V_{DS} < V_P$, Id V_{DS}, when V_{GS} is constant. i.e., FET acts as a resistor.In this region FET is used as a Voltage controlled resistor. Or Voltage variable resistor. Or Voltage dependant resistor.



Differences between BJT and FET

- FET is unipolar device – current I_D is due to majority (Where as BJT is Bipolar) charge carries only.
- FET is less noisy as there are no junctions(in conduction channel) FET
- FET Input impedance is very high (100 M) (due to reverse bias)
- FET is voltage controlled device, BJT is current controlled device
- FETs are easy to fabricate
- FET performance does not change much with temperature. FET has –Ve temp. Coefficient, BJT has +Ve temp. coefficient.
- FET has higher switching speeds
- FET is useful for small signal operation only
- BJT is cheaper than FET