COURSE FILE

ON

PULSE AND DIGITAL CIRCUITS

Department of ECE

CMR COLLEGE OF ENGINEERING & TECHNOLOGY

PULSE AND DIGITAL CIRCUITS

COURSE FILE INDEX

INDEX

	1.4.2	Pulse Input Voltage	
	1.4.3	Square Wave Input Voltage	
	1.4.4	Ramp input voltage	
	1.4.5	Sinusoidal Input	
	1.4.6	Low Pass RC Circuit as an Integrator	
	1.5	High pass RL circuit	
	1.5.1	Step Input Voltage	
	1.6	Attenuators	
	1.6.1	Application of Attenuator as a CRO Probe	
	1.7	RL Circuits	
	1.8	RLC Circuits	
	1.8.1	RLC Series Circuit	
	1.9	Ringing Circuit	
UNIT-2		NON-LINEAR WAVE SHAPING	
	2.1	Introduction	
	2.2	Clipping Circuits	
	2.2.1	Series Clipper	
	2.2.2	Parallel Clipper	

	2.2.3	Diode Clippers	
	2.2.4	Positive Clipper and Negative Clipper	
	2.2.4.1	Positive Diode Clipper	
	2.2.4.2	Negative Diode Clipper	
	2.2.5	Biased Positive Clipper and Biased Negative Clipper	
	2.2.6	Combination Clipper	
	2.2.7	Drawbacks of Series and Shunt Diode Clippers	
	2.3	Transistor Clipping Circuits	
	2.3.1	Emitter Coupled Clipper	
	2.3.2	Diode Clipper Applications	
	2.4	Voltage Comparators	
	2.5	Applications Of Comparator	
	2.5.1	Null detector	
	2.5.2	Zero-crossing detector	
	2.5.3	Relaxation oscillator	
	2.5.4	Level shifter	
	2.5.5	Analog-to-digital converter	
	2.6	Diode Clampers	

	2.7	Clamping Circuit Theorem	
	2.8	Practical Clamping Circuits	
	2.8.1	Effect Of Vγ Of Diode On Clamping Circuit	
	2.9	Effect of Diode Characteristics on Clamping Circuit	
	2.10	Synchronized Clamping	
UNIT-3		SWITCHING CHARACTERISTICS OF DEVICES	
	3.1	Switching Characteristics Of A Diode	
	3.2	Diode As A Switch	
	3.3	Piece-Wise Linear Diode Characteristics	
	3.4	Switching Times In A Diode	
	3.4.1	Forward Recovery Time	
	3.4.2	Reverse Recovery Time	
	3.5	Breakdown In P-N Junction Diodes	
	3.5.1	Avalanche Breakdown	
	3.5.2	Zener Breakdown	
	3.6	Transistor As A Switch	
	3.6.1	Transistor Switching Times	
	3.6.2	The Delay Time	

	3.6.3	Rise Time And Fall Time	
	3.6.4	Storage Time	
	3.7	Breakdown Voltages Of A Transistor	
	3.8	Temperature Sensitivity Of Saturation Parameters	
	3.9	Silicon-Controlled –Switch Circuits	
UNIT-4		MULTIVIBRATORS	
	4.1	Introduction	
	4.1.1	Basic Configuration Of A Multivibrator	
	4.2	Astable Multivibrator Using Transistor	
	4.2.1	Operation	
	4.3	Monostable Multivibrator	
	4.3.1	Operation	
	4.4	Bistable Multivibrator	
	4.5	Triggering In Multivibrators	
	4.6	Schmitt Trigger	
	4.6.1	Fundamental Idea	
	4.6.2	Modified Input Voltage (Parallel Feedback)	
	4.6.3	Schmitt Triggers Using Transistor	

	4.6.4	Collector-Base Coupled Circuit	
	4.6.5	Comparison Between Emitter- And Collector-Coupled Circuits	
UNIT-5		TIME BASE GENERATORS	
	5.1	Introduction	
	5.2	General Features Of time-base Signa1	
	5.3	Methods of generating time base waveforms	
	5.4	Miller and Boot strap sweep circuit	
	5.5	Miller time base and bootstrap time base	
	5.6	Current time base generator	
	5.7	Linearization using const current circuit	
UNIT-6		SAMPLING GATES	
	6.1	Introduction	
	6.2	Basic Operating Principle of Sampling Gates	
	6.3	Unidirectional Sampling Gates	
	6.4	Bidirectional Sampling Gate using Transistor	
	6.5	Four Diode Sampling Gate	
	6.6	Reduction of Pedestal in Gate Circuits	

	6.7	Six Diode Gate	
	6.8	Applications of Sampling Gates	
UNIT-7		SYNCHRONIZATION AND FREQUENCY DIVISION	
	7.1	Introduction	
	7.2	Pulse Synchronization of Relaxation Devices	
	7.3	Frequency Division in the UJT Sweep	
	7.4	Astable Multivibrator	
	7.5	Monostable Relaxation Circuit	
	7.6	Stability of Relaxation Dividers	
	7.7	Synchronization of a sweep circuits with Sinusoidal Signals	
UNIT-8		*REALIZATION OF LOGIC GATES USING DIODES & TRANSISTORS*	
	8.1	Introduction to Digital Logic Gates	
	8.2	Two Input AND Gate using diodes with Truth table	
	8.3	Two Input OR Gate Using Diodes with Truth table	
	8.4	Basic NOT Gate Using Transistor	
	8.5	Different logic families	
	8.6	CML Logic Families and its Comparison	

PULSE AND DIGITAL CIRCUITS

SYLLABUS

Unit-I

Linear Wave Shaping: High pass and low pass RC circuits and their response for Sinusoidal, Step, Pulse, Square & Ramp inputs, High pass RC network as Differentiator, Low pass RC circuit as an Integrator, Attenuators and its application as a CRO Probe, RL and RLC Circuits and their response for step Input, Ringing Circuit.

Unit-II

Non-Linear Wave Shaping: Diode clippers, Transistor Clippers, Clipping at two independent levels, Comparators, Applications of Voltage comparators. Clamping Operation, Clamping circuit taking Source and Diode resistances into account, Clamping Circuit Theorem, Practical Clamping Circuits, Effect of Diode Characteristics on Clamping Voltage, Synchronized Clamping.

Unit-III

Switching Characteristics of Devices: Diode as Switch, Piecewise Linear Diode Characteristics, Diode Switching times, Transistor as a Switch, Breakdown voltages, Transistor in Saturation, Temperature variation of Saturation Parameters, Transistor-switching times, Silicon-controlled –switch circuits.

Unit-IV

Multivibrators: Analysis and Design of Bi-stable, Mono-stable, Astable Multivibrators and Schmitt trigger using Transistors.

Unit-V

Time Base Generators: General features of a Time base signal, Methods of Generating Time Base Waveform, Miller and Bootstrap Time Base Generators-Basic Principles, Transistor Miller Time Base generator, Transistor Bootstrap Time base Generator, Transistor Current Time Base Generators, Methods of Linearity improvement.

Unit-VI

Sampling Gates: Basic operating principles of Sampling Gates, Unidirectional and Bi-directional sampling Gates, Four Diode Sampling Gate, Reduction of pedestal in gate Circuits, Six Diode Gate, and Application of Sampling Gates.

Unit-VII

Synchronization and Frequency Division: Pulse Synchronization of Relaxation Devices, Frequency division in Sweep Circuit, Stability of Relaxation Devices, Astable Relaxation Circuits, Monostable Relaxation Circuits, Synchronization of a Sweep Circuit with Symmetrical Signals, Sine wave frequency division with a Sweep Circuit, A Sinusoidal Divider using Regeneration and Modulation.

Unit-VIII

Realization of Logic Gates Using Diodes & Transistors: AND, OR and NOT Gates using Diodes and Transistors, DCTL, RTL, DTL, TTL and CML Logic Families and its Comparison.

COURSE OBJECTIVE

This course helps in understanding the generation and processing of non sinusoidal waveforms. The switching mode of operation can also be analyzed. This subject gives us an idea or overview to transmit the signal from one location to another, to amplify it, to select a portion of it in voltage, to choose a section of it in time, to combine it with other signal in order to perform a logic operation, to use it to synchronize a system and so orth.

COURSE TITLE: ECE-PULSE and DIGITAL CIRCUITS

EVEN SEMESTER: II B.TECH (ECE)

NUMBER OF CREDITS: 4

2012-13 CATALOG DATA:

1. Linear Wave Shaping
2. Non- Linear Wave Shaping
3. Switching Characteristics of Devices
4. Multivibrators
5. Time Base Generators
6. Sampling Gates
7. Synchronization and Frequency Division
8. Realization of Logic Gates Using Diodes & Transistors

TEXT BOOKS:

REFERENCES:

COORDINATOR/INSTRUCTOR:

COURSE GOALS:

EVALUATION METHODS:

1. Quiz 1:20%
2. Quiz 2:20%

*Average of quiz marks is taken

3. Final exam: 80%

PROFESSIONAL COMPONENT:

1. Engineering topics:70%
2. General education: 0%
3. Mathematics and basic sciences:30%

PREREQUISITES:

COMPUTER USAGE:

INSTRUCTIONAL OBJECTIVES:

PROGAMME OUTCOMES:

COURSE / LABORATORY SHEDULE:

PULSE AND DIGITAL CIRCUITS

ABOUT THE COURSE

In this Course students will learn about:

The subject is concerned with the generation and processing of non sinusoidal waveforms.

Most non sinusoidal waveforms that appear regularly are step, ramp, pulse, and square, exponential. The responses to there of RC, RL, RLC circuits are discussed in Chapter 1.

Basic functions such as clipping, clamping, comparators, generation of square wave or pulse waveforms are studied in chapter 2.

Chapter 3 discuss about switching characteristics of diode and transistor.

Memory is the basic requirement of all computers. The basic memory element is a flip-flop i.e. the bistable multivibrator.The various types of multivibrators are discussed in chapter 4.

Time base generators are essential for display of signals on the screen. Voltage and current time base generators, about time base generators which have applications in radar and TV indicators, CRO etc.are presented in Chapter 5.

Synchronization and frequency division of various generators with pulse type as well as symmetrical signals are the topics in Chapter 6.

When signals are to be transmitted only for specified intervals of time and are to be blocked during other intervals of time, we require sampling gates. Various types of sampling gates are explained in Chapter 7.

Chapter 8 discusses about basic logic gates which are basic building blocks of any digital system and also realization of logic gates using diodes and transistors is discussed. Various types of logic families are also discussed.

COURSE PLAN

Course Plan for the Academic Year -2010

SUB: PULSE AND DIGITAL CIRCUITS **YEAR:** II B.Tech –I I SEM

BRANCH: ECE

UNIT-I: Linear Wave Shaping

Sl. No.	Topic	No. of periods	Cumulative periods	Completed date
1	High Pass RC circuit, HPRC circuit act as Differentiator	1	1	
2	Response of HPRC circuit to Step input, Pulse input, Square input, Ramp input	3	4	
3	Low Pass RC circuit, LPRC circuits act as Integrator	1	5	
4	Response of LPRC circuits to Step input, Pulse input, Square input, Ramp input	3	8	
5	Attenuators, its application in CRO probe, RL and RLC circuits and their res for Step input, Ringing circuit, problems	2	10	
6	Review	1	11	

7	Unit Test-I	1	12	

UNIT-II: Non Linear Wave Shaping

Sl. No.	Topic	No. of periods	Cumulative periods	Completed date
1	Diode clippers, Transistor clippers, Clipping at two independent levels, problems	3	15	
2	Transfer chars of clippers, Emitter coupled clippers	2	17	
3	Comparators, Applications of Voltage comparators	1	18	
4	Clamping operation, Clamping circuit using diode with different i/ps	2	20	
5	Clamping circuit theorem, Practical clamping circuits, problems	1	21	
6	Effect of diode characteristics on clamping voltage, Transfer chars of clampers	1	22	
7	Review	1	23	
8	Unit Test-II	1	24	

UNIT-III: Switching Characteristics of Devices

Sl. No.	Topic	No. of periods	Cumulative periods	Completed date
1	Diode as a Switch, piecewise linear diode characteristics	1	25	
2	Transistor as a Switch, Break down voltage consideration of Transistor,	1	26	
3	Saturation parameters of Transistor and their variation with temperature	1	27	
4	Design of transistor switch, transistor-switching times	1	28	
5	Review	1	29	
6	Unit Test-III	1	30	

UNIT-IV: Multivibrators

Sl. No.	Topic	No. of periods	Cumulative periods	Completed date
1	Analysis and Design of Bistable multivibrator ,problems	2	32	

2	Monostable multivibrator	2	34	
3	Astable multivibrator	2	36	
4	Schmitt trigger using transistors	1	37	
5	Review	1	38	
6	Unit Test-IV	1	39	

UNIT-V: Time Base Generators

Sl. No.	Topic	No. of periods	Cumulative periods	Completed date
1	General feature of Time base signal, methods of generating time base waveform	1	40	
2	Miller and Bootstrap time base generators-basic principles	1	41	
3	Transistor Miller, Bootstrap time base generators, Current time base generator, problems	2	43	
4	Review	1	44	
5	Unit Test-V	1	45	

UNIT-VI: Sampling Gates

Sl. No.	Topic	No. of periods	Cumulative periods	Completed date
1	Basic operation of Sampling gates, Unidirectional and Bi-directional sampling gate	3	48	
2	Reduction of pedestal in gate circuit Application of sampling gate	2	50	
3	Review	1	51	
4	Unit Test-VII	1	52	

UNIT-VII: Synchronization and Frequency Division

Sl. No.	Topic	No. of periods	Cumulative periods	Completed date
1	Principles of synchronization, frequency division in sweep circuit	2	53	
2	Astable, Monostable relaxation circuits	1	54	
3	Sync of sweep circuit with symmetrical signals	1	55	

4	Sine wave freq division with a sweep circuit	1	56	
5	Review	1	57	
6	Unit Test-VI	1	58	

UNIT-VIII: Realization of Logic Gates using Diode and Transistor

Sl. No.	Topic	No. of periods	Cumulative periods	Completed date
1	AND, OR gates using Diodes, Resistor, Transistor Logic	2	59	
2	Diode Transistor Logic	1	61	
3	Review	1	62	
4	Unit Test-VIII	1	63	

References: 1. Pulse,Digital and Switching wave form – by J. Millman and H. Taub, McGraw-Hill 1991.

2. Pulse and Digital circuits – A Anand Kumar,PHI.

3. Pulse and Digital Circuits – Yoganarasimham

TIME TABLE

COURSE MATERIAL

UNIT-1

LINEAR WAVE SHAPING

1.1 Introduction:

Consider a transmission network consisting of linear elements. If a sinusoidal signal is applied to such a network, in the steady state, the output signal is also sinusoidal in shape. Thus, the circuit preserves the sinusoidal input wave shape, at the output. The effect of the circuit on the input to produce the output is characterized by two parameters which are

1) Ratio of the amplitude of output to input

2) The phase angle between output and input

But it can be noted that such a reproduction of the input wave shape at the output is possible only in case of sinusoidal signals and not in case of other signals. No other periodic wave shape preserves its shape. Generally, there is vast difference between output wave shape and input wave shape. The process by which the shape of a nonsinusoidal signal is changed by passing the signal through the network consisting of linear elements is called *Linear Wave Shaping*.

We come across number of nonsinusoidal signals in practice such as step, pulse, square wave, ramp etc. Such signals are very common in case of pulse circuits. The effect of simple linear networks such as RC and RL circuits, on the nonsinusoidal waveforms is discussed in this chapter.

1.2 Nonsinusoidal Waveforms:

The commonly occurring nonsinusoidal waveforms are

- Step waveform
- Pulse waveform
- Square waveform
- Ramp waveform

1.2.1. Step wave form:

The step voltage input has the characteristics that its value is zero for all t<0 and its value is constant say A units for all t>0.The switch over from the value zero to the value A units takes place at t=0 and that too instantaneously. The step wave form is shown in the *Fig.1.1*

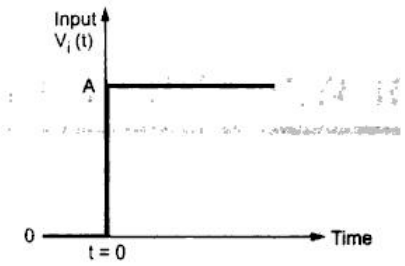


Fig.1.1.The step wave form

Mathematically it can be expressed as,

$$V_i(t) = 0 \quad t < 0$$
$$= A \quad t \geq 0$$

1.2.2. Pulse waveform:

The ideal pulse waveform is shown in *Fig 1.2.*The wave form has the value zero for all t<0 and for all $t>t_p$.while in between t=0 and $t=t_p$ its value is A units. The transition from 0 to level A takes place at t=0 instantaneously while transition from A to 0 takes place at $t=t_p$ instantaneously.

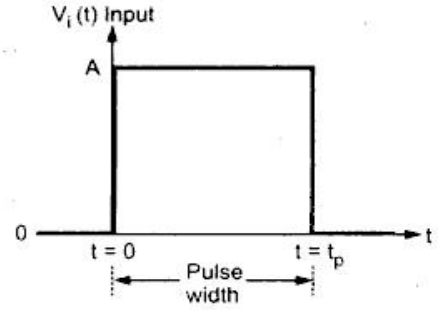


Fig.1.2 The pulse wave form

Mathematically it can be expressed as,

$$V_i(t) = 0 \quad \text{for } t < 0 \text{ and } t > t_p$$

$$= A \quad \text{for } 0 \le t \le t_p$$

The two step voltages constituting a pulse waveform,are shown in the *Fig,1.3.(1) and (b),*while their addition is shown in *Fig.1.3(c).*

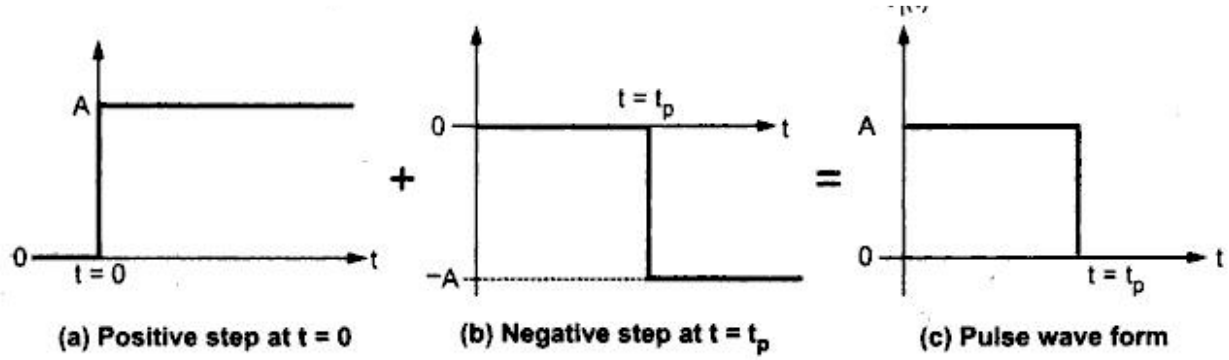


Fig.1.3

1.2.3. Square Wave form:

The square waveform has a constant level A' maintained for a time perid T_1 while it has another constant level A" maintained for a time period T_2 and this behavior is repetetive ; with a perid $T=T_1+T_2$.Such square wave is shown in *Fig 1.4.*

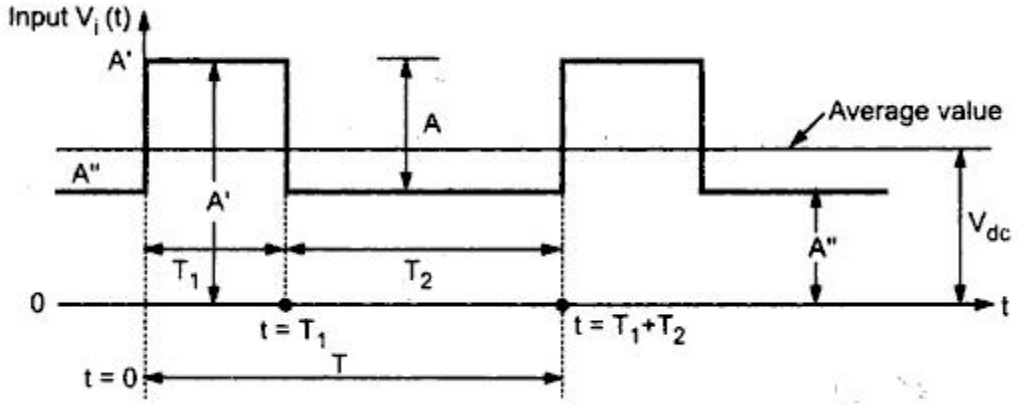


Fig.1.4.The square waveform

The square wave consists of a d.c level as V_{dc} in the *Fig 1.3*.It is called average value of the square waveform. The amplitude of the square wave is the difference between its two levels A' and A''.It is denoted as A=A'-A''.

A=Amplitude of square wave =A'-A''

Mathematically square waveform is expressed as,

$$V_i(t) = A' \qquad 0 < t < T_1$$
$$= A'' \qquad T_1 < t < T$$

The transition between two levels occurs at t=0, $t=T_2$, $t=T_1+T_2$ and so on.

1.2.4. Ramp Waveform:

A wave form which is zero for all t<0 and then increases linearly with time for t>0 is called a ramp waveform or sweep waveform. It is shown in the *Fig.1.5.*

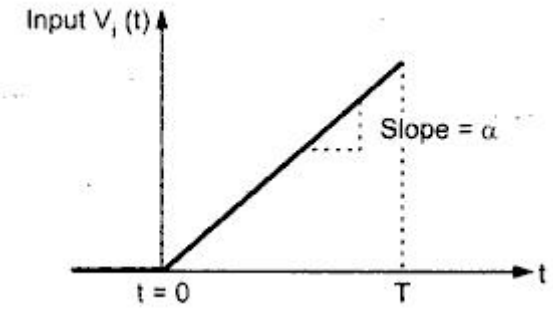


Fig.1.5 The ramp wave form

The slope of the ramp is shown as α, hence mathematically it can be expressed as,

$$V_i(t) = 0, \quad \text{for } t < 0$$
$$= \alpha t, \quad \text{for } t \geq 0$$

There are four commonly occurring nonsinusoidal waveforms. Let us see the effect of RC and RL linear networks on these inputs. The RC circuit can be divided into two categories which are:

1. High pass RC circuit and

2. Low pass RC circuit

1.3. The High Pass RC circuit:

Consider the RC circuit shown in the *Fig .1.6.*The output is taken across the resistance C.The input is $V_i(t)$ while the output is denoted as $V_o(t)$.'q' is the charge on the capacitor C.

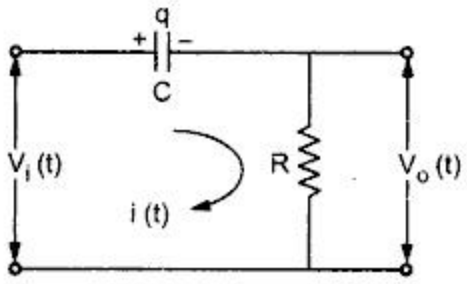


Fig.1.6.The High Pass RC circuit

The capacitive reactance offered by the capacitor depends on the frequency and is given by,

$$X_C = \frac{1}{2\pi f C} \qquad (1.1)$$

Where f=frequency of the input waveform.

As X_c is inversely proportional to f, the reactance decreases as frequency increases.

At zero frequency i.e., for d.c input the reactance becomes infinity and hence offers open circuits. Thus the circuit obstructs the low frequencies while it allows high frequencies to reach output. Hence the circuit is called high pass RC circuits. Due to this feature of the circuit, it is commonly used as the coupling circuit to provide dc isolation between input and output. For such a high pass RC circuit, the magnitude of the ratio of out to input is called transfer function or amplification or gain is given by,

$$|A| = \frac{1}{\sqrt{1+\left(\frac{f_1}{f}\right)^2}}$$

Where f1= $\frac{1}{2\pi RC}$, f = input frequency

At the frequency f1 the magnitude of the capacitive reactance is equal to resistance. The gain is 0.707.Thus the drop in the signal level is 3db .hence f1 is also called as lower 3db frequency or cutoff frequency or corner frequency.

Let us consider various nonsinusoidal waveforms applied as input to high pass RC circuit and study the effect of the circuit on the input applied, to produce the output.

1.3.1 Step input Voltage:

Consider the step input voltage of magnitude A volts is applied as an input to the high pass RC circuit.

The output is the voltage across the resistance R it can be observed that when the excitation applied to the circuit, the current starts flowing instantaneously ,as the capacitor charges exponentially, the current decays exponentially. Thus the output voltage also decays exponentially. When capacitor charges equal to the input voltage level of A volts, current stops and thus in steady state the output voltage attains zero value.

Let us mathematically analyze this behavior. The output voltage is of the form,

$$V_o(t) = B_1 + B_2 e^{-t/\tau} \quad (1.2)$$

Where B_1,B_2 = Constants, t=time constant of the circuit.

$$\tau = RC \quad (1.3)$$

The output voltage expression consist of two parts which are,

1) The steady state part represented by B_1

2) The transient part represented by exponentially decaying term $B_2 e^{-t/\tau}$

Obtaining the constants B_1 and B_2:

The circuit is said to achieve steady state when the transient part completely dies out i.e,t→∞.

$$\lim_{t\to\infty} V_o(t) = \lim_{t\to\infty} (B_1 + B_2\ e^{-t/\tau})$$
$$= B_1 \text{ as } \lim_{t\to\infty} e^{-t/\tau} = 0$$

Let the actual steady state value of the output voltage V_i

$$B_1 = V_i \tag{1.4}$$

To determine the constant B_2, consider the initial output voltage i.e., at t=0. And the output voltage at t=0 be V_o. Thus we get,

$$V_o(t)\big|_{t=0} = B_1 + B_2 = V_i$$
$$V_i = V_f + B_2$$
$$B_2 = V_i - V_f \tag{1.5}$$

Substituting the values of B_1 & B_2 in equation (2)

$$V_o(t) = V_f + (V_i - V_f)\ e^{-t/\tau} \tag{1.6}$$

This is the generalized expression for the output voltage and is called the basic equation. Now determine V_i and V_0 for the circuit to which the step voltage of A volts is applied.

As mentioned earlier, in the steady state $t\to\infty$, the input is constant=A volts. Thus as $t\to\infty$, the input to the circuit is as good as dc of A volts. The capacitor blocks dc. Hence final steady state output voltage is zero.

$$V_f = 0\ V$$

Incase of capacitor, the current starts flowing instantaneously but it takes finite time to charge the capacitor. Thus at $t=0^+$ i.e., just after t=0 the input voltage $V_i(t)$ attains a value of A volts. The voltage across capacitor is zero as it cannot change instantaneously .And hence the output voltage at $t=0^+$ is same as the input voltage equal to A volts .So when capacitor is initially uncharged, them the output is same as input at $t=0^+$.

$$V_i = A \text{ volts}$$

Substituting in basic equation (6), the response of high pass RC circuit to step input can be obtained as,

$$V_o(t) = A\, e^{-t/RC} = A\, e^{-t/\tau} \qquad (1.7)$$

Now let –t/t=x

$$V_o(t) = A\ e^{-x}$$

Hence the vales of the output voltage for various values of x can be obtained as shown in the *Table1.1.*

x	V_o
0	A
0.5	0.606 A
1	0.367 A
2	0.135 A
3	0.05 A
4	0.018 A
5	0.007 A

Table 1.1

Note that the output is 60.6% of then the magnitude of the step input at x=0.5 i.e., t=0.5 t while 36.7% at t=*t* and so on. At t=5t it is 0.7% of the magnitude of step and the output waveform is asymptotic to the zero voltage line. But for all practical purposes it is assumed as the steady state has bee reached after t=5t.

Time constant : The time required by the output variable to reduce to 36.7% of its maximum value is called time constant of the circuit. It is denoted as τ.

For the high pass RC circuit, τ = RC.

The output waveform is shown in *Fig1.7.*

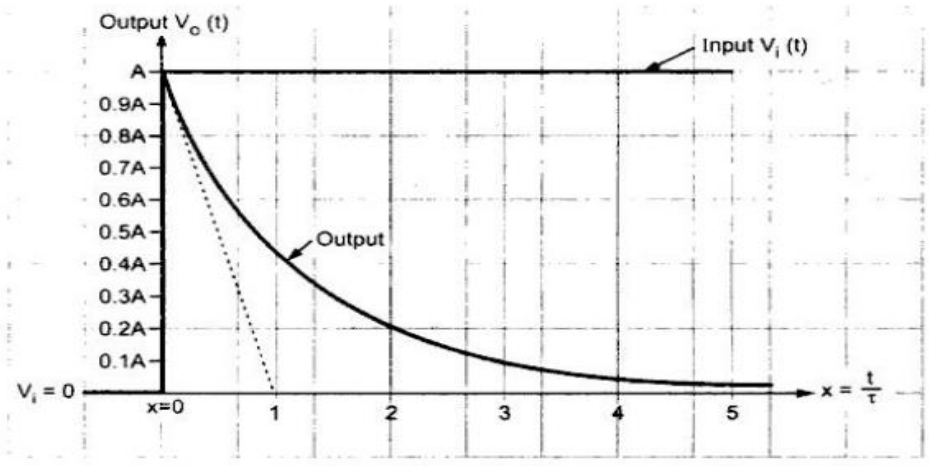


Fig.1.7. Step response of high pass RC circuit

The dashed line shown in tangent to the exponential response at t=0+ i.e., just after t=5*t* when input transition from zero to A, takes place.

1.3.2. Pulse Input Voltage:

Consider that the pulse type of voltage having pulse width t_p is applied as the input to the high pass RC circuit. It has been mentioned that the pulse is the sum of the two step voltages.

Consider the part of the pulse till time just before t=tp i.e tp=the response of the circuit to this part will be exactly similar to the response of the circuit to the step input.

$$V_{o1}(t) = A\, e^{-t/RC} \qquad \text{for } 0 < t < t_p$$

At $t=t_p$,

$$V_{o1}(t) = A\, e^{-t_p/RC} = V_p \qquad (1.8)$$

Now consider the second part of the input for $t>t_p$, at $t=t_p$, the input falls instantaneously from the level A to 0.The output just before this instant is V_p as given by the equation (1.8).Now though pulse input decreases abruptly by A volts, the capacitor voltage can't change instantaneously. Hence the output drop by A volts instantaneously just after $t=t_p$ i.e t_p^+.Then the capacitor voltage changes, the output voltage decreases exponentially to 0.
For the second part of the pulse we can write,

$$\text{at } t = t_p+, \quad V_{o2}(t_p^+) = V_p - A$$

$$\therefore \quad V_{o2}(t_p^+) = A\,e^{-t_p/RC} - A$$

$$V_{o2}(t_p^+) = A\left(e^{-t_p/RC} - 1\right) \tag{1.9}$$

This is the initial output voltage for the second part of the pulse input.

$$V_i = A\left(e^{-t_p/RC} - 1\right)$$

The final value of the output voltage is zero.

$$V_f = 0$$

$$V_{o2}(t) = V_f + (V_i - V_f)\,e^{-t/RC}$$

$$V_{o2}(t) = A\left(e^{-t_p/RC} - 1\right)e^{-(t-t_p)/RC} \tag{10}$$

The step has occurred at $t=t_p$ hence the term $e^{-t/RC}$ is changed to $e^{-(t-t_p)/RC}$ in the basic equation. The eq(10) represents the expression for the output voltage for $t>t_p$. the $V_{o1}(t)$ and $V_{02}(t)$ together represent the response of the high pass RC circuit to the pulse input. It is shown in the *Fig.1.8*.

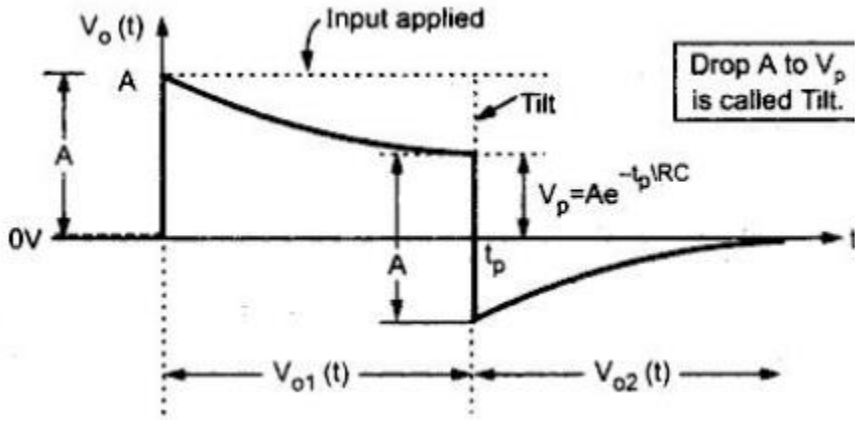


Fig.1.8..Pulse responses of high pass RC circuit

It can be observed from the response that there are two types of distortions resulted after passing a pulse through high pass RC circuit.

1) A tilt at the top of the pulse.
2) An under shoot at the end of the pulse.

To minimize these distortions, to keep the output waveform same as the input, the time constant RC must be as large as possible compared with the pulse width t_p.However ,for all the values of the ratio RC/t_p, there exists an undershoot whatever small it may be.

To prove that are below the axis is equal to that above the axis:

To verify this, let us obtain the are, by directly integrating the expressions of $V_{01}(t)$ and $V_{02}(t)$.

$$A_1 = \int_0^{t_p} V_{01}(t)\,dt = \int_0^{t_p} A e^{-t/\tau}\,dt \qquad \text{where } \tau = RC$$

$$= A\left[\frac{e^{-t/\tau}}{\frac{-1}{\tau}}\right]_0^{t_p}$$

$$A_1 = A\tau\left[-e^{-t_p/\tau} + 1\right]$$

$$A_2 = \int_{t_p}^{\infty} V_{02}(t)\,dt = \int_{t_p}^{\infty} A(e^{-t_p/\tau} - 1)\, e^{-(t-t_p)/\tau}\,dt$$

$$= A(e^{-t_p/\tau} - 1)\left[\frac{e^{-(t-t_p)/\tau}}{\frac{-1}{\tau}}\right]_{t_p}^{\infty} = A(e^{-t_p/\tau} - 1)\left[0 - \left(-\frac{1}{1/\tau}\right)\right]$$

$$A_2 = A\tau\left[e^{-t_p/\tau} - 1\right]$$

It can be seen that the two areas A_1 and A_2 are equal in magnitude and opposite in sign. This proves the fact that two areas are equal and one is above the axis while other is below the axis. The response with large time constant $RC/t_p >> 1$ shown in the *Fig.1.9.*

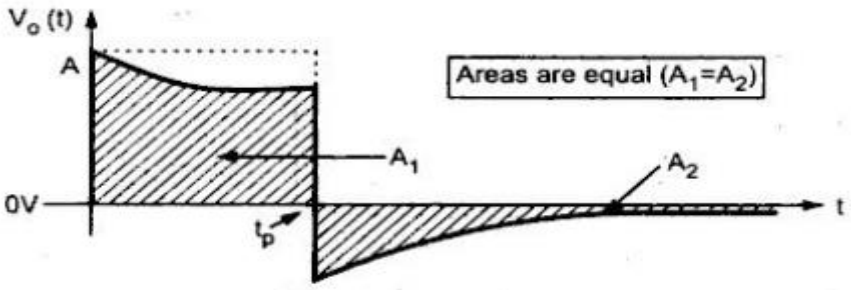


Fig.1.9.The pulse response if RC/t_p >>1

It can be observed that large time constant the tilt is very small and undershoot also is very small. Both the distortions are small. But the negative waveform, decreases very slowly as its area is equal to that of positive portion, as shown in *Fig1.9.*With the small time constant RC/tp<<1,the response changes as shown in the *Fig1.10.*

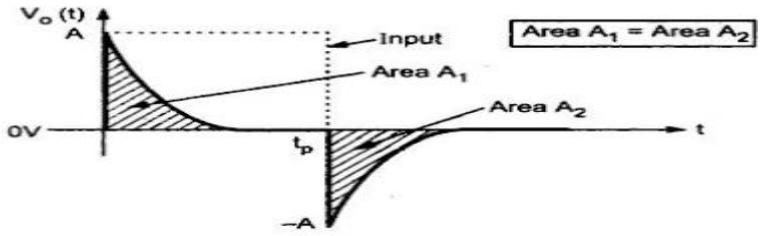


Fig.110.The pulse response if RC/t_p <<1

For a small time constant, the output consists of a positive spike or a pip of amplitude A at the start of the pulse while it consists of a negative spike of the same size at the end of the pulse. In fact the process of converting pulses into spikes or pips by using circuits of small time constant is called **peaking**.

1.3.3 Square Wave Input Voltage:

It has been mentioned earlier that the square wave has some average value above zero voltage level. Let us find out what happens if such a square wave is impressed on the high pass RC circuit.

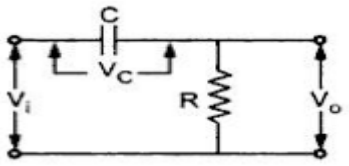


Fig 1.11

For any Periodic input waveform the average level of the steady state output response obtained from the high pass RC circuit is always zero, irrespective of the dc level of the input .Let us prove this fact first. Consider he various voltages present in the high pass RC circuit as shown in the *fig1.11*.

Let V_i=Input Voltage, V_c=voltage across capacitor, V_o=Output voltage.

q=Charge on capacitor.

By Kirchhoff's voltage law,

$$V_i = V_C + V_o \tag{1.13}$$

$$V_i = \frac{q}{C} + V_o \quad \text{Note : } V_C \times C = \text{charge } q \tag{1.14}$$

Differentiating the equation (14)

$$\frac{dV_i}{dt} = \frac{1}{C}\frac{dq}{dt} + \frac{dV_o}{dt}$$

But $\frac{dq}{dt} = i$ ……Rate of flow of charge

$$\frac{dV_i}{dt} = \frac{i}{C} + \frac{dV_o}{dt} \tag{1.15}$$

Now V_o=iR

$$i=V_o/R \tag{1.16}$$

Substituting in(16)

$$\frac{dV_i}{dt} = \frac{V_o}{RC} + \frac{dV_o}{dt} \tag{1.17}$$

Multiplying by dt,

$$dV_i = \frac{V_o}{RC}dt + dV_o \tag{1.18}$$

Integrating this over one time period from 0 to T,

$$\int_0^T d\,V_i = \frac{1}{RC}\int_0^T V_o\,dt + \int_0^T d\,V_o$$

$$[V_i]_0^T = \frac{1}{RC}\int_0^T V_o\,dt + [V_o]_0^T$$

$$V_i(T) - V_i(0) = \frac{1}{RC}\int_0^T V_o\,dt + V_o(T) - V_o(0) \tag{1.19}$$

Under steady state condition both input & output waveform are periodic in nature with period T.

$$V_i(T) = V_i(0) \text{ and } V_o(T) = V_o(0)$$

Substituting in (19),

$$\frac{1}{RC}\int_0^T V_o\,dt = 0 \tag{1.20}$$

But $\int_0^T V_o\,dt$ represents the are under the output waveform over one cycle i.e., the average value of the output response.

Important points about high pass RC circuit:

The following points can be noted for high pass RC circuit:

1. The average level of the output signal is always zero, under steady state, independent of the average level of the input.

2. The output extends in both positive and negative direction with respect to zero voltage axes.

3. The area of the part of waveform above zero voltage axis is same as the area of the part Of waveform below zero voltage axis.

4. When input changes discontinuously by an amount V, output also changes by the same amount, in the same direction.

5. If input maintains a constant level for a finite time interval like a step input, the output decays exponentially towards zero voltage.

Thus in the limiting case, when the ratios RC/T_1, and RC/T_2 are both very large with respect to unity, the output waveform is exactly same as the input. In such limiting case there is no exponential decay present in the output and the average value of output is zero i.e. D.C. component present in the output is zero. Such responses of high pass RC circuit for a square wave input is shown in the *Fig. 1.12.*

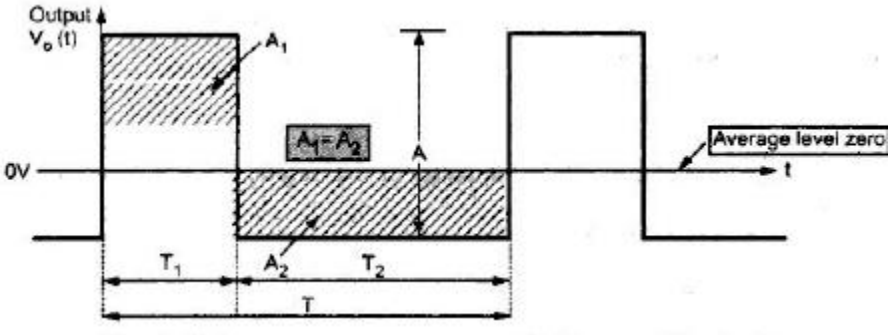


Fig.1.12.The response of high pass RC circuit for a square wave input with very large time constant

Now consider another extreme case when RC/T_1, and RC/T_2 are both very small, is compared to unity. In this case, for a positive pulse type part of square wave input, there exists a positive spike of amplitude A while for the negative part of square wave there exists a negative spike of amplitude A. 'Thus, peak to peak amplitude of the output in such a case is twice the peak to peak amplitude of the input.

This response is shown in the *Fig. 1.13*.

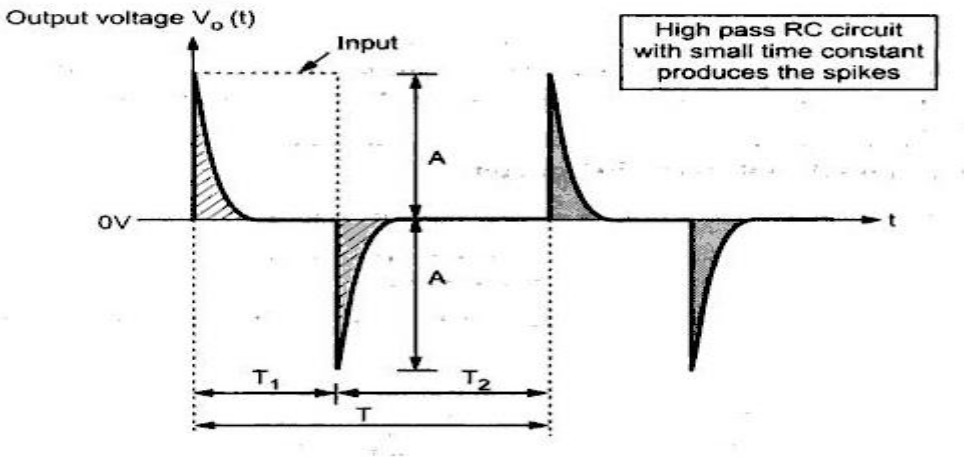


Fig.1.13.Square wave response of high pass RC circuit with very small time constant

More generally the square wave response of high pass RC circuit can be obtained by using equation

The voltage level of the positive part of the output square wave is A_1, hence after time T_1, we will get the output equal to say V_1

$$V_1' = A_1 e^{-T_1/RC} \qquad (1.21(a))$$

Then in the input there is discontinuity of A volts. So in the output also there exists a discontinuity of A volts at $t=T_1$,

$$A_2 = V_1' - A \qquad (1.21(b))$$

Then again there will 'be an exponential decay of the output towards zero for the time period T_2 given by,

$$V_2' = A_2 e^{-T_2/RC} \qquad (1.21(c))$$

And again after one time period T, there is discontinuity of A volts in the output in the positive direction.

$$A_1 = V_2' + A \qquad (1.21(d))$$

The behavior repeats with the time period T. The general square wave response of high pass RC circuit is shown the *Fig. 1.14*.

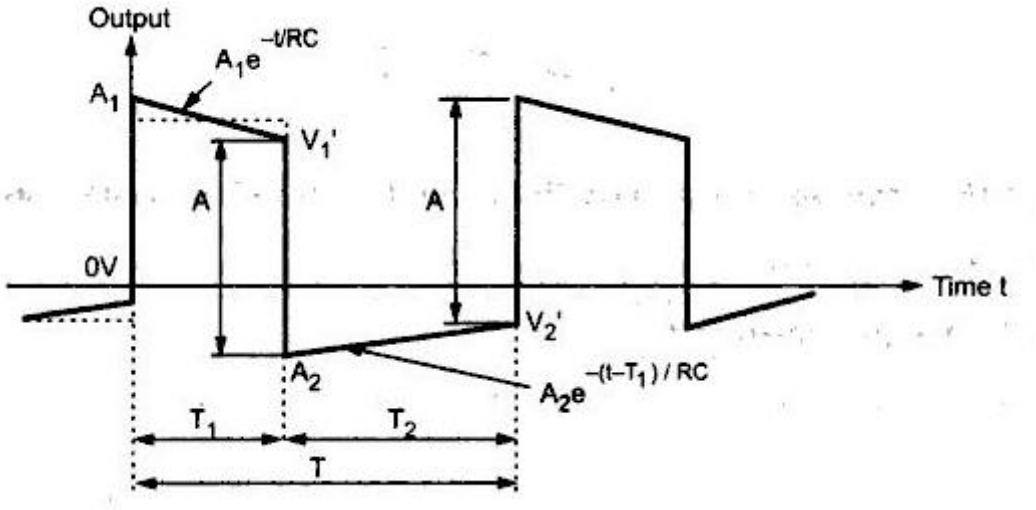


Fig.1.14General square wave response of high pass RC circuit

For a symmetrical square wave then $T_1=T_2=T/2$, we can write,

$$A_1 = -A_2 \text{ and } V_1' = -V_2' \text{ due to symmetrical input}$$

Under this condition the equations (1.21(a)) and (1.21b)) will be identical with the equations (1.21(c)) and (1.21(d)). In this case,

$$A_1 = \frac{A}{1 + e^{-T/2RC}} \qquad (1.22(a))$$

$$V_1' = A_1 e^{-T/2RC} = \frac{A}{1 + e^{+T/2RC}} \qquad (1.22(b))$$

For T/2RC<<1 the above set of equations reduces to,

$$A_1 \approx \frac{A}{2}\left(1 + \frac{T}{4RC}\right) \qquad (1.23(a))$$

And $$V_1' \approx \frac{A}{2}\left(1-\frac{T}{4RC}\right)$$ (1.23(b))

The response to symmetric square wave can be shown as in the *Fig. 1.15.*

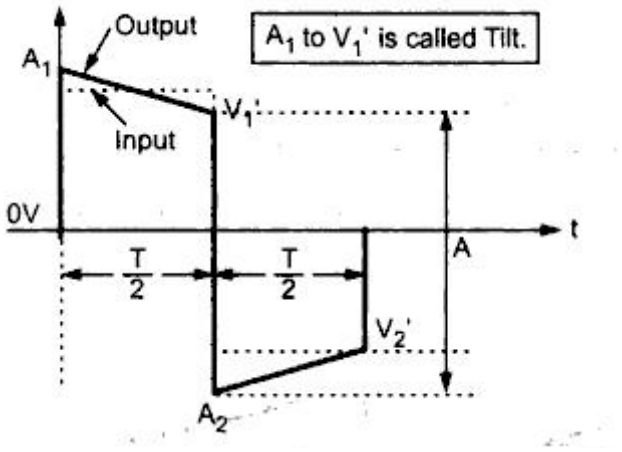


Fig.1.15Response of high pass RC circuit to symmetric square wave

Expression for the percentage tilt:

The Tilt is defined as the decay in the amplitude of the output voltage waveform, when the input maintains its level constant.

It can be seen that when the input maintains its level constant at A' during the time T1, then the output amplitude changes from A1, to V1'. This change in the amplitude of the output is called as tilt.

The percentage tilt is the decay of the output amplitude expressed as a percentage of the input amplitude.

Mathematically the percentage tilt P is defined as.

$$P = \frac{A_1 - V_1'}{\text{input amplitude}} \times 100$$ (1.24(a))

Tilt for symmetrical input:

Let us obtain the expression for the tilt considering symmetrical input.

Now for the symmetrical input the amplitude during the positive swing is A/2. Substituting in the above equation (24 (a)),

$$P = \frac{A_1 - V_1'}{A/2} \times 100 \qquad (1.24(b))$$

Substituting the expressions of as and V_1' from the equations (1.22 (a)) and (1.22 (b)) we get,

$$P = \frac{\left[\frac{A}{1+e^{-T/2RC}}\right] - \left[\frac{A}{1+e^{T/2RC}}\right]}{\left(\frac{A}{2}\right)} \times 100$$

$$= \frac{\left(1+e^{T/2RC} - 1 - e^{-T/2RC}\right)}{\left(1+e^{-T/2RC}\right)\left(1+e^{T/2RC}\right)} \times 2 \times 100$$

$$= \frac{\left(1+e^{T/2RC} - 1 - e^{-T/2RC}\right)}{\left(1+e^{-T/2RC}\right)\left(1+e^{T/2RC}\right)} \times 200$$

Now $e^{T/2RC} - e^{-T/2RC} = \left(1 - e^{-T/2RC}\right)\left(1+e^{T/2RC}\right)$

$$P = \frac{\left(1 - e^{-T/2RC}\right)\left(1+e^{T/2RC}\right)}{\left(1+ e^{-T/2RC}\right)\left(1+e^{T/2RC}\right)} \times 200$$

$$P = \frac{\left(1 - e^{-T/2RC}\right)}{\left(1+ e^{-T/2RC}\right)} \times 200 \qquad (1.24(c))$$

This is the general expression for the percentage tilt.

For $RC >> T$ and $RC / T >> 1$

$T / RC << 1$ and $T / 2RC << 1$

As $T/2RC<<1$, expressing exponential term into its power series form

and neglecting higher order terms we get,

Now $$e^{-T/2RC} \approx 1 - \frac{T}{2RC}$$

Substituting in the equation (1.28 (c)),

$$\% P = \frac{1-\left(1-\frac{T}{2RC}\right)}{1+\left(1-\frac{T}{2RC}\right)} \times 200$$

$$= \frac{\frac{T}{2RC}}{2-\frac{T}{2RC}} \times 200$$

Neglecting T / 2RC compared to 2 from the denominator we get

$$\% P \approx \frac{T}{2RC} \times 100\ \% \qquad (21.4(d))$$

Relationship between tilt and Time constant:

For high pass RC circuit time constant is given by,

$$\tau = RC$$

Substituting the equation for tilt,

$$\% P = \frac{T}{2\tau} \times 100\ \% \qquad (1.25(a))$$

Relationship between 3dB frequency and Time constant:

For high pass RC circuit 3dB frequency f1 is given by,

$$f_1 = \frac{1}{2\pi RC}$$

But $\tau = RC$

$$f_1 = \frac{1}{2\pi\tau} \qquad (1.25(b))$$

Relationship between 3dB frequency and Tilt:

From the relation of 3-dB frequency and the time constant we can write, Hence the tilt can he expressed as,

$$\% P = \frac{T}{2\left(\frac{1}{2\pi f_1}\right)} \times 100\%$$

$$\% P = \pi f_1 T \times 100\% \qquad (1.25(c))$$

Now

$$T = \frac{1}{f}$$

$$\% P \approx \frac{\pi f_1}{f} \times 100\% \qquad (1.25(d))$$

Where f=input frequency of square wave=1/T

f1=lower 3-dB frequency=1/2πRC

1.3.4. Ramp input Voltage:

Consider that the ramp input of slope α is applied to the high pass RC circuit. From equation (14) we can write,

$$V_i = \frac{q}{C} + V_o$$

where $V_i(t) = \alpha t$ = input ramp

$$V_i = \frac{q}{C} + V_o \qquad (1.26)$$

Differentiating the equation (1.26)

$$\alpha = \frac{1}{C}\frac{dq}{dt} + \frac{dV_o}{dt} \qquad (1.27)$$

$$\text{but} \qquad \frac{dq}{dt} = i$$

$$\text{and} \qquad V_o = iR$$

$$i = \frac{V_o}{R}$$

$$\frac{dq}{dt} = \frac{V_o}{R}$$

Substituting in the equation (1.27)

$$\alpha = \frac{V_o}{RC} + \frac{dV_o}{dt} \qquad (1.28)$$

Thus differential equation has a solution

$$V_o = \alpha RC\,(1 - e^{-t/RC})$$

Where $V_0=0$ at t=0 (1.29)

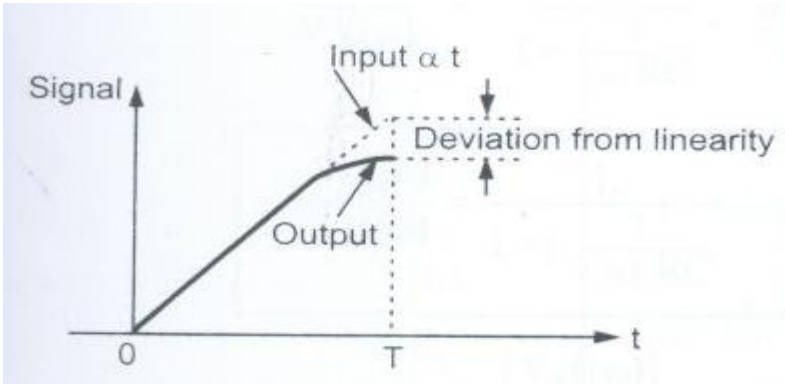


Fig.1.16 Ramp response of high passRC circuit RC/T >> 1

For times t which are very small in comparison with the time constant RC, the exponential term can be replaced by its series as,

$$V_o = \alpha\, t\left(1 - \frac{t}{2\,RC} + \cdots\right) \tag{1.30}$$

This equation represents the response of high pass RC circuit to a ramp input. The Output waveform is shown in the Fig. 1.16. The falling away of output from input is called deviation of output from linearity. It is the difference between input and output divided by the input, at a particular time t. Thus error at time T can be obtained as,

$$e_t = \left.\frac{V_i - V_o}{V_i}\right|_{t=T}$$

$$e_t \approx \frac{T}{2RC} \approx \pi f_1 T \tag{1.31}$$

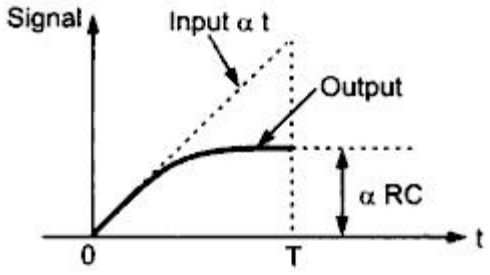


Fig.1.17.Ramp responses of high pass RC circuit with RC/T << 1

Where f1= $\frac{1}{2\pi RC}$, = lower 3-dB frequency

When RC is very small compared to t, then in the equation (1.29) the term $e^{-t/RC}$ approaches to zero. Hence in steady state output attains a fixed value of αRC after time t = T. This is shown in the *Fig. 1.17.*

This is the maximum value of lower3-dB frequency to achieve less than0.5% transmission error.

In general for e_t less than 0.5%,

f1<0.795Hz

i.e. RC< 0.2 Sec

1.3.4. Sinusoidal input:

The analysis of the high pass RC circuit to sinusoidal input is obtained using Laplace transform approach. The circuit in Laplace domain is shown in *Fig.1.18*.

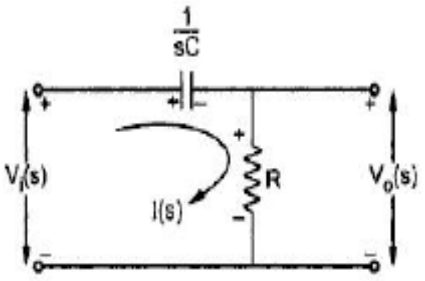


Fig.1.18.Laplace network of high pass RC circuit

Applying KVL to the circuit,

$$-\frac{1}{sC}\,I(s)-I(s)\,R+V_i(s)=0$$

$$\therefore \quad I(s)=\frac{V_i(s)}{\left[R+\frac{1}{sC}\right]}$$

$$V_o(s) \;=\; I(s)\,R=\frac{R\,V_i(s)}{R+\frac{1}{sC}}$$

$$\frac{V_o(s)}{V_i(s)}=\frac{R}{R+\frac{1}{sC}}=\frac{1}{1+\frac{1}{sRC}}$$

The frequency response of the circuit can be obtained by applying sinusoidal input and varying its frequency from 0 to ∞ .This can be analyzed from the transfer function by replacing s by jw.

$$\frac{V_o(j\omega)}{V_i(j\omega)} \;=\; \frac{1}{1+\frac{1}{j\omega RC}} \quad \text{but } \frac{1}{j}=-j \text{ and } \omega=2\pi f$$

$$\frac{V_o(j\omega)}{V_i(j\omega)} = \frac{1}{1 - j\,\frac{1}{2\pi f RC}}$$

$$A = \left|\frac{V_o(j\omega)}{V_i(j\omega)}\right| = \frac{1}{\sqrt{1+\left(\frac{1}{2\pi f RC}\right)^2}} = \text{Gain of the circuit}$$

Thus as frequency increases, the gain A approaches to unity. Initially output increases as the frequency increases and becomes equal to input at high frequencies. As $f\rightarrow\infty, A\rightarrow 1$ and circuit allows to pass high frequencies.

Lower cut-off frequency: The frequency at which the gain A is $(1/\sqrt{2})$is called lower cut off frequency f_l of the circuit.

$$\frac{1}{\sqrt{2}} = \frac{1}{\sqrt{1+\left(\frac{1}{2\pi f_l RC}\right)^2}}$$

$$\frac{1}{2} = \frac{1}{1+\left(\frac{1}{2\pi f_l RC}\right)^2}$$

$$2 = 1+\left(\frac{1}{2\pi f_l RC}\right)^2$$

$2\prod f_l RC=1.$

$$f1=\frac{1}{2\pi RC}=\text{Lower cut - off frequency}$$

The gain against the frequency plot for the sinusoidal input is shown in *Fig1.19.*

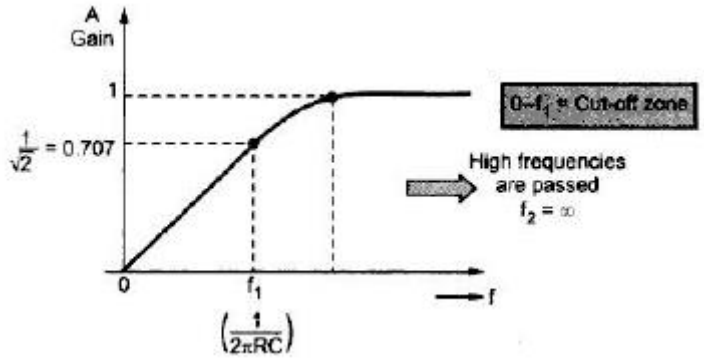


Fig.1.19. Gain-Frequency plot

Bandwidth: The frequency range for which gain does not fall below 0.707 times its maximum value is called the bandwidth (BW) of the circuit.

$$BW=f2-f1=\infty-f1=\infty$$

1.3.5. High Pass RC circuit as a Differentiator:

For a high pass RC circuit ,if time constant is very small as compared to the time required by the input signal to make an appreciable change, the circuit acts as a differentiator. Under this case, the drop across R is negligible compared to drop across C. Thus entire input Vi can be assumed to be appearing across C.

Then the current I is given by,

$$i = C\frac{dV_C}{dt} = C\frac{dV_i}{dt} \qquad (1.32)$$

Hence the output which is drop across R is

$$V_o=iR$$

$$V_o=RC\ dV_i/dt$$

(1.33)

Thus the output is proportional to the derivative of the input.

This can be verified for the various inputs discussed earlier. For a square wave input, at the points of discontinuity, the differentiation results in the impulses of infinite amplitude, zero width and alternating polarity. They are already shown in *Fig1.13.*The only thing is that, in this waveform, impulses have finite amplitude of A while ideal differentiation should give infinite amplitude. This error is due t the fact that for ideal differentiation, the voltage across R is neglected but practically it is not negligible as compared to the voltage across capacitor C.

For the ramp type of input, V_i is at which is linearly increasing. After differentiation, we get RC dV_i/dt i.e α RC which is constant magnitude output. These facts prove that a small time constant the high RC circuit behaves as a differentiator.

1.4. Low Pass RC Circuit:

Consider the RC circuit shown in the *Fig: 1.20.*the output is taken across the capacitor C. The input is $V_i(t)$ while output is $V_o(t)$.

The capacitive reactance X_c depends on the frequency.

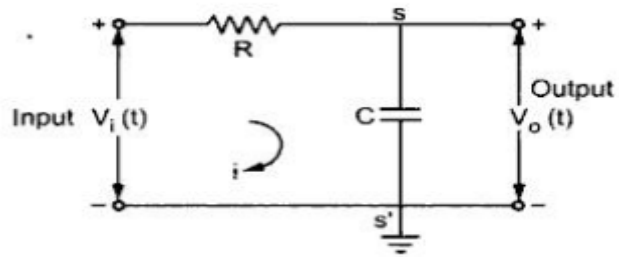


Fig.1.20.Low pass RC Circuit

At high frequencies, the capacitor acts as a virtual short circuit and hence output falls to zero. Thus the high frequencies get attenuated. The basic feature of the circuit is that it represents the situation which exists at the signal source terminals. The source terminals are s-s'.Looking back into these terminals. The source can be replaced by its Thevenins equivalent. The voltage Vi is the open circuit voltage and R is the Thevenins equivalent output impendence. The capacitor C now represent all the capacitance appearing in parallel across s-s'.This capacitance may be due to wires used to couple load and s-s',or may be due

to the capacitive component of admittance presented by load or due to the stray capacitance present across the source terminals. Due to this, the circuit is used when it is required to extend the range of operation of some electronic circuit to a higher frequency.

Let us consider the response of such low pass RC circuit to the various nonsinusoidal waveforms.

1.4.1 Step Input Voltage:

Consider that the step input voltage of magnitude A is applied to the low pass RC circuit ,having a time constant RC.The output is the voltage across the capacitor .The capacitor voltage cannot change instantaneously. Hence though there is discontinuity from 0 to A volts in the input at t=0, the capacitor voltage remains zero.

Initial voltage = $V_i = 0$ V

As time progresses, the capacitor gets charged and in the steady state its voltage is equal to the magnitude of the step voltage input i.e., A volts.

Final voltage = $V_f = A$ V

The general expression for the output is,

$$V_o(t) = V_f + (V_i - V_f)\, e^{-t/\tau}$$

Substituting the above values, we get the expression for the output as,

$$V_o(t) = A + (0 - A)\, e^{-t/\tau}$$

$$V_o(t) = A\,(1 - e^{-t/\tau})$$

(1.34)

Where t = RC=time constant

Thus the step response of low pass RC circuit is exponential with the time constant RC.It starts from zero and rises towards the as steady state value A.

Now let $t/\tau = x$

$$V_o(t) = A(1 - e^{-x})$$

Hence the values of the output voltage for the various values of x can be obtained as shown in the *Table1.2.*

x	V_o
0	0
0.5	0.39 A
1	0.63 A
2	0.86 A
3	0.95 A
4	0.98 A
5	0.99 A

Table1.2.

Note that the output is 632% of the final steady value at x=1 i.e, t=*t*=1 time constant. While after x= 5 i.e, t=5*t* the output is almost equal to A and for all practical purposes the circuit is assumed to reach its steady state. The step response is shown in the *Fig 1.21.*

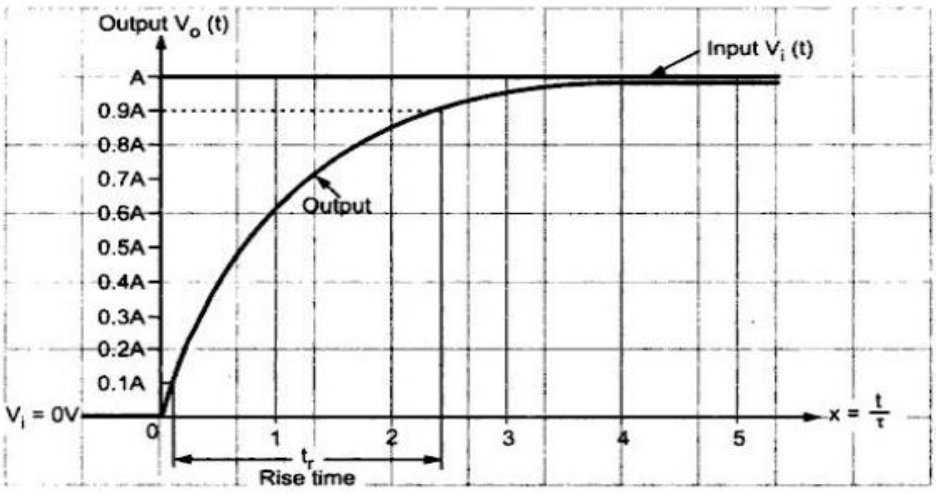


Fig1.21.Step responses of Low pass RC circuit

Rise time (t_r): It is the time required by the output response to rise from 10% to 90% of its final steady state value. It is indicated in the *Fig 1.21.*

Te time required for the output to achieve 10% of its final value can be obtained as,

$$V_o(t) = A(1 - e^{-t/RC})$$

$$0.1\ A = A\ (1 - e^{-t/RC})$$

$$0.1 = 1 - e^{-t/RC}$$

$$e^{-t/RC} = 0.9$$

$$\frac{-t}{RC} = ln(0.9)$$

$$t = 0.1\ RC$$

(1.35)

Similarly the time required for the output to achieve 90% of its final value is,

$$t = 2.3\ RC$$

(1.36)

$$t_r = 2.3\ RC - 0.1\ RC$$

$$t_r \approx 2.2\ RC \approx 2.2\ \tau$$

(1.37)

But $$f_2 = \frac{1}{2\pi R C}$$

$$t_r = \frac{2.2}{2\pi f_2} = \frac{0.35}{f_2}$$

.

(1.38)

1.4.2 Pulse Input Voltage:

Consider a pulse input voltage having pulse width t_p, applied as input to the low pass RC circuit. The pulse is sum of the two step voltages. Hence for the part of pulse just before $t= t_p$ the response of the low pass circuit is same as the response of circuit to step input of magnitude A. This can be indicated as,

$$V_{o1}(t) = A\,(1 - e^{-t/RC}) \quad \text{for } 0<t<t_p$$

At $t=tp_r$ $\quad V_{o1}(t) = A\left(1-e^{-t_p/RC}\right) = V_p$

(1.39)

Thus at the end of the pulse, the output achieves the voltage equal to V_p.

Now at $t=t_p$, the input decreases abruptly from A to OV. But the output which is voltage across capacitor cannot change instantaneously. Hence the capacitor char;, accumulated during the pulse cannot leak instantaneously. Hence just after $t=t_p$, i.e. at t_p^+. The output remains V_p. And then exponentially decreases towards zero with a time constant RC. Mathematically this part of the waveform can be expressed as,

$$V_{o2}(t) = V_p\, e^{-(t-t_p)/RC}, \quad \text{for } t > t_p \qquad (1.40)$$

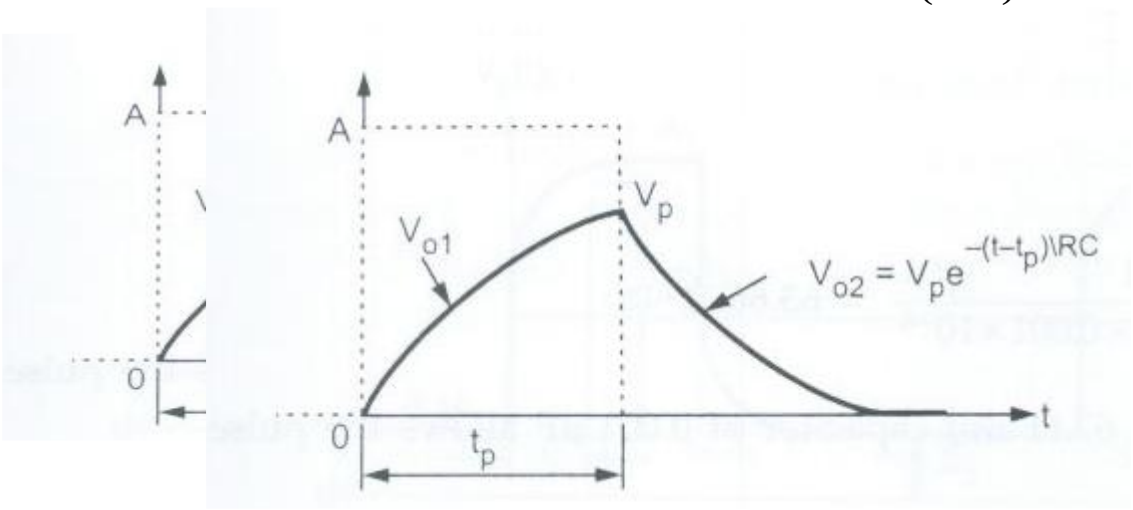


Fig.1.22.pulse responses of low pass RC circuit

Hence, the overall pulse response of low pass RC circuit is the addition of $V_{01}(t)$ and $V_{02}(t)$,shown in the *Fig.1.22*.The output response distorted for a pulse type of input.

If the upper3-dB frequency f_2 is chosen equal to reciprocal of the pulse width t_p, the output is faithful reproduction of the input.

$$f_2=1/t_p \qquad (8(a))$$

$$\text{i.e. } t_r=0.35t_p \qquad (8(b))$$

The output in such case is shown in *Fig.1.23*.

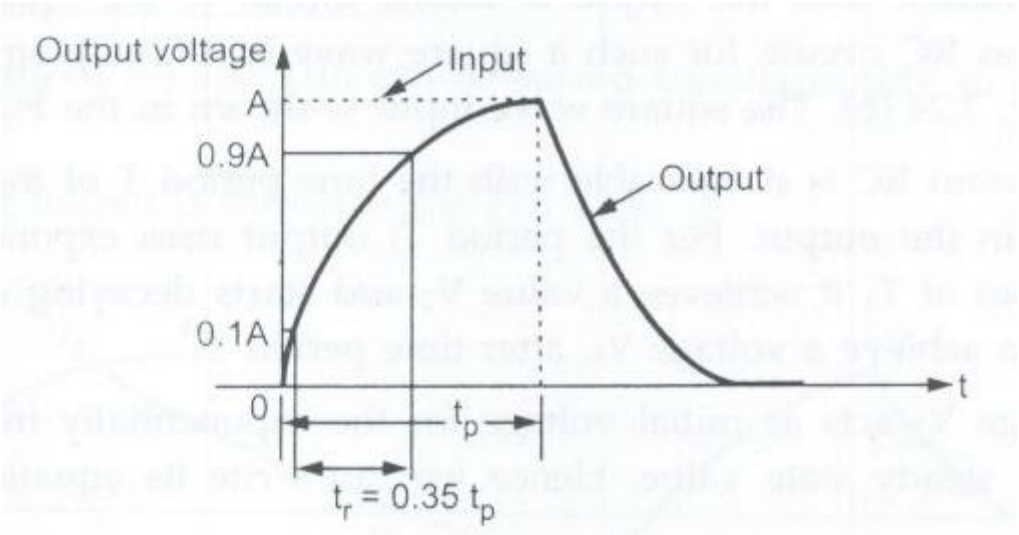


Fig.1.23 Pulse response for f2 =1 / t_p

1.4.3 Square Wave Input Voltage:

Consider a square wave whose instantaneous vale is constant at A_1 for the period T_1 while it changes suddenly from A_1 to A_2 and remain at A_2 for the period T_2.The addition of the two periods T_1+T_2 is nothing but the time period of the square wave. Such a square wave has some wave has some average value Vdc over the zero voltage level.

Now for the faithful reproduction it is necessary to have rise time t_r, smaller than the pulse width .The square wave can be considered to be made up of pulses of alternating polarity. In one cycle, there exists a positive pulse with width T_1 and a negative pulse of width T_2.When the rise time is very small compared to pulse width i.e, the time constant for the circuit is smallest then the output is almost similar to the square wave input. The response of low pass RC circuit, for such a square wave input, with smallest time constant is shown in the *Fig.1.24 (b).*The square wave input is shown in the *Fig1.24 (a).*

If the time constant RC is comparable with the time period T of the square wave, then there is distortion in the output .For the period T1 output rises exponentially and tries to achieve level A_1 .But at T_1 it achieves a value V_2 and starts decaying exponential towards the level A_2 but can achieve a voltage V_1, after time period T.Now the voltage V_1 acts as initial voltage for the exponentially increasing behavior and A_1 is its final steady state value. Hence we can write its equation as per the basic equation (6) as,

$$V_{o1} = A_1 + (V_1 - A_1)\, e^{-t/RC}$$

(1.41)

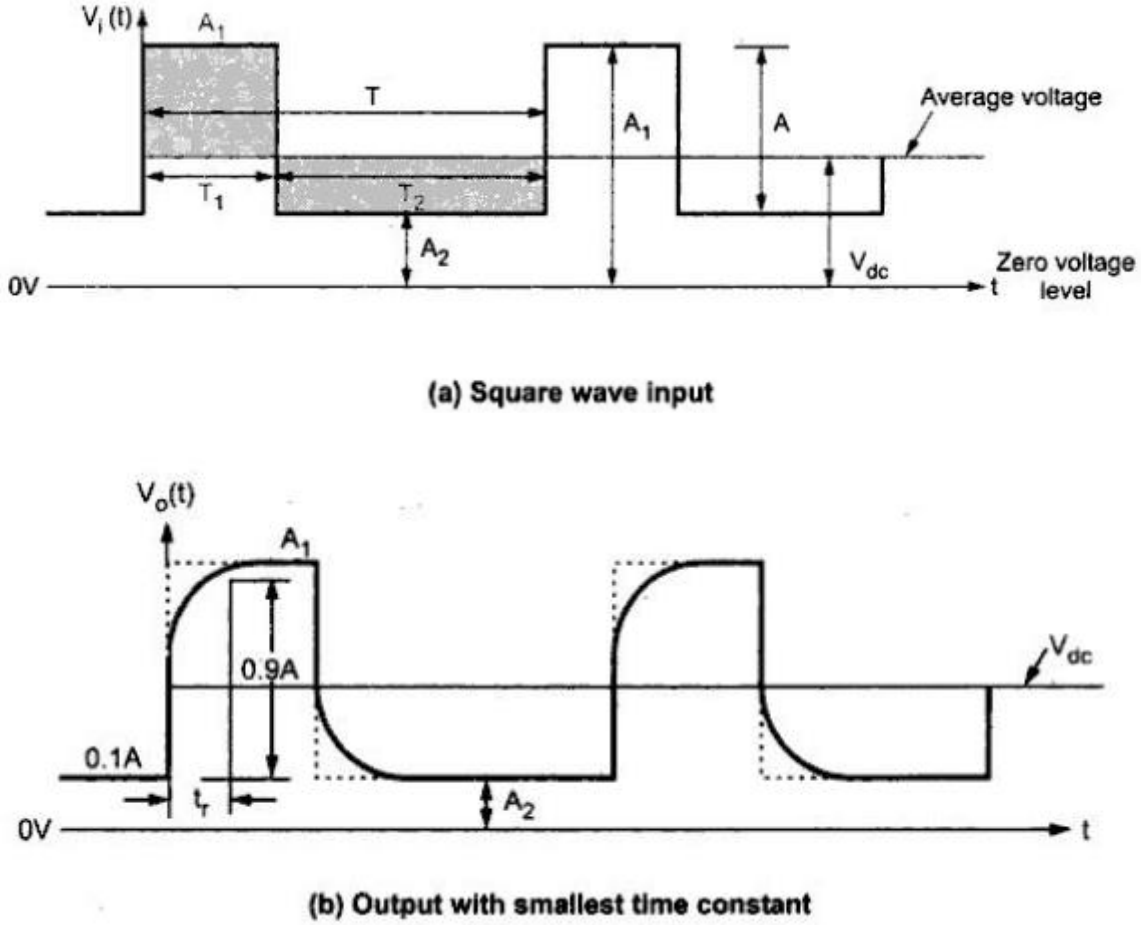


Fig.1.24.Square wave response of low pass RC circuit

While for exponential decay, the initial voltage is V2 and the final steady state value is A hence its equation becomes

$$V_{o2} = A_2 + (V_2 - A_2)\, e^{-(t - T_1)/RC}$$

(1.42)

If we set, $V_{o1} = V_2$ at $t = T_1$

$V_{o2} = V_1$ at $t = T_1 + T_2 = T$,

Then the two equations (1.41) & (1.42) can be solved simultaneously to obtain the values V_1 & V_2

The corresponding output is shown in the *Fig 1.25.*

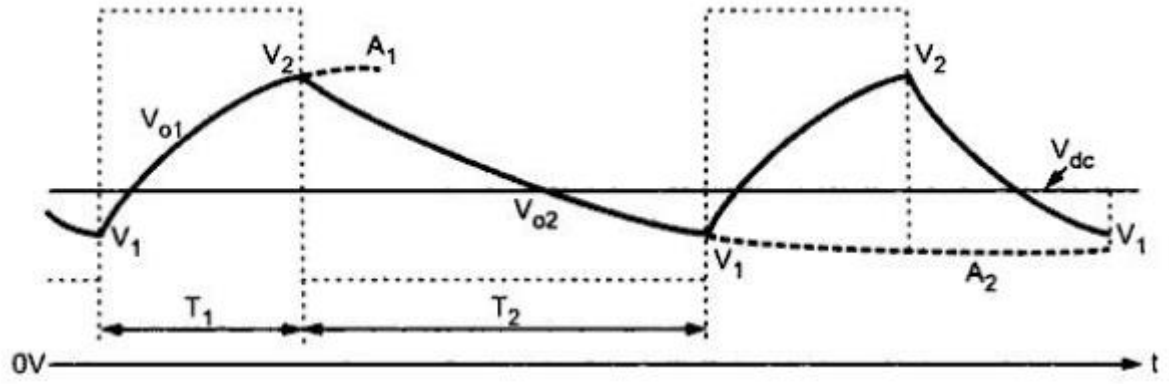


Fig.1.25 .Output when time constant RC is comparable with t

When the time constant is large as compared to the time period T of the square wave, t-n there exists exponential sections in the output which are almost linear. This is shown the *Fig. 1.26.* There exists maximum distortion under this case.

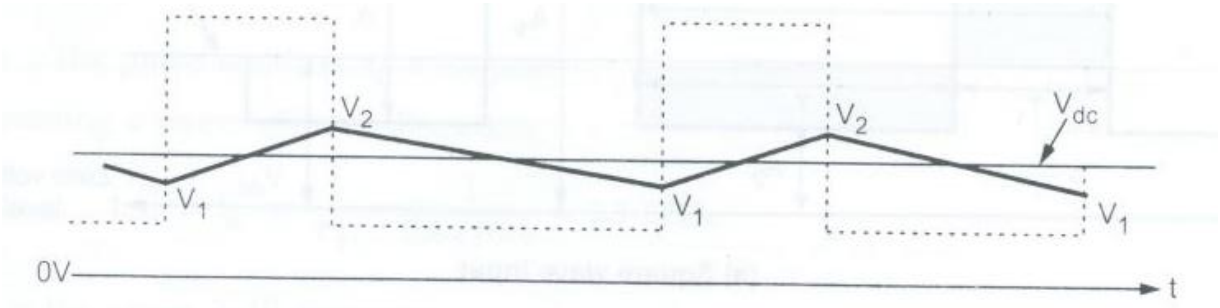


Fig.1.26.Output when time constant is largest

It has been proved earlier that the average value of the voltage across the resistance R is zero independent of the d.c. level present in the input. Hence the d.c. level present in the voltage across the capacitor C remains same as present in the input. Hence the Average value of the output is shown as V_{dc}, in all the waveforms shown in the *Fig. 1.24,* and *1.26.*

Then the equations (1.41) and (1.42) shows that V1=-V2 and solving the two equations simultaneously we get,

$$V_2 = \frac{A}{2}\frac{e^{2x}-1}{e^{2x}+1}$$

(1.43)

$$V_2 = \frac{A}{2}\tanh x$$

Where x=T/4RC

And T=time period of the square wave

1.4.4 Ramp input voltage:

Consider a ramp of slope a applied to the low pass RC circuit. Basically low pass or high pass RC circuit is RC series circuit and according to Kirchhoff's law we can write,

$$V_i = V_R + V_c$$

(1.44)

where V_R =Voltage across Resistance

V_c=Voltage across Capacitor

V_i=input Ramp Voltage

The expression for the voltage across resistance is already obtained and is represented the equation (1.44), in section 1.3.4.

$$V_R = \alpha RC\,(1 - e^{-t/RC})$$

Substituting in (12),

$$\therefore \quad V_C = V_i - \alpha RC\,(1 - e^{-t/RC})$$
$$= \alpha\, t - \alpha RC + \alpha RC\, e^{-t/RC}$$
$$= \alpha\,(t - RC) + \alpha RC\, e^{-t/RC}$$

$$V_o = \alpha\,(t - RC) + \alpha RC\, e^{-t/RC} \qquad (1.45)$$

For minimum distortion, the time constant must be as small as possible, as compared to total ramp time T. In such case output follows input but it gets delayed by one time constant RC from the input. Only at the input such delay is not present, which is nothing but a distortion in the output.

The response is shown in the *Fig. 1.27*. The transmission error is already defined .i﷽ the difference between input and output divided by the input at t = T.

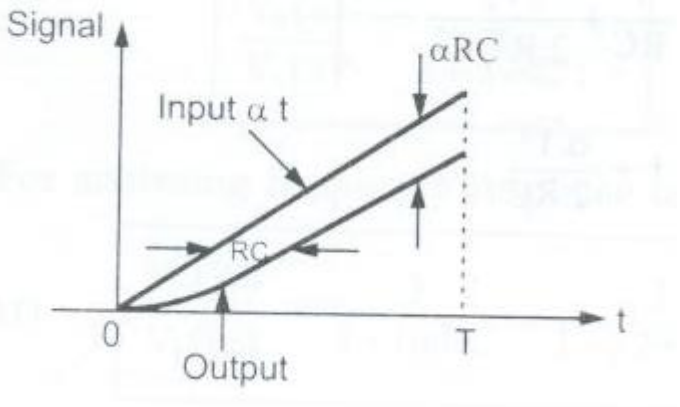


Fig.1.27.Ramp response for low pass RC circuit when RC/T<<1

divided by the input at t = T.

$$e_t = \left.\frac{V_i - V_o}{V_i}\right|_{t=T}$$

Now $V_i = \alpha T$ at $t = T$

and $V_o = \alpha (t - RC) + \alpha RC\, e^{-T/RC}$ at $t = T$

$$\therefore \quad e_t = \frac{\alpha T - \alpha (T - RC) - \alpha RC\, e^{-T/RC}}{\alpha T} = \frac{\alpha T - \alpha T + \alpha RC - \alpha RC\, e^{-T/RC}}{\alpha T}$$

$$= \frac{\alpha RC\left(1 - e^{-T/RC}\right)}{\alpha T}$$

$$\approx \frac{RC}{T} \text{ as } 1 - e^{-T/RC} = 1 \text{ as } RC << T$$

$$\therefore \quad e_t \approx \frac{RC}{T} \qquad \ldots (14\ (a))$$

But $$f_2 = \frac{1}{2\pi RC}$$

$$e_t = \frac{1}{2\pi f_2 T}$$

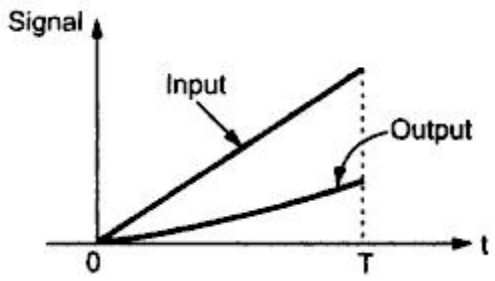


Fig1.28.The Ramp response when RC/T>>1

where f2 = upper 3-dB frequency. When the time constant is large i.e. RC/T >> 1 then the output is distorted in nature. It is shown in the *Fig.1.28*.

Now if in the equation (1.45) the exponential term is expanded in its series form, we get

$$V_o = \alpha (t - RC) + \alpha RC \left(1 - \frac{t}{RC} + \frac{t^2}{2 R^2 C^2} - \cdots\right)$$

$$= \alpha t - \alpha RC + \alpha RC - \alpha t + \frac{\alpha t^2}{2 RC} \ldots\ldots$$

$$V_o = \frac{\alpha t^2}{2 RC} \qquad (1.46)$$

1.4.5 Sinusoidal Input:

The Laplace transform of the low pass RC circuit is shown in the *Fig 1.29*

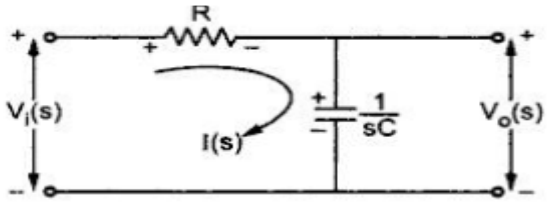


Fig 1.29.

Applying KVL to the circuit,

$$-I(s)R - \frac{I(s)}{sC} + V_i(s) = 0$$

$$\therefore \quad I(s) = \frac{V_i(s)}{R + \frac{1}{sC}} = \frac{sC\,V_i(s)}{1 + sRC} \qquad \ldots (1)$$

$$\text{and} \quad V_o(s) = I(s) \times \frac{1}{sC} = \frac{V_i(s)}{1 + sRC}$$

$$\frac{V_o(s)}{V_i(s)} = \frac{1}{1 + sRC}$$

$$V_{o2}(t) = V_p\, e^{-(t - t_p)/RC}, \qquad \text{for } t > t_p$$

For analyzing frequency response replace by jω

$$\frac{V_o(j\omega)}{V_i(j\omega)} = \frac{1}{1+j\omega RC} = \frac{1}{1+j\,2\pi f RC}$$ ……Frequency domain transfer function

$$A = \left|\frac{V_o(j\omega)}{V_i(j\omega)}\right| = \frac{1}{\sqrt{1+(2\pi f RC)^2}} = \text{Gain of the circuit}$$

Thus as frequency increases, gain decreases .As f→0,A→1 and circuit allows low frequencies to pass.

Upper cut-off frequency: The frequency at which the gain A is $(1/\sqrt{2})$ times its maximum value is called upper cut-off frequency f2 of the circuit.

$$\frac{1}{\sqrt{2}} = \frac{1}{\sqrt{1+(2\pi f_2 RC)^2}}$$

$$\frac{1}{2} = \frac{1}{1+(2\pi f_2 RC)^2}$$

$$2 = 1+(2\pi f_2 RC)^2$$

$$f_2 = \frac{1}{2\pi RC} = \text{Upper cut-off frequency}$$

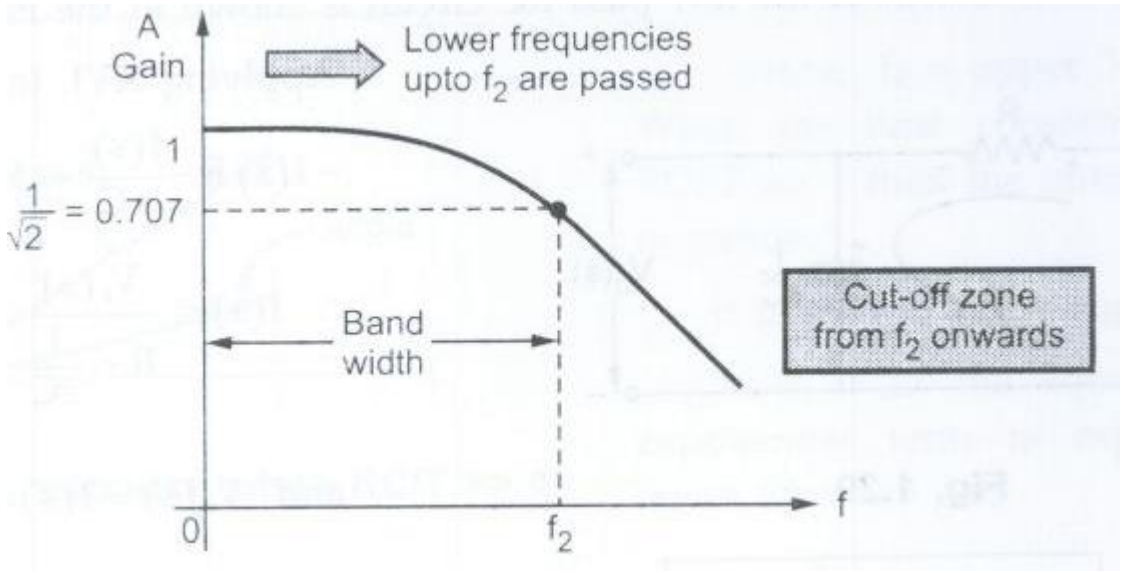


Fig.1.30.Gain frequency plot

Bandwidth: The frequency range 0 to f_2 is the bandwidth of this circuit.

$$BW=f_2-f_1=f_2-0=f_2$$

The frequency f_2 is called upper 3-dB frequency or cutoff frequency or corner frequency.

1.4.6 Low Pass RC Circuit as an Integrator:

For a low pass RC circuit, if the time constant is very large as compared to the time required by the input signal make an appreciable change, the circuit acts asan integrator.Under this case, the drop across C is negligible compared to drop across R. Thus the entire input Vi(t) can be assumed to be appearing across R. Then the current i is given by,

$$V_r = V_i = iR$$

$$I = V_i/R$$

$$V_o = V_C = \frac{1}{C}\int i\,dt$$

Hence the output which is voltage across the capacitor is,

$$V_o = \frac{1}{RC}\int V_i(t)\,dt$$

Thus the output is proportional to integration of input.

This can be verified for the various inputs discussed earlier. For a square wave, when the input is constant during the period 0 to T1, and T1 to T2, then the output is linear it nature when RC/T>>1. This is because s K dt= Kt where K is constant. This is shown ii the *Fig.1.26*. As the time constant decreases, the output deviates from the true integration.

In case of ramp input, the input is linear αt and αt is αt2/2. It has been proved and shown by the equation (14(c)) that Vo α t2 i.e. the integration of the input, when RC/T >> 1. This is shown in the *Fig.1.28.*

Advantages of Integrators:

Integrators are more preferred over differentiators because,

1 The gain of an integrator decreases as the frequency hence easy to stabilize. The gain of the differentiator increases as the frequency hence suffers from the problems of stability.

2. Due to high gain at high frequency, the noise problems are severe for differentiators. An integrator is less sensitive to the noise.

3. The differentiator overloads the amplifier if input changes rapidly. This is not the case for an integrator.

4. With an integrator, initial conditions can be easily introduced in the circuit.

Similar to the RC circuits, the RL circuits are also categorized as:

1) High pass RL circuit

2) Low pass RL circuit

Let us steady the effect of high pass RL circuit on the nonsinusoidal inputs, first.

1.5. High Pass RL Circuit:

Consider the RL circuit shown in the *Fig.1.31.*

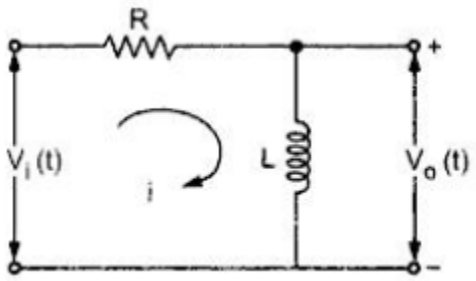


Fig.1.31.High pass RL circuit

The output is taken across the inductor L.The output is denoted as V0(t) while the input is denoted as Vi(t).Initially there is no current through the inductor L.The inductive reactance offered by the inductor L depends on the input frequency and is given by

$$X_L = 2\pi fL \quad (1)$$

The reactance XL is directly proportional to the frequency.

Thus the output which is a voltage across inductor falls to Zero. The behavior of inductor as a short circuit is true for certain low frequency range and for this output is Zero. **And hence in this circuit, low frequency components cannot reach to the output.**

Let us consider the response of high pass RL circuit to nonsinusoidal waveforms.

1.5.1 Step Input Voltage:

Consider a step of magnitude A is applied to the high pass RL circuit .For a RL circuit the time constant is dependent on the values of R and L and is given by,

$$\tau = \frac{L}{R} = \text{time constant} \quad (2)$$

The voltage across the inductor L is given by L(di/dt) . Now when the voltage changes instantaneously, the current tries to change instantaneously .Hence di/dt→∞ and hence L(di/dt)→∞.But practically the voltage across inductor cannot be infinite. This indicates that though voltage changes instantly, current through inductor cannot change instantaneously .It takes finite time to change the current and to achieve its steady state value.

In case of step input, there is abrupt change in the input voltage from 0 to A volts at t=0. But just after t=0 i.e, at $t=0^+$, current through circuit is zero as current through the inductor cannot change instantaneously .**Hence the entire voltage of A volts appears across the inductor, as voltage across inductor can change instantly.**

Hence initially the output voltage is A volts.

As the time approaches to ∞, the input voltage is constant at A volts. Hence current achieves a steady state value equal to A/R amperes. As current is constant,di/dt is zero hence the voltage across inductor which is Ldi/dt becomes zero. Thus the output voltage is zero in the steady state.

The drop in the output from A to zero is exponential in nature. Thus for the high pass RL circuit,

$$V_i = A \text{ volts and } V_f = 0 \text{ V}$$

Using the basic equation (6) we can write,

$$V_o(t) = A\, e^{-t/\tau} \quad (3)$$

Where $\tau = \frac{L}{R}$ = time constant

The step response of high pass RL circuit is shown in the *Fig1.32*

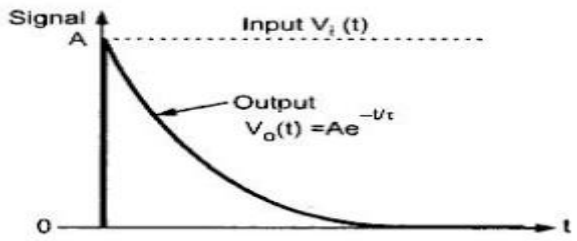


Fig1.32.Step responses high pass RL circuit

1.6. ATTENUATORS:

Attenuators are resistive networks, which are used to reduce the amplitude of the input signal. The simple resistor combination of *Fig1.33 (a)* would multiply the input signal by the ratio $\alpha = R_1R_2/(R_1 + R_2)$ independently of the frequency. If the output of the attenuator is feeding a stage of amplification, the input capacitance C_2 of the amplifier will be the stray capacitance shunting the resistor R2 of the attenuator and the attenuator will be as shown *Fig.1.33 (b),* and the attenuation now is not independent of frequency. Using Thevenins theorem, the circuit in *Fig.1.33 (b)* may be replaced by its equivalent circuit shown *Fig.1.33(c),* in which R is equal to the parallel combination of R_1 and R_2. Normally R1 and R2 must be large so that the nominal input impendence of the attenuator is large enough to prevent loading down the input signal. But if R, and R: are large, the rise time $t_r = (R_1R_2/R_1+R_2)\, C_2$ will be large and a large rise time is normally unacceptable.

The attenuator may be compensated by shunting R_1 by a capacitor C_1 as shown in *Fig.1.33 (d),* so that its attenuation is once again independent of frequency. The

circuit has been drawn in *Fig.1.33 (e*) to suggest that the two resistors and the two capacitors may be viewed as the four arms of a bridge. If $R_1C_1 = R_2C_2$. The bridge will be balanced and no current will flow in the branch connecting the point X to the point Y. For the purpose of computing the output, the branch X-Y may be omitted and the output will again be equal to αvi independent of the frequency. In practice, $_{C1}$ will ordinarily have to be made adjustable,

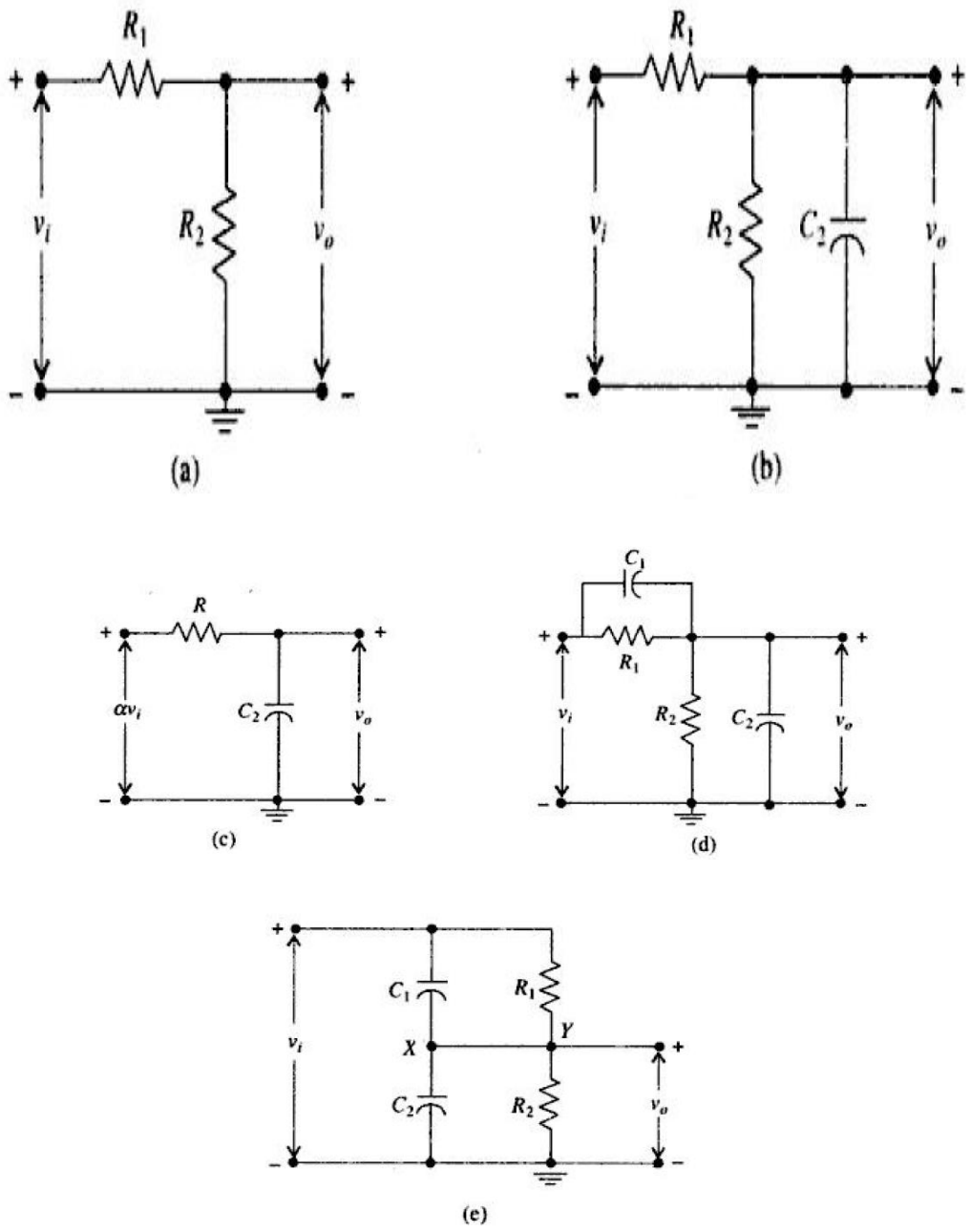


Fig. 1.33 An attenuator (a) ideal circuit (b) actual circuit (c) equivalent circuit (d) compensated attenuator (e) compensated attenuator redrawn as a bridge

Suppose a step signal of amplitude V volts is applied to the circuit. As the input changes abruptly by V volts at t = 0, the voltages across C_I and C_2, will also change

Since the same current flows through the capacitors C_1 and C_2, we have

charge accumulated in capacitor $C_1 = \int_{0^-}^{0^+} i(t)\,dt = q$

Initial voltage across $C_1 = \frac{q}{C_1} = V_1$

Charge accumulated in capacitor $C_2 = \int_{0^-}^{0^+} i(t)\,dt = q$

Initial voltage across $C_2 = \frac{q}{C_2} = V_2 = v_o(0^+)$

Input signal, $V = V_1 + V_2 = \frac{q}{C_1} + \frac{q}{C_2} = q\left(\frac{C_1 + C_2}{C_1 C_2}\right)$

$$\frac{v_o(0^+)}{V} = \frac{\frac{q}{C_2}}{q\left(\frac{C_1 + C_2}{C_1 C_2}\right)} = \frac{C_1}{C_1 + C_2}$$

$$v_o(0^+) = V\frac{C_1}{C_1 + C_2} = v_i\frac{C_1}{C_1 + C_2}$$

Abruptly. This happens because at r = 0. The capacitors act as short-circuits and a very large (ideally infinite) current flows though the capacitors for an infinitesimally small time so that a finite charge q= i(t) dt is delivered to each capacitor. The initial output voltage is determined by the capacitors.

The final output voltage is determined by the resistors RI and R2, because the capacitors C, and C, act as open circuits for the applied dc voltage under steady-state conditions. Hence

$$v_o(\infty) = V\frac{R_2}{R_1 + R_2} = v_i\frac{R_2}{R_1 + R_2}$$

Looking back from the output terminals (with the input short circuited) we see a resistor $R = R_1R_2/(R_1 + R_2)$ in parallel with $C = C_1 + C_2$. Hence the decay or rise of the output (when the attenuator is not perfectly compensated) from the initial to the final value takes place exponentially with a time constant r = RC. The responses of

an attenuator for C_I equal to, greater than, and less than R_2C_2/R.

Perfect compensation is obtained if $v_0(0+) = v_0(\infty)$, that is, if the rise time $t_r = 0$

$$\therefore \quad V\frac{C_1}{C_1+C_2} = V\frac{R_2}{R_1+R_2}$$

$$\text{i.e.} \quad R_1C_1 + R_2C_1 = R_2C_1 + R_2C_2$$

$$\text{i.e.} \quad R_1C_1 = R_2C_2 \quad \text{or} \quad C_1 = \frac{R_2C_2}{R_1}$$

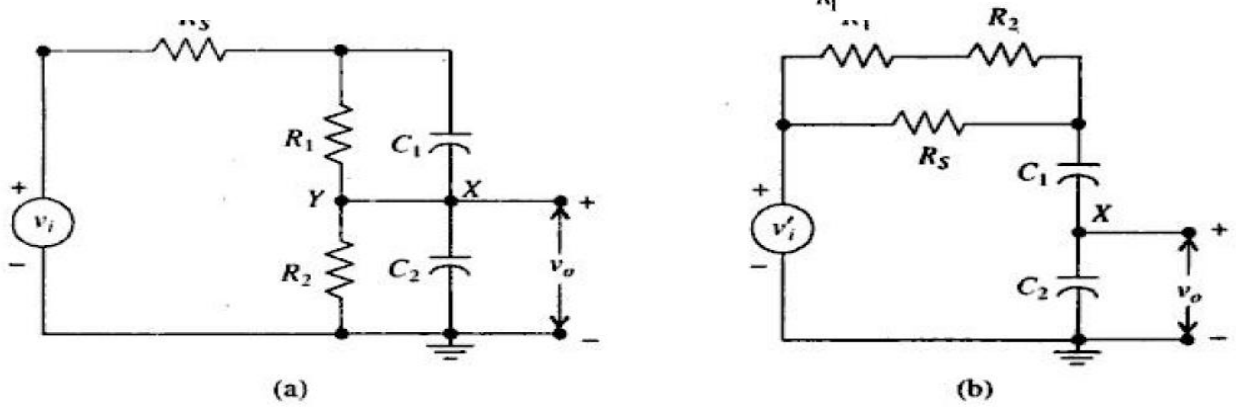


Fig.1.34 (a) Compensated attenuator including source resistance R_s and (b) its equivalent circuit with $V_i' = V(R_1+R_2)/R_s+R_1+R_2$.

The input to the attenuator will be an exponential of time constant RSC', where C' is the capacitance of the series combination of C1 and C2. i.e. C' = C1C2/(C1 + C2). It is this exponential waveform rather than the step, which the attenuator will transmit faithfully. If the generator terminals were connected directly to the terminals to which the attenuator output is connected, the generator would see a capacitance C2. In this case the waveform at these terminals would be an exponential with time constant r = RSC2. When the attenuator is used, the time constant is r' = RSC'.

$$\text{Since } \tau'/\tau = C'/C = C1/(C1+C2)$$

An improvement in waveform results. For example, if the attenuation is equal to 10 ($\alpha = 1/10$) then the rise time of the waveform would be divided by a factor 10.

1.6.1 Application of Attenuator as a CRO Probe:

To measure the signal at a point in the circuit, the input terminals of the oscilloscope are connected to the signal point. Normally the point at which the signal is available will be at some distance from the oscilloscope terminals and if the signal appears at a high impedance level, a shielded cable is used to connect the signal to the oscilloscope. The shielding is necessary in this case to isolate the input lead from stray fields such as those of the ever present power line. The capacitance seen looking into several feet of cable may be as high as 100 to 150 pF. This combination of high input capacitance together with the high output impedance of the signal source will make it impossible to make faithful observations of waveforms. A probe assembly, which permits the use of shielded cable and still keeps the capacitance low, is indicated in Figure 1.51.

1.7 RL Circuits:

In Sections 1.2 and 1.3, we discussed the behavior of RC low-pass circuits for various types of input waveforms. Suppose the capacitor and the resistor R in those circuits are replaced by a resistor R' and an inductor L respectively, then, if the time constant UR' equals the time constant RC, all the preceding results remain unchanged.

When a large time constant is required, the inductor is rarely used because a large value of inductance can be obtained only with an iron-core inductor which is physically large, heavy and expensive relative to the cost of a capacitor for a similar application. Such an iron cored inductor will be shunted with a large amount of stray distributed capacitance. Also the nonlinear properties of the iron cause distortion, which may be undesirable. If it is required to pass very low frequencies through a circuit in which L is a shunt element, then the inductor may become prohibitively large. Of course in circuits where a small value of R' is tolerable, a more reasonable value of inductance may be used. In low time constant applications, a small inexpensive air-cored inductor may be used. *Fig.1.24 (a)* and *1.24(b)* show the RL Low-pass and high-pass circuits. At very low frequencies the reactance of the inductor is small, so the output across the resistor R' is almost equal to the input. As the frequency increases, the reactance of the inductor increases and so the signal is attenuated. At very high frequencies the output is almost equal to zero. So the circuit in *Fig.1.24 (a)* acts as a low pass filter.

The circuit of *Fig.1.24 (b)* acts as a high-pass circuit because at low frequencies the output is very small and the output increases as the frequency increases and at high frequencies the output is almost equal to the input.

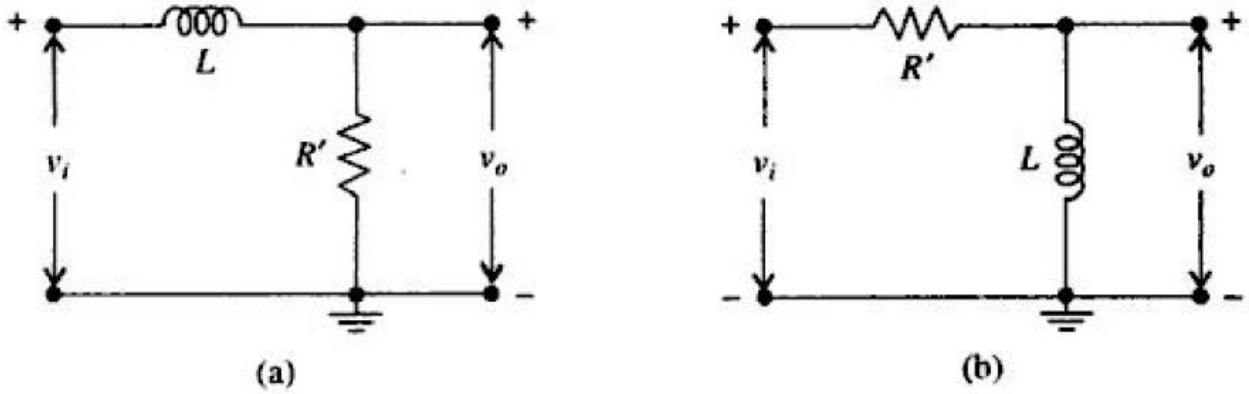


Fig.1.24. (a) RL Low passes Circuit (b) RL High Pass circuit

1.8 RLC Circuits:

1.8.1. RLC Series Circuit:

Cosider a Series RLC circuit shown in Fig.1.25.

Writing the KVL around the loop,we obtain

Taking the laplace Transform on both sides

The transfer function of the circuit of *Fig.1.25*

The roots of the characteristic equation s1 and s2 are the values of s satisfying the equation. If (R/2L)2>1/LC i.e.R> $\frac{1}{2}\sqrt{LC}$,both the roots are real and different. The circuit is ( ) and there are no oscillations in the output. (R/2L)2=1/LC,i.e $R = \frac{1}{2}\sqrt{LC}$ both the roots are real and equal. The circuit is critically damped. If (R/2L)2<1/LC In the RL circuit shown in *Fig.1.24 (b)*, to

include the effect of coil winding capacitance, output capacitance and gray capacitance to ground, a capacitor is added across the output. So, the RLC circuit shows in *Fig.1.25 (a)* results. In terms of a current source, the equivalent circuit has shown in *Fig.1.25 (b)* results.The transfer function of the network of *Fig.1.25 (a)* is

$$\frac{V_o(s)}{V_i(s)} = \frac{1}{RC}\left(\frac{s}{s^2 + \frac{1}{RC}s + \frac{1}{LC}}\right)$$

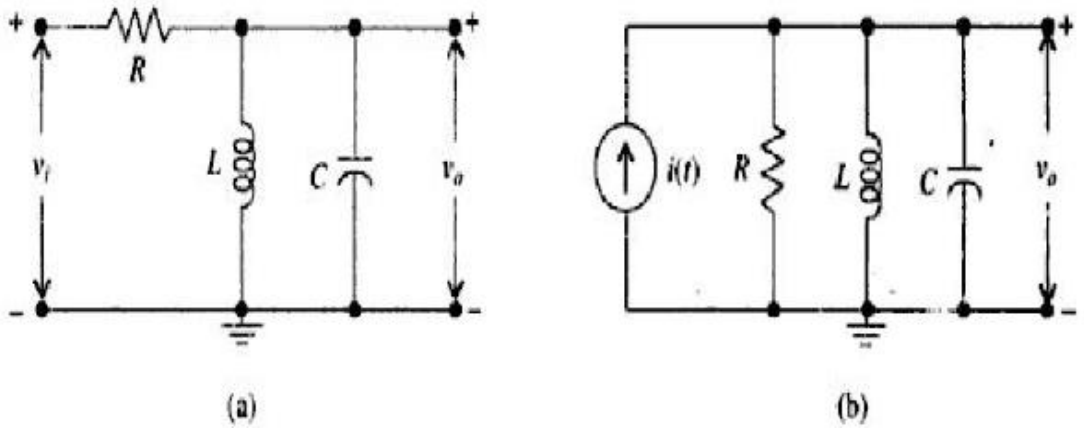


Fig. 1.25 (a) v_i is applied through R to a parallel LC circuit and (b) Parallel RLC circuit driven by a current source

The roots of the characteristic equation are

$$s_1, s_2 = -\frac{1}{2RC} \pm \sqrt{\left(\frac{1}{2RC}\right)^2 - \frac{1}{LC}}$$

These are also the characteristic roots of the network in *Fig.1.25 (b).*

The circuit is over damped if $R < \frac{1}{2}\sqrt{L/C}$.

Critically damped if $R = \frac{1}{2}\sqrt{L/C}$

And Under damped if R> $\frac{1}{2}\sqrt{L/C}$

The response to the voltage across RLC parallel circuit is similar to that to the

current through the RLC series circuit with the difference that the input to the RLC parallel circuit is a step current.

In the series RLC network, the current response to a step input voltage ultimately dies to zero because of the capacitor in series. In the parallel RLC circuit the voltage across the RLC network is zero because of the inductance.

1.9. Ringing Circuit:

In a previous section it was given that to obtain a pulse from step voltage (peaking) the circuit should operate in the neighborhood of critical damping. In some applications almost undamped oscillations are required. A circuit which can provide as nearly undamped oscillations as possible is called a *ringing circuit*. If the damping is very small the circuit will rig for many cycles. Many times the value of Q of a circuit which has to ring for a given number N of cycles before the amplitude increase to 1/e of its initial value needs to be known. This is given by $Q=\pi N$.

Thus a circuit Q=12 will ring for $Q/\pi=4$ cycles before the amplitude of the oscillations decreases to 37% of its initial value. A ringing circuit may be used to generate a sequence if pulses regularly spaced in time. These pulses find applications in many timing operations.

UNIT-2

NON-LINEAR WAVE SHAPING

2.1. INTRODUCTION:

Non linear wave shaping:

The process by which the shape of sinusoidal and non-sinusoidal wave forms is altered when they are passed through a non-linear network.

Non linear wave shaping circuit:

It is a circuit which provides non-sinusoidal output of a given sinusoidal input. The non-linear network comprises of both linear and non-linear elements.

Linear Elements: Resistor, Inductor, Capacitor.

Non-Linear Elements: Transistors, Diodes, Vacuum Tubes etc..,

* Diode plays a very important role in these non-linear wave shaping circuits.

Examples for on-linear wave shaping circuits are

1. Clipping Circuits.
2. Clamping Circuits.

2.2. Clipping Circuits:

It is a circuit which removes the undesired part of wave form and transmits only the desired part of signal, which is above or below some practical reference level.

* These circuits are also called as *voltage limiters* (or) *current limiters* (or) *slicers* (or) *amplitude selector.*

* This circuits may use diodes (or) transistors.
* Clipping may be done in two ways
  1. Single level clipping.
  2. Two level clipping.

Ex: The best example for clipper circuit is Half-Wave rectifier.

Based on orientation of diode in circuit, the clippers are mainly classified as two types

1. Series Clipper.
2. Parallel Clipper.

2.2.1. Series Clipper:

The clipper circuit in which diode is connected in series with load is called series clipper.

2.2.2. Parallel Clipper:

The clipper circuit in which diode is connected in parallel with load is called Parallel clipper.

Circuit Models of a Diode:-

The diode is required to be replaced by equivalent circuit model to analysis the non-linear network. This equivalent circuit is called Circuit model of a diode. There are 3 methods of replacing diode by its circuit model. They are

1. Practical Diode Model.

2. Ideal Diode model.

3. Piece Wise Linear Diode Model.

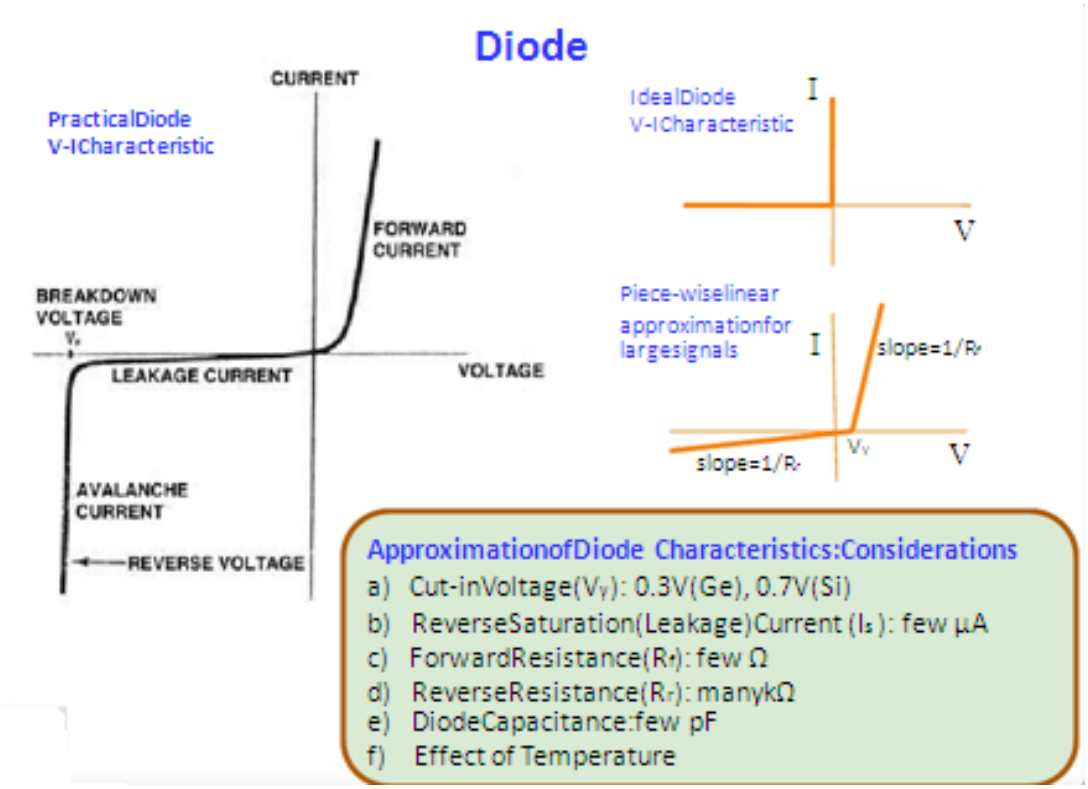


Fig 2.1. Ideal and practical characteristics of diode.

2.2.3. Diode Clippers:

A Clipper circuit in which active component is diode is called diode clipper.

According to non-linear devices used, clippers may be classified as

- **Diode clippers** and
- **Transistor clippers**.

According to biasing, the clippers may be classified as

- **Unbiased clippers and**
- **Biased clippers.**

According to configuration used the clippers may be

- **Series diode clippers**

- **Parallel or shunt diode clippers**
- **A series combination of diode, resistor and reference supply**
- **Multi-diode clippers consisting of several diodes, resistors and reference voltages**
- **Two emitter-coupled transistors operating as an over-driven difference amplifier.**

According to level of clipping the clippers may be

- **Positive clippers**
- **Negative clippers**
- **Biased clippers and**
- **Combination clippers**

The basic components required for a clipping circuit are – an ideal diode and a resistor. In order to fix the clipping level to the desired amount, a dc battery must also be included. When the diode is forward biased, it acts as a closed switch, and when it is reverse biased, it acts as an open switch. Different levels of clipping can be obtained by varying the amount of voltage of the battery and also interchanging the positions of the diode and resistor.

Depending on the features of the diode, the positive or negative region of the input signal is "clipped" off and accordingly the diode clippers may be positive or negative clippers.

There are two general categories of clippers: series and parallel (or shunt). The series configuration is defined as one where diode is in series with the load, while the shunt clipper has the diode in a branch parallel to the load.

2.2.4. Positive Clipper and Negative Clipper:

2.2.4.1. Positive Diode Clipper:

In a positive clipper, the positive half cycles of the input voltage will be removed. The circuit arrangements for a positive clipper are illustrated in the *Fig.2.2.*

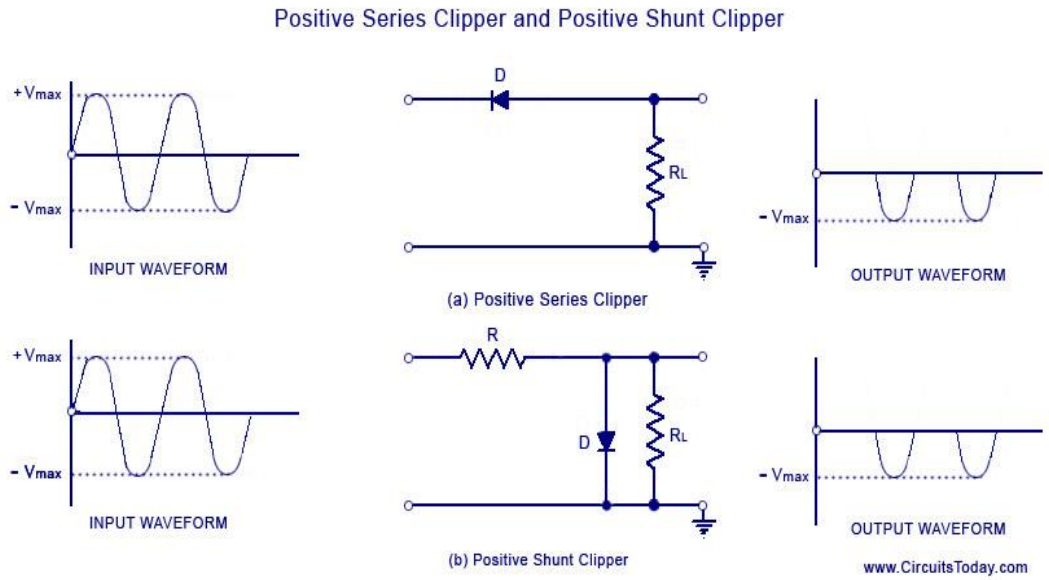


Fig 2.2 Positive Diode Clippers

As shown in the figure, the diode is kept in series with the load. During the positive half cycle of the input waveform, the diode 'D' is reverse biased, which maintains the output voltage at 0 Volts. Thus causes the positive half cycle to be clipped off. During the negative half cycle of the input, the diode is forward biased and so the negative half cycle appears across the output.

In *Fig.2.2 (b),* the diode is kept in parallel with the load. This is the diagram of a positive shunt clipper circuit. During the positive half cycle, the diode 'D' is forward biased and the diode acts as a closed switch. This causes the diode to conduct heavily. This causes the voltage drop across the diode or across the load resistance R_L to be zero. Thus output voltage during the positive half cycles is zero, as shown in the output waveform. During the negative half cycles of the input signal voltage, the diode D is reverse biased and behaves as an open switch. Consequently the entire input voltage appears across the diode or across the load resistance R_L if R is much smaller than R_L Actually the circuit behaves as a voltage divider with an output voltage of $[R_L / R+ R_L]$

$$V_{max} = -V_{max} \text{ when } R_L >> R$$

2.2.4.2. Negative Diode Clipper:

The negative clipping circuit is almost same as the positive clipping circuit, with only one difference. If the diode in *Fig.2.2 (a) and (b)* is reconnected with reversed polarity, the circuits will become for a negative series clipper and negative shunt clipper respectively. The negative series and negative shunt clippers are shown in *Fig.2.3 (a) and 3(b)* as given below.

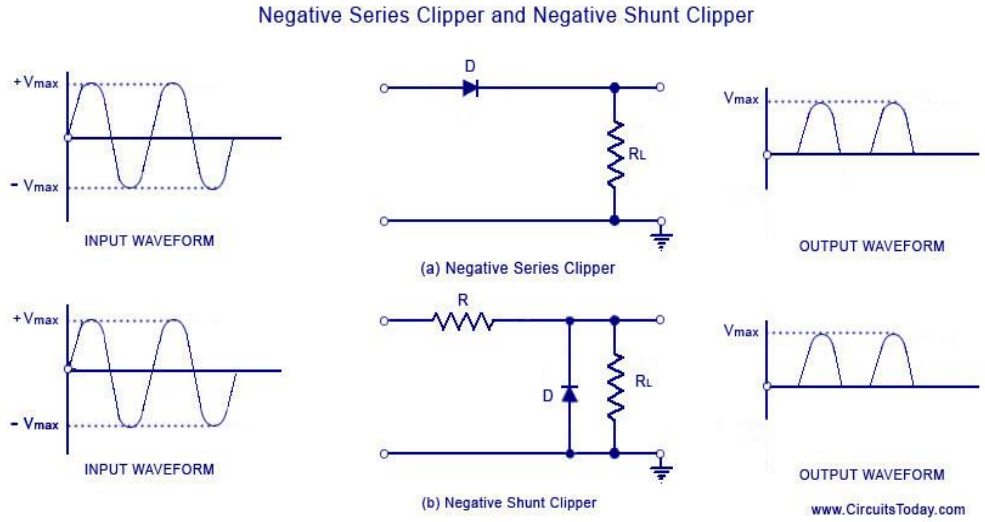


Fig 2.3 Negative Diode Clipper.

In all the above discussions, the diode is considered to be ideal one. In a practical diode, the breakdown voltage will exist (0.7 V for silicon and 0.3 V for Germanium). When this is taken into account, the output waveforms for positive and negative clippers will be of the shape shown in the *Fig 2.4.*

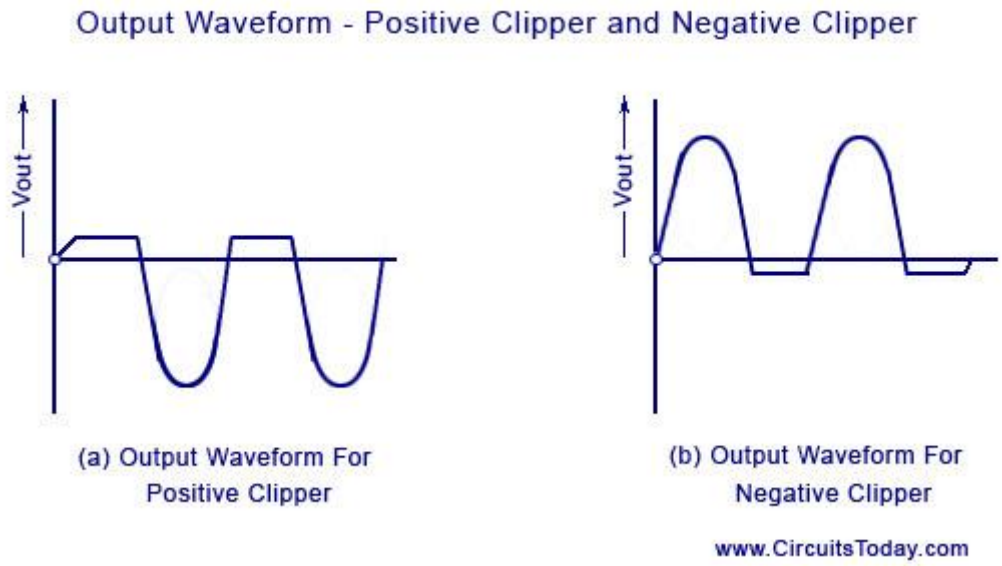


Fig 2.4 Output waveform of Positive and Negative Clippers

2.2.5. Biased Positive Clipper and Biased Negative Clipper:

A biased clipper comes in handy when a small portion of positive or negative half cycles of the signal voltage is to be removed. When a small portion of the negative half cycle is to be removed, it is called a biased negative clipper. The circuit diagram and waveform is shown in the *Fig.2.5*.

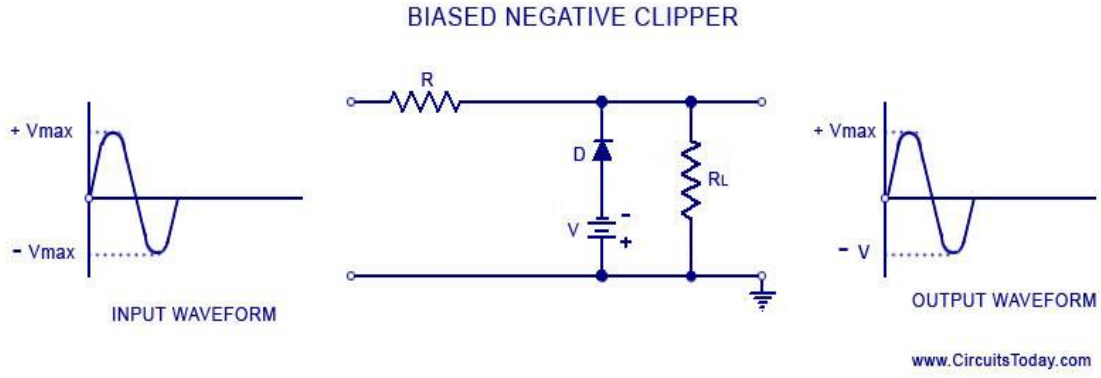


Fig 2.5 Biased Negative Clippers

In a biased clipper, when the input signal voltage is positive, the diode 'D' is reverse-biased. This causes it to act as an open-switch. Thus the entire positive half cycle appears across the load, as illustrated by output waveform *Fig.2.5.* When the input signal voltage is negative but does not exceed battery the voltage 'V', the diode 'D' remains reverse-biased

and most of the input voltage appears across the output. When during the negative half cycle of input signal, the signal voltage becomes more than the battery voltage V, the diode D is forward biased and so conducts heavily. The output voltage is equal to '- V' and stays at '- V' as long as the magnitude of the input signal voltage is greater than the magnitude of the battery voltage, 'V'. Thus a biased negative clipper removes input voltage when the input signal voltage becomes greater than the battery voltage. Clipping can be changed by reversing the battery and diode connections, as illustrated in *Fig.2.6.*

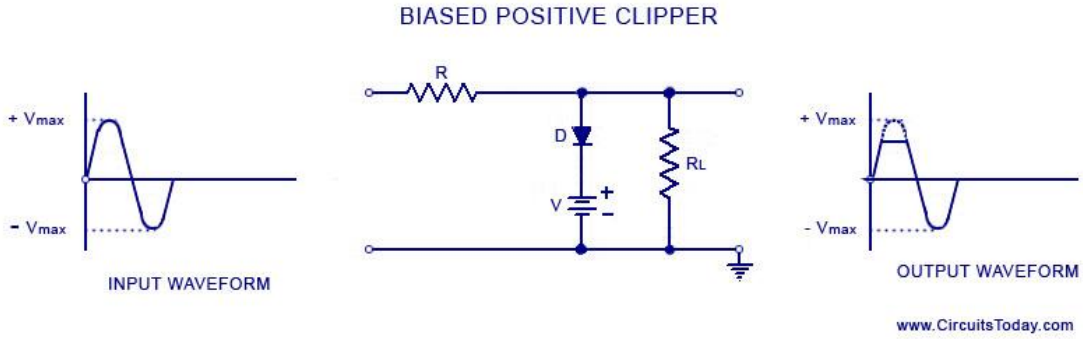


Fig 2.6 Biased Positive Clippers

Some of other biased clipper circuits are given below in the *Fig.2.7.* While drawing the wave-shape of the output basic principle discussed above are followed. The diode has been considered as an ideal one.

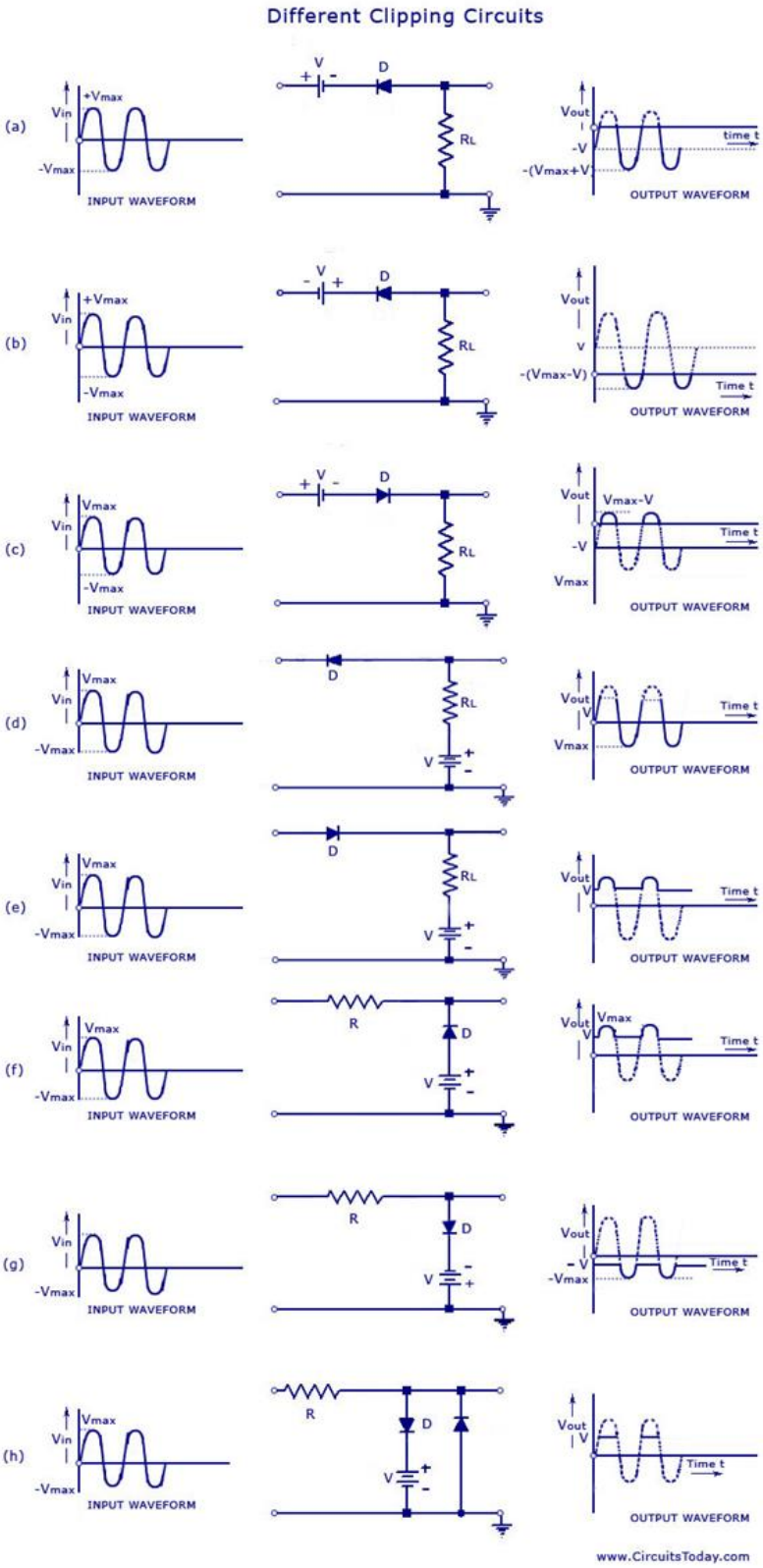


Fig 2.7 Different Clipper Circuits

2.2.6. Combination Clipper:

When a portion of both positive and negative of each half cycle of the input voltage is to be clipped (or removed), combination clipper is employed. The circuit for such a clipper is given in the *Fig.2.8.*

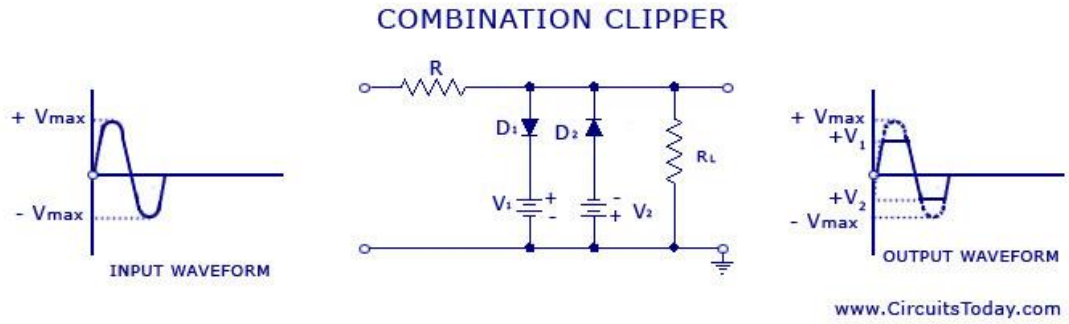


Fig 2.8 Combination Clipper.

The action of the circuit is summarized below. For positive input voltage signal when input voltage exceeds battery voltage '+ V_1'$_{diode}$ D_1 conducts heavily while diode 'D_2'is reversed biased and so voltage '+ V_1'appears across the output. This output voltage '+ V_1'stays as long as. The input signal voltage exceeds '+ V_1'. On the other hand for the negative input voltage signal, the diode 'D_1' remains reverse biased and diode 'D_2' conducts heavily only when input voltage exceeds battery voltage 'V_2' in magnitude. Thus during the negative half cycle the output stays at '- V_2'so long as the input signal voltage is greater than '-V_2'.

2.2.7. Drawbacks of Series and Shunt Diode Clippers:

- In series clippers, when the diode is in 'OFF' position, there will be no transmission of input signal to output. But in case of high frequency signals transmission occurs through diode capacitance which is undesirable. This is the drawback of using diode as a series element in such clippers.
- In shunt clippers, when diode is in the 'off condition, transmission of input signal should take place to output. But in case of high frequency input signals, diode capacitance affects the circuit operation adversely and the signal gets attenuated (that is, it passes through diode capacitance to ground).

2.3. Transistor Clipping Circuits:

The transistor has two types of linearity's — one linearity happens when the transistor passes from cut-in region to the active region. The other linearity occurs when the transistor passes from the active region to the saturation region. When any input signal passes through the transistor, across the boundary between cut-in region and active region, or across the boundary between the active region and saturation region, a portion of the input signal waveform will be clipped off. Portion of the input waveform which keeps the transistor in the active region shall appear at the output without any distortion. In such a case, it is the input current rather than the input voltage that should have the waveform of the signal of interest. Obvious reason is that over a large signal excursion in the active region, the transistor output current responds linearly to the input current but is related quite non-linearly to the input voltage. Therefore, a current drive is used in a transistor clipper, as illustrated in the *Fig2.9.*

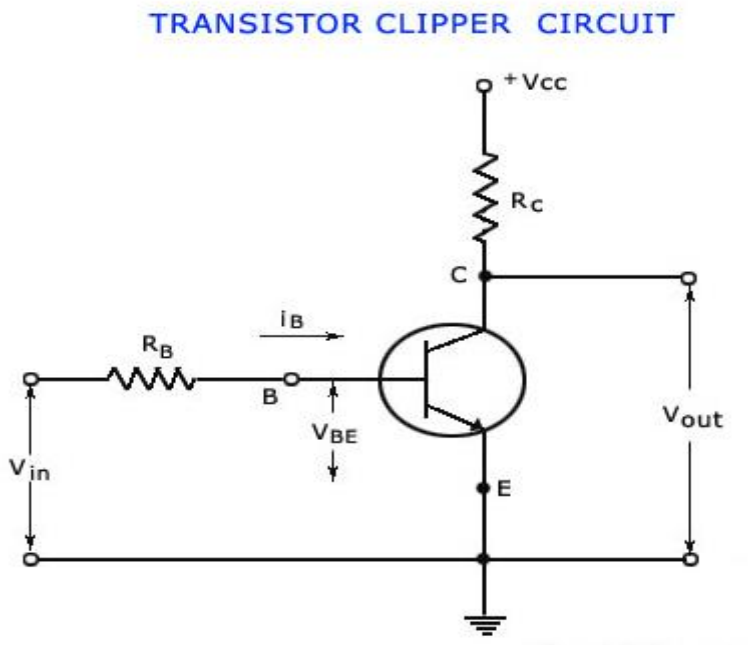


Fig 2.9 Transistor Clipper Circuit.

In the active region, the value of the resistor R_B must be large enough when compared to the input resistance of the transistor. The input base current will have the waveform of input voltage and

$i_B = v_{in}$ – base-to-emitter cut-in voltage / R_B

Waveforms for the transistor clipper for ramp input are shown in the *Fig2.10.*

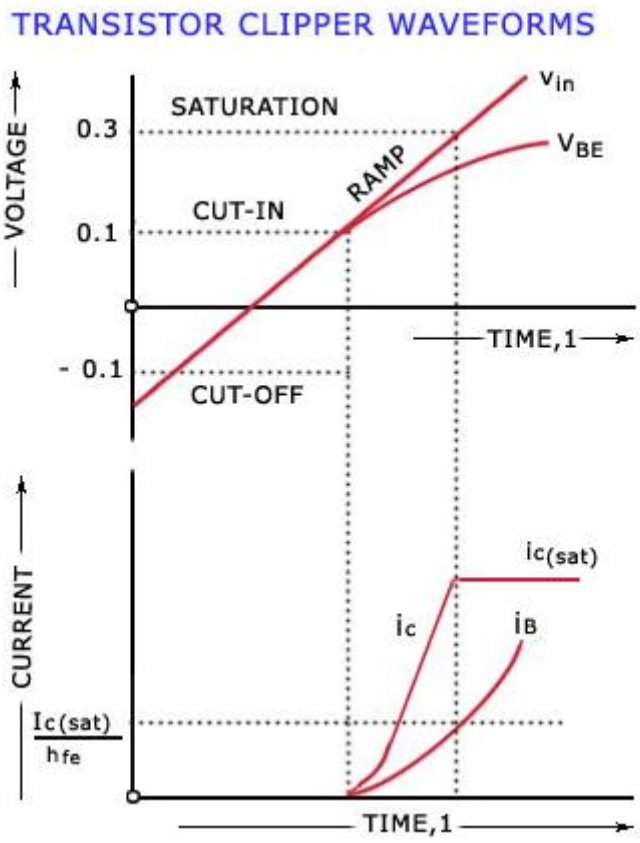


Fig.2.10 Transistor Clipper Waveforms

The voltages are considered for a germanium transistor. The transistor will be working in the cut-off region at -0.1 V. When the voltage reaches 0.1 V, the transistor t starts conducting and will switch to the active region. When the voltage increases to 0.3 V, the transistor switches to the saturation region and the base-emitter voltage V_{BE} is limited to 0.3 V. As the transistor switches from the cut-off region to active region and then into saturation, the input base current i_B increases slowly. In the graph, the output current (collector current, I_c) will be of the same form as the input base current., when the transistor works in the active region. In saturation region, however collector current will become constant and becomes $Ic(_{sat})$.

Waveforms for the transistor clipper for sinusoidal input are shown in the *Fig.2.11.*

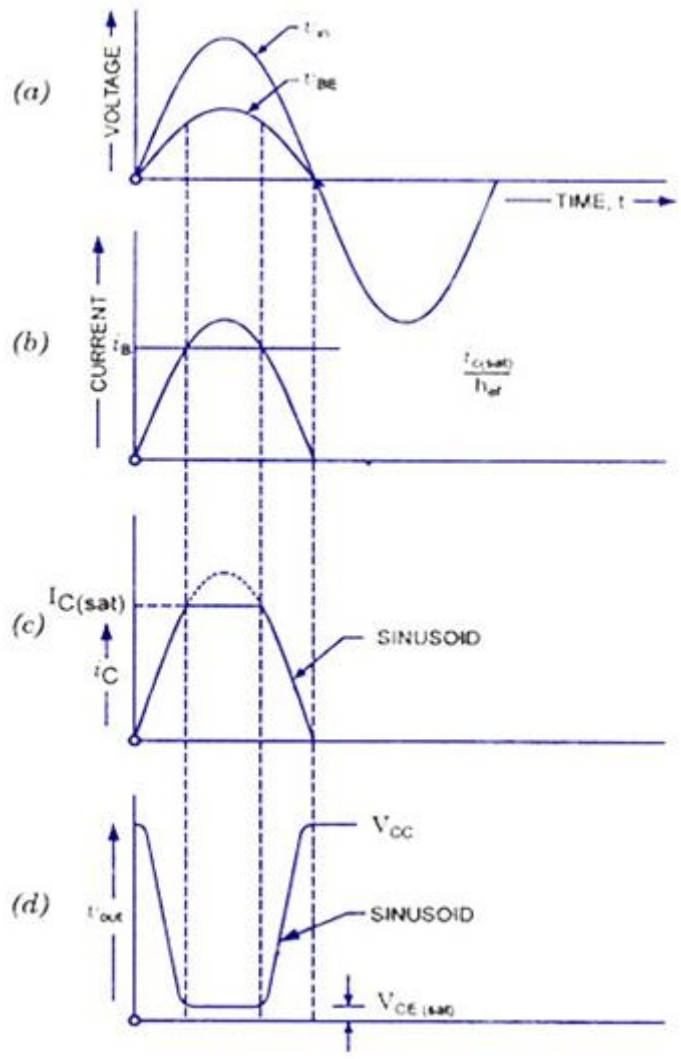


Fig.2.11 Transistor Clipper Waveform With Sinusoidal Input

2.3.1. EMITTER COUPLED CLIPPER:

The emitter coupled clipper uses two transistors. The emitter coupled clipper circuit is that circuit in which emitters of the transistors are coupled together. It has two clipping levels and hence double ended clipper. The *Fig2.12.* Shows the circuit diagram. It uses two transistors Q_1 and Q_2. The emitters of two transistors are coupled together and connected to $-V_{EE}$ through common emitter resistance Re. This carries current $I=I_1+I_2$. The constant voltage V_{BB2} is supplied to base of Q_2 such that when Q_1 is OFF, then Q_2 is in active region.

Operation:

Initially the input voltage V_i is negative which ensures that Q_1 is in cut-off. At that time, V_{BB2} keeps Q_2 in active region. When Q_1 is in cut-off, only Q_2 carries the entire current.

As V_i increases, at some level, Q_1 becomes active from cut-off. At this time, both the transistors will carry the currents. As both the transistors are in active region, the input waveform appears at the output. This is amplified but not inverted. As V_i further increases due to common emitter circuit, emitter follows the base of Q_1. Hence emitter current increases. This increases the drop across Re. Due To this, emitter E_2 of Q_2 becomes more positive with respect to base B_2. As V_{BB2} is constant, at a particular instant, E_2 voltage becomes so much positive which drives Q_2 to cut-off from saturation. This causes second clipping in the output.

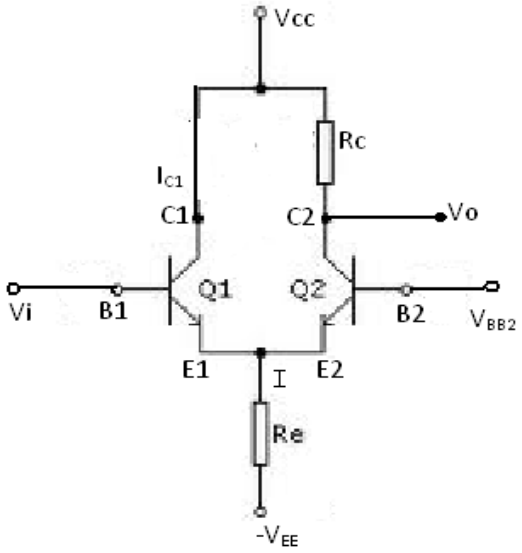


Fig.2.12 Emitter Coupled Clipper

The total range ΔVo of output over which output follows the input is IRc, where I is sum of the currents in Q_1 and Q_2 when both are in active region.

The part of the waveform to be transmitted at the output can be selected by,

1. Adjusting biasing voltage on which V_i is superimposed
2. Adjusting the voltage V_{BB2}

Transfer characteristics of emitter coupled clipper:

The emitter current I is given by,

$$I = I_1 + I_2 = \frac{V_{BB2} + V_{EE} - V_2}{R_e} \qquad (1)$$

This is obtained by applying KVL to B-E loop of Q2

Now change in V2 is hardly 0.2V as transistor changes from cut-in to saturation. This is very small compared to the V_{BB2}+V_{EE}. Hence when both devices are in active region then I is almost constant asV_{BB2}, V_{EE} and R_e are constants.

When Q1 is OFF,I_1=0 and I_2=I. This decides the lower level of o/p given by,

$$V_{oL} = V_{CC} - I_{C2}R_C \tag{2}$$

When Q2 is OFF, I2=0 and I1=I. This decides the upper level of o/p given by,

$$V_{oU} = V_{CC} \tag{3}$$

Applying KVL to input, V1, V2 and V_{BB2} we get

$$V_{BB2} - V_2 + V_1 - V_i = 0$$

$$V_{BB2} - V_2 + V_1 = V_i \tag{4}$$

The current varies exponentially with base –emitter voltage V1 or V2. Hence the change in output level from V_{oL} to V_{oU} is exponential in nature.

From the relation between transistor current and base-emitter voltage, it can be written as,

$$V_i = V_{BB2} + \eta V_T ln\left[\frac{I_1}{I_2}\right] \tag{5}$$

Now upper input level V_{iU} corresponds to I2= 0.1 I and I1= 0.9I

While lower input level V_{iL}, corresponds to I1=0.1I and I2=0.9 I

Using in (5)

$$V_{iU} = V_{BB2} + \eta V_T ln\left[\frac{0.9I}{0.1I}\right] = V_{BB2} + \eta V_T ln9$$

$$V_{iL} = V_{BB2} + \eta V_T ln\left[\frac{0.1I}{0.9I}\right] = V_{BB2} - \eta V_T ln9$$

Hence the total voltage input swing ΔVi which produces the swing of IC2Rc in the output is

$$\Delta V_i = V_{iU} - V_{iL} = 2\,\eta V_T ln9$$

$$\Delta V_i = 4\,\eta V_T$$

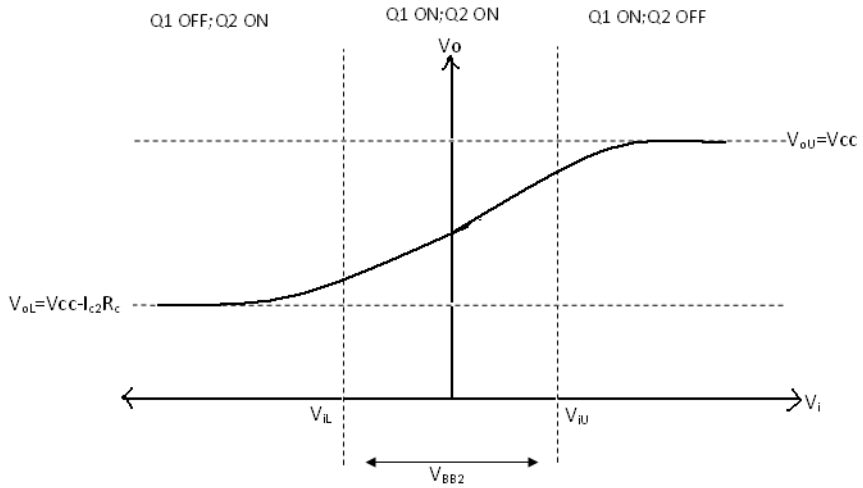


Fig.2.13 Transfer Characteristics of Emitter Coupled Clipper

2.3.2. Diode Clipper Applications:

There are numerous applications for diode clippers. They find wide application in television receiver for separating synchronizing signals from composite picture signals and also in television transmitters at the time of processing the picture signals. They are also employed for different wave generation such as trapezoidal, square or rectangular waves. Series clippers are employed as noise limiters in FM transmitters by clipping excessive noise peaks above a specified level.

The diode clipper can be used for the protection of different types of circuits. For example, a digital circuit against transients which may cause considerable damage. The arrangement is shown in the *Fig.2.14.*

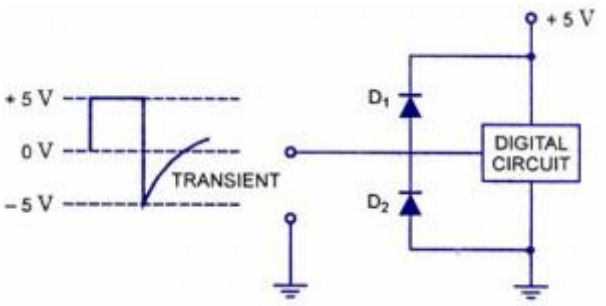


Fig.2.14 Diode Clipper – Applications

When a transient takes place on the input line, as shown in figure given below, diode D_2 gets forward biased and starts conducting. Thus transient is shorted to ground and the circuit is protected from damage due to transient.

2.4. VOLTAGE COMPARATORS:

The clipping circuit discussed above can be used as comparators..A comparator circuit is used to identify the inst\ant at which the arbitrary input wave form attains a particular reference level. This is done by comparing arbitrary inputs with the reference level hence called comparator. The difference between clipper and comparator is that in clipper the waveform other than the part which is clipped off is also important. But in comparator, only the instant at which the comparison is successful, is important while other wave form is not important to be reproduced at the output.

Consider simple comparator as shown in *Fig.2.15* Consider V_i as ramp input, increasing linearly from zero. The output will remain at V_R, till input is less than V_R+Vr, as the diode is not conducting.

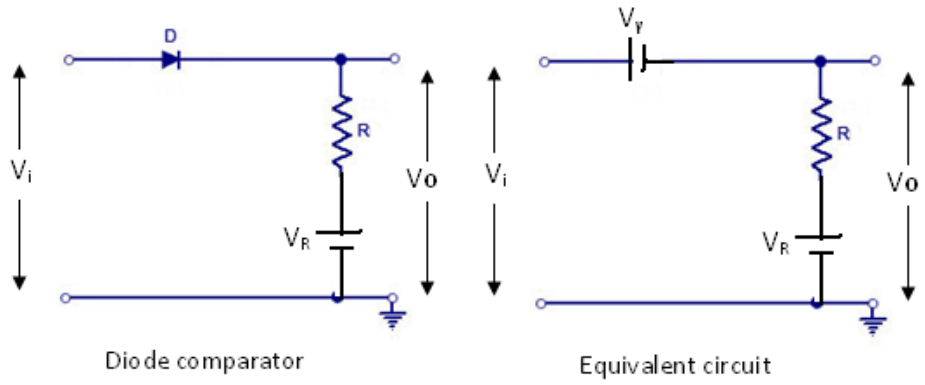


Fig.2.15 Diode Comparator and its Equivalent circuit.

At t=t1 V_i becomes equal to V_R+Vr, after which Vo increase along with the input signal Vi.

The comparator o/p is given to a particular device. This device will respond when the comparator voltage increases to some level of Vo above V_R.The i/p and o/p wave forms are shown in *Fig.2.16*.

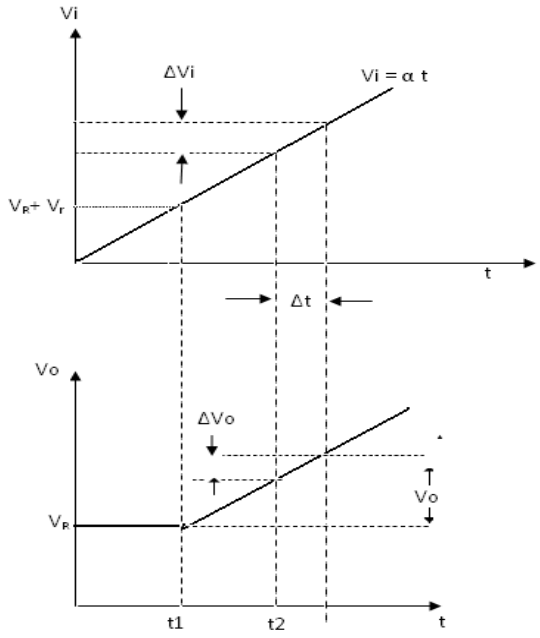


Fig.2.16 Input and Output Waveforms of Diode Clipper.

2.5. APPLICATIONS OF COMPARATOR:

2.5.1. Null detector:

A null detector is one that functions to identify when a given value is zero. Comparators can be a type of amplifier distinctively for null comparison measurements. It is the equivalent to a very high gain amplifier with well-balanced inputs and controlled output limits. The circuit compares the two input voltages, determining the larger. The inputs are an unknown voltage and a reference voltage, usually referred to as v_u and v_r. A reference voltage is generally on the non-inverting input (+), while v_u is usually on the inverting input (-). (A circuit diagram would display the inputs according to their sign with respect to the output when a particular input is greater than the other.) The output is either positive or negative, for example +/-12V. In this case, the idea is to detect when there is no difference between in the input voltages. This gives the identity of the unknown voltage since the reference voltage is known.

When using a comparator as a null detector, there are limits as to the accuracy of the zero value measurable. Zero output is given when the magnitude of the difference in the voltages multiplied by the gain of the amplifier is less than the voltage limits. For example, if the gain of the amplifier is 10^6, and the voltage limits are +/-6V, then no output will be given

if the difference in the voltages is less than 6μV. One could refer to this as a sort of uncertainty in the measurement.

2.5.2. Zero-crossing detector:

For this type of detector, a comparator detects each time an ac pulse changes polarity. The output of the comparator changes state each time the pulse changes its polarity, that is, the output is HI (high) for a positive pulse and LO (low) for a negative pulse. The comparator also amplifies and squares the input signal.

2.5.3. Relaxation oscillator:

A comparator can be used to build a relaxation oscillator. It uses both positive and negative feedback. The positive feedback is a Schmitt trigger configuration. Alone, the trigger is bi-stable multivibrator. However, the slow negative feedback added to the trigger by the RC circuit causes the circuit to oscillate automatically. That is, the addition of the RC circuit turns the hysteretic bi-stable multivibrator into an astable multivibrator.

2.5.4. Level shifter:

This circuit requires only a single comparator with an open-drain output as in the LM393, TLV3011 or MAX9028. The circuit provides great flexibility in choosing the voltages to be translated by using a suitable pull up voltage. It also allows the translation of bipolar ±5V logic to unipolar 3V logic by using a comparator like the MAX972.

2.5.5. Analog-to-digital converter:

When a comparator performs the function of telling if an input voltage is above or below a given threshold, it is essentially performing a 1-bit quantization. This function is used in nearly all analog to digital converters (such as flash, pipeline, successive approximation, delta-sigma modulation, folding, interpolating, dual-slope and others) in combination with other devices to achieve a multi-bit quantization.

2.6 DIODE CLAMPERS:

A clamping circuit is used to place either the positive or negative peak of a signal at a desired level. The dc component is simply added or subtracted to/from the input signal. The clamper is also referred to as a DC restorer and ac signal level shifter.

In some cases, like a TV receiver, when the signal passes through the capacitive coupling network, it loses its dc component. This is when the clamper circuit is used so as to re-establish the dc component into the signal input. Though the dc component that is lost in transmission is not the same as that introduced through a clamping circuit, the necessity to establish the extremity of the positive or negative signal excursion at some reference level is important.

A clamp circuit adds the positive or negative dc component to the input signal so as to push it either on the positive side, as illustrated in *Fig.2.17 (a)* or on the negative side, as illustrated in *Fig.2.17 (b).*

The circuit will be called a positive clamper, when the signal is pushed upward by the circuit. When the signal moves upward, as shown in *Fig.2.17. (a),* the negative peak of the signal coincides with the zero level.

The circuit will be called a negative clamper, when the signal is pushed downward by the circuit. When the signal is pushed on the negative side, as shown in *Fig.2.17. (b),* the positive peak of the input signal coincides with the zero level.

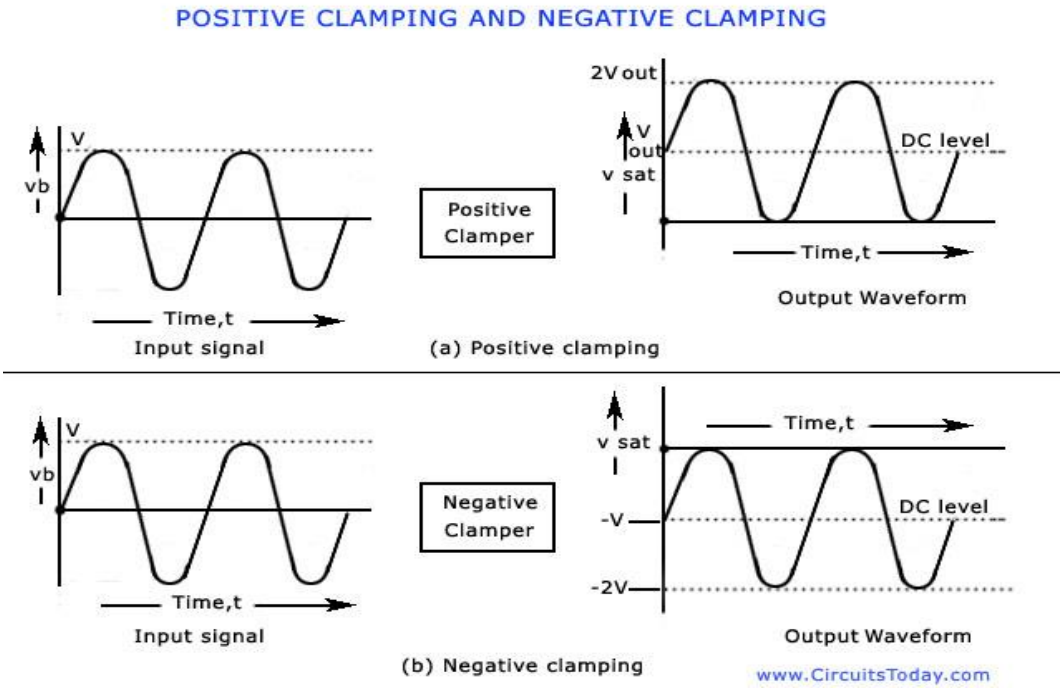


Fig.2.17 Input and Output Waveforms of Clampers.

For a clamping circuit at least three components — a diode, a capacitor and a resistor are required. Sometimes an independent dc supply is also required to cause an additional shift. The important points regarding clamping circuits are:

- The shape of the waveform will be the same, but its level is shifted either upward or downward,
- There will be no change in the peak-to-peak or rms value of the waveform due to the clamping circuit. Thus, the input waveform and output waveform will have the same peak-to-peak value that is, $2V_{max}$. This is shown in the figure above. It must also be noted that same readings will be obtained in the ac voltmeter for the input voltage and the clamped output voltage.
- There will be a change in the peak and average values of the waveform. In the figure shown above, the input waveform has a peak value of V_{max} and average value over a complete cycle is zero. The clamped output varies from 2 V_{max} and 0 (or 0 and -$2V_{max}$). Thus this peak value of the clamped output is $2V_{max}$ and average value is $V_{max.}$
- The values of the resistor R and capacitor C affect the waveform.
- The values for the resistor R and capacitor C should be determined from the time constant equation of the circuit, t = RC. The values must be large enough to make sure that the voltage across the capacitor C does not change significantly during the time interval the diode is non-conducting. In a good clamper circuit, the circuit time constant t = RC should be at least ten times the time period of the input signal voltage.

It is advantageous to first consider the condition under which the diode becomes forward biased.

Clamping circuits are often used in television receivers as dc restorers. The signal that is sent to the TV receiver may lose the dc components after being passed through capacitive coupled amplifiers. Thus the signal loses its black and white reference levels and the blanking level. Before passing these signals to the picture tube, these reference levels have to be restored. This is done by using clamper circuits. They also find applications in storage counters, analog frequency meter, capacitance meter, divider and stair-case waveform generator.

Consider a negative clamping circuit, a circuit that shifts the original signal in a vertical downward direction, as shown in the figure below. The diode D will be forward biased and the capacitor C is charged with the polarity shown, when an input signal is applied. During the positive half cycle of input, the output voltage will be equal to the barrier potential of the diode, V_0 and the capacitor is charged to $(V - V_Q)$. During the negative half cycle, the diode becomes reverse-biased and acts as an open-circuit. Thus, there will be no effect on the capacitor voltage. The resistance R, being of very high value, cannot discharge C a lot during the negative portion of the input waveform. Thus during negative input, the output voltage will be the sum of the input voltage and the capacitor voltage and is equal to – V – (V — V_0) or – (2 V – V_0). The value of the peak-to-peak output will be the difference of the negative and positive peak voltage levels is equal to V_0-[-(2V-V_0)] or 2 V.

The *Fig.2.18* shown below can me modified into a positive clamping circuit by reconnecting the diode with reversed polarity. The positive clamping circuit moves the original signal in a vertical upward direction. A positive clamping circuit is shown in the figure below. It contains a diode D and a capacitor C as are contained in a negative clamper. The only difference in the circuit is that the polarity of the diode is reversed. The remaining explanation regarding the working of the circuit is the same as it is explained for the negative clamper.

To remember which way the dc level of a signal moves, look at figure shown below. Notice that the diode arrows point downward, the same direction as the dc shift.

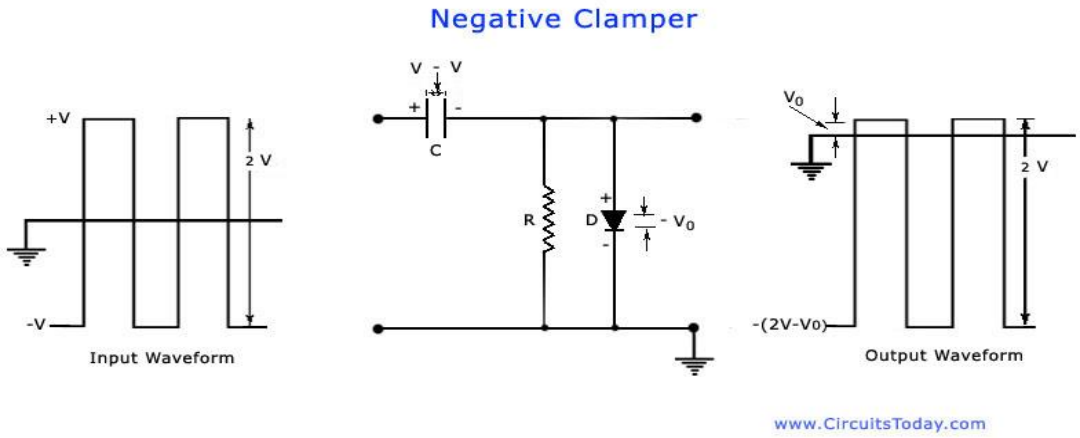


Fig 2.18 Negative Clamping Circuit.

Similarly in the *Fig2.19* shown below, the diode arrow points upward, again the same direction as the dc shifts. It means that, when the diode points upward. We have a positive dc clamper and when the diode points downward, the circuit is a negative dc clamper.

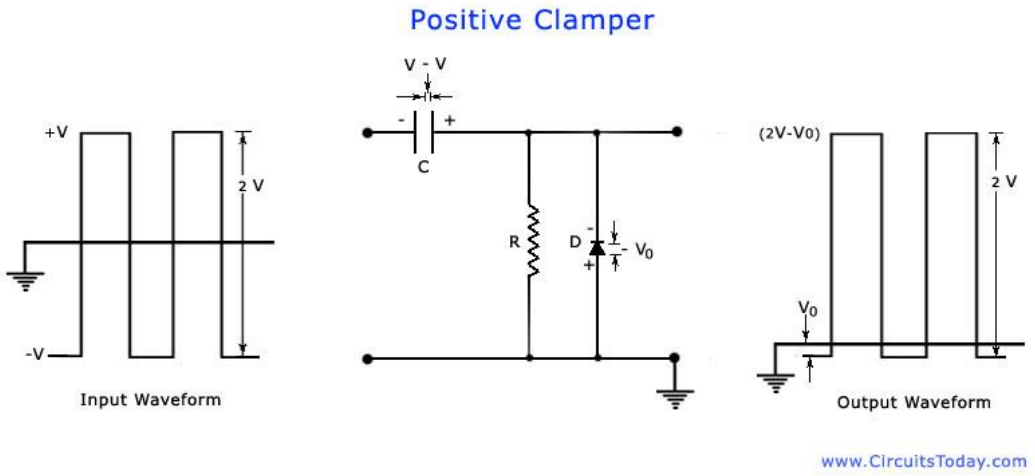
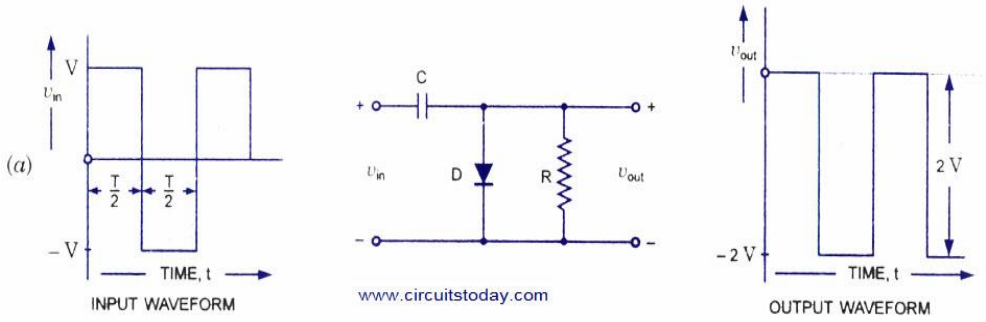
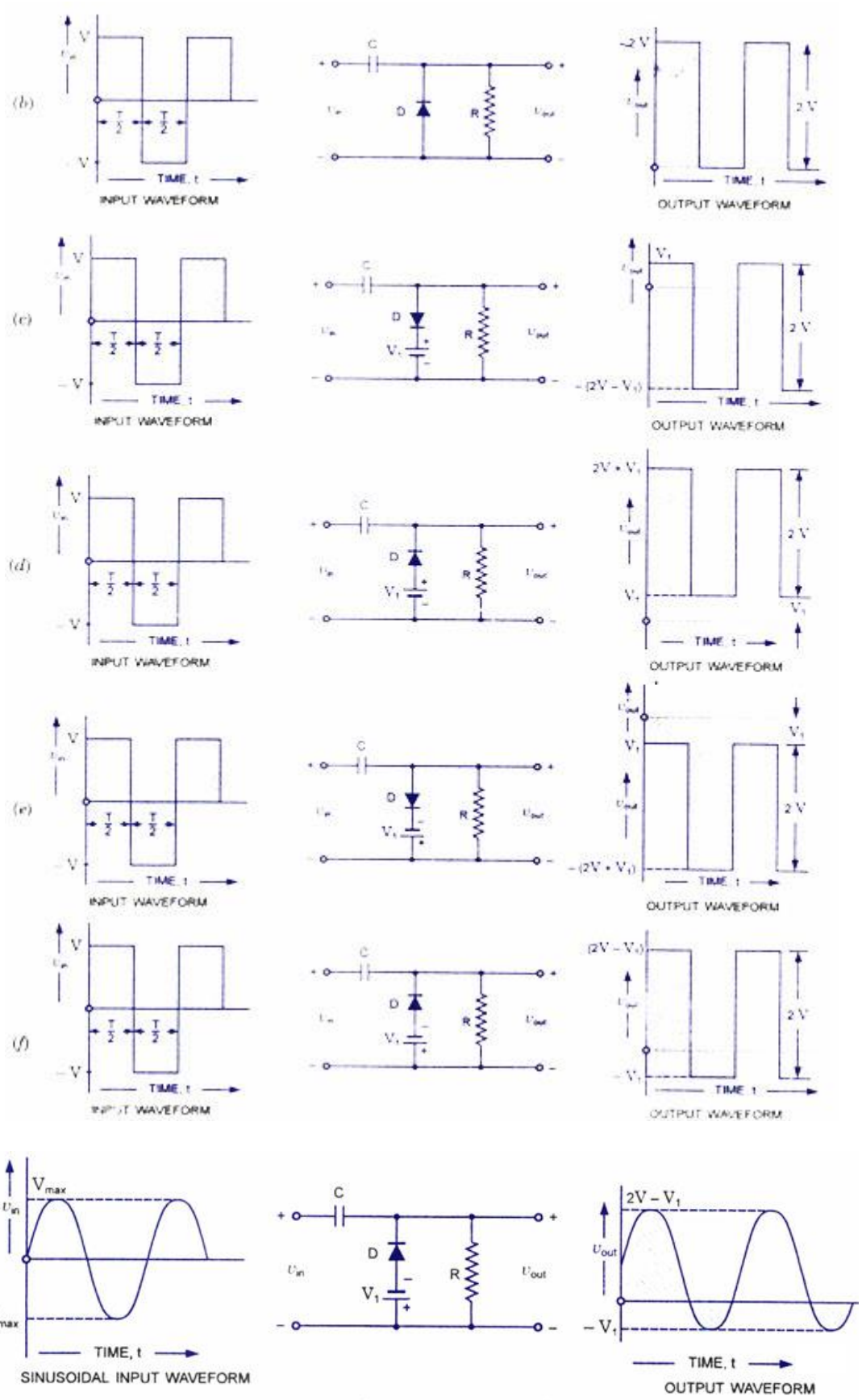


Fig.2.19 Positive Clamping Circuit.

A number of clamping circuits with their effect on the input signal are shown in the figure given below. All the figures shown below have the input and output signals in square waves, the same procedure can be used for sinusoidal inputs. In fact, one approach to the analysis of clamping networks with sinusoidal inputs is to replace the sinusoidal wave signal by a square wave of the same peak values. The resulting output will then form an envelope for the sinusoidal response, as illustrated in *Fig.2. 20(g)* for a network appearing in *Fig.2.20 (f).* The diodes have been assumed to be ideal and 5 RC » T/2 in drawing the output wave-forms.





Different Clamping Circuits

Fig.2.20 Different Clampers Circuits.

2.7 Clamping Circuit Theorem:

Under steady-state conditions, for any input waveform, the shape of the output waveform of a clamping circuit is fixed and also the area in the forward direction (when the diode conducts) and the area in the reverse direction (when the diode does not conduct) are related.

The clamping circuit theorem states that, for any input waveform under steady-state conditions, the ratio of the area Aj under the output voltage curve in the forward direction to that in the reverse direction Ar is equal to the ratio Rf/R.

This theorem applies quite generally independent of the input waveform and the magnitude of the source resistance. The proof is as follows:

In the interval $0 < t < T\backslash$, the input is at its upper level, the diode is ON. If $v_f(t)$ is the output waveform in the forward direction, then the capacitor charging current is

$$i_f(t) = \frac{v_f(t)}{R_f}$$

Therefore, the charge gained by the capacitor during the forward interval is

$$Q_c = \int_0^{T_i =} i_f(t)\,dt = \frac{1}{R_f}\int_0^{T_1} v_f(t)\,dt = \frac{A_f}{R_f}$$

In the interval $T_x < t < 7, + T_2$, the input is at its lower level, the diode is OFF, If $v_r(i)$ is the output voltage in the reverse direction, then the current which discharges the capacitor is

$$i_f(t) = \frac{v_f(t)}{R_f}$$

Therefore, the charge lost by the capacitor during the reverse interval is

$$Q_c = \int_0^{T_i+T_2} i_f(t)\,dt = \frac{1}{R_f}\int_0^{T_i+T_2} v_f(t)\,dt = \frac{A_f}{R_f}$$

Under steady-state conditions, the net charge acquired by the capacitor over one cycle must be equal to zero. Therefore, the charge gained in the interval C < *t* < *Tu* will be equal to the charge lost in the interval $T_1 < t < T_1 + T_2$, i.e. $Qg = Q_1$.

$$\frac{A_f}{R_f} = \frac{A_f}{R} \quad \text{i.e,} \quad \frac{A_f}{A_r} = \frac{R_f}{R}$$

2.8 Practical Clamping Circuits:

Perfect flatness of the positive and negative peaks of a square wave can be obtained only if the capacitor C is arbitrarily large. Practically, in clamping circuits the capacitor C is such that $(R_f + R_S)C \ll T_u$ and $(R + R_S)C \gg T_2$. So, a square wave after clamping appears as shown in Figure 21. This is because during the interval T_2, when $(R + R_S)C \gg T_2$, the capacitor discharges very slowly and hence there will be a small tilt in the output. In the interval T_h when $(R_f + R_S)C \ll T_h$ the capacitor recharges very fast and hence there will be a small spike of magnitude *Ap* at the beginning, and for the remaining interval the output will be zero. The overshoot A_f is usually smaller than the tilt A_f.

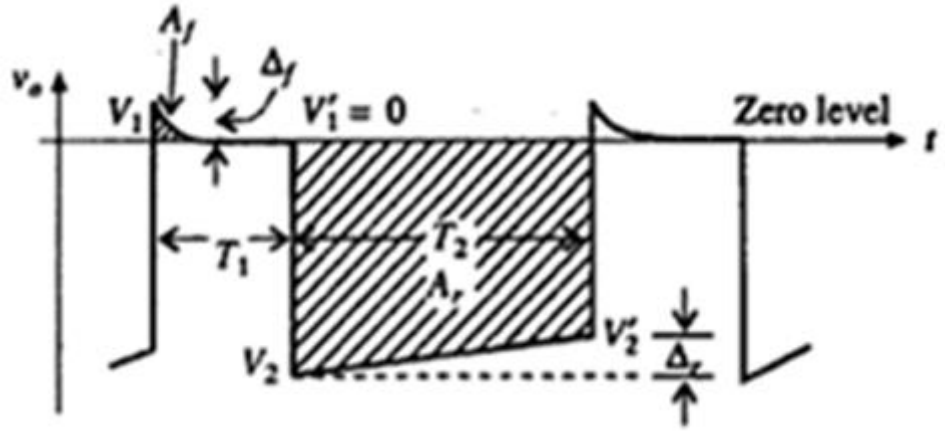


Fig.2.21 The output of a practical clamping circuit for a square wave input.

For the case shown in *Fig.2.21*, the voltage values are

$$V_1' = 0, \quad V_2 = -V\frac{R}{R+R_s}$$

where *V* is the amplitude of discontinuity in input.

$$V_2^{'} = V_2 e^{-T_2/(R+R_S)C}, \quad \Delta_f = V_2^{'} - V_2$$

$$\Delta_f = V_1 - V_1^{'} = V_1 = \frac{R_f}{R_f + R_S} \cdot \frac{R}{R + R_S} \Delta_f$$

Even if we assume that the capacitor C is arbitrarily large, unless the source resistance ***Rs*** is zero, the part of the input signal which occurs when the diode is conducting appears at the output multiplied by ***R/(Rf + Rs) ,*** and the signal which occurs when the diode is not conducting, appears at the output multiplied by ***R/(R + Rs) .*** Usually ***R/(R + Rs)*** is much closer to unity than ***Rf(Rf + Rs).*** Such selective attenuation flattens that part of the signal, which drives the diode into conduction. This distortion is more easily observed in the case of a signal with a sharp peak such as a ramp. It is not apparent in the case of a square wave because it has flat top and flat bottom. Quite independent of the distortion, the clamping circuit theorem ***Af/Ar = Rf/R*** is valid. See *Fig.2.22*.

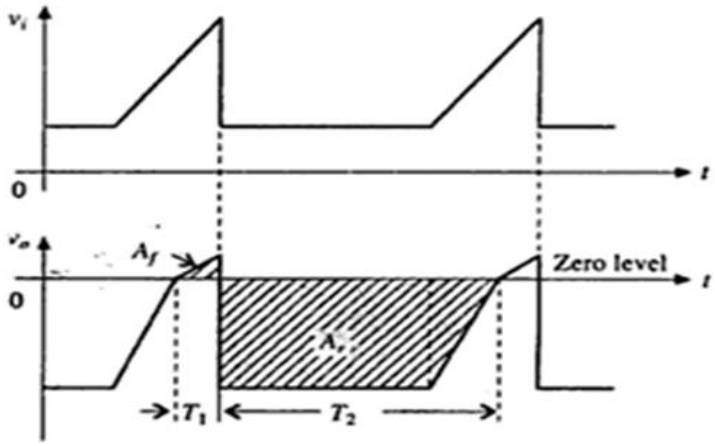


Fig.2.22 Clamping of a ramp signal: (a) input waveform and (b) output waveform.

In the case of biased clamping, i.e. when a reference voltage source V_R is connected in series with the diode to clamp the signal positively or negatively with reference to V_R, for perfect circuit operation, the positive excursion of the signal with reference to its average value must be larger than V_R. If the diode breakdown voltage *Vy* is not negligible, the clamping circuit theorem for biased clamping is

$$\frac{A_f - (V_R + V_\gamma)T_1}{A_r} = \frac{R_f}{R}$$

where *Tx* is the interval over which the diode is forward biased and *R » Rf.*

2.8.1. Effect of Vγ of Diode On Clamping Circuit:

Until now it is assumed that the cut-in voltage of the diode is assumed as 0V. But for Si diode it is 0.6 V and for Ge diode it is 0.2V. Consider the biased clamper as shown in *Fig.2.23.*

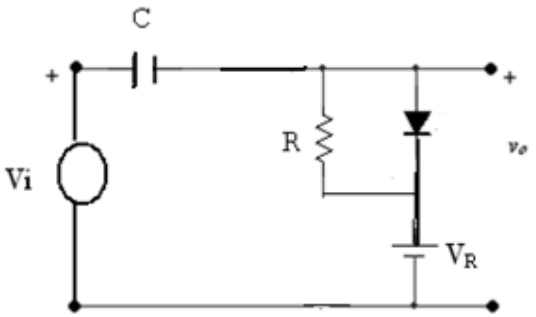


Fig.2.23 Clamping Circuit with resistor connected across diode.

The positive extremity of the voltage Vo is clamped to V_R in this circuit. The clamping circuit theorem is applicable provided areas AF and AR are measured with respect to the level V_R than with respect to ground.

Some time the circuit is modified as shown in the *Fig.2.24*. The resistor R is connected across both diode and the biasing reference voltage V_R.

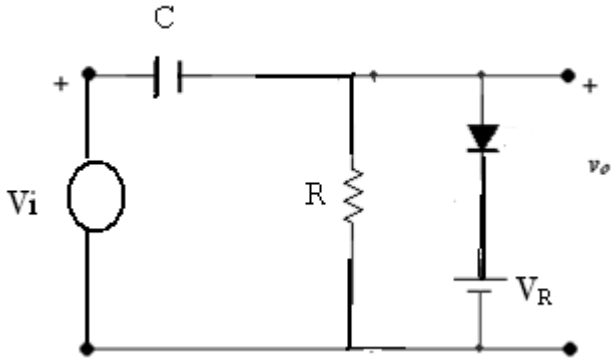


Fig.2.24 resistor R is connected across both diode and the biasing reference voltage V_R.

In such a modified circuit, for proper functioning it is necessary that the positive excursion of the signal with reference to its average value must be larger than V_R.Now due to V_γ, the reference level becomes $V_{R+\gamma}$. The clamping theorem for such a circuit can be written as,

$$\frac{A_F-(V_R+V_\gamma)T_1}{A_R}=\frac{R_f}{R}$$

2.9 Effect of Diode Characteristics on Clamping Circuit:

Until now either ideal diode approximation is used or the diode is used or the diode is replaced by the battery of cut-in voltage V_γ and forward resistances R_f. Let us now consider the effect of diode volt-ampere (V-I) characteristics on the clamping voltage.

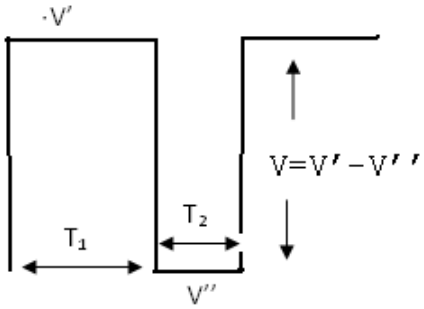
The diode characteristics is given by,

$$I = I_o e^{V/\eta V_T}$$

The above equation is valid for $e^{V/\eta V_T} \gg 1$. Let us assume R_S=0 for the clamper in this analysis.

The *Fig.2.25* shows the clamper under consideration. The input applied is a square wave having amplitude V which is V'=V''. The input is at V' for period T1 and is at V'' for period T2.

When the input is at V' i.e., positive maximum then diode conduct and clamp the output at some clamping voltage V_{cl}.



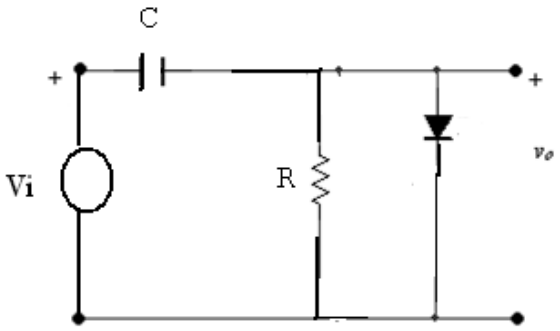


Fig2.25 clamping circuit.

$$I_{cl} = I_o e^{V_{cl}/\eta V_T} = Diode\ current\ when\ Vi = V'$$

This current charges the capacitor C to the voltage Vc.

$$V_C = V' - V_{cl}$$

When input decreases to V'', then diode is non conducting and voltage across R is,

$$V_C - V'' = V - V_{cl}$$

Now V_{cl} is << V. Hence V-V_{cl}≈V. The discharge current of the capacitor is is V/R.

For symmetrical square wave, the charging current must be equal to discharging current.

$$\therefore I_{cl} = I_o e^{V_{cl}/\eta V_T} = \frac{V}{R}$$

$$\therefore V_{cl} = \eta V_T ln\left[\frac{V}{RI_o}\right]$$

Differentiating both sides

$$\therefore dV_{cl} = \eta V_T \frac{dV}{V}$$

The above equation gives the variation of clamping voltage with the amplitude of the input signal. As V increases, the dependence of V_{cl} on V reduces. This is because the diode clamps higher on its V-I characteristics.

2.10. Synchronized Clamping:

The dc restorers discussed above are examples of clamping circuits in which the time during which the clamping is effective is controlled by the signal itself. Useful features result when the time of clamping is not determined directly by the signal but is determined

rather by an auxiliary voltage, called a control signal, which occurs synchronously with the signal. For example, suppose the waveform of *Fig.2.26.(a)* is to be used to displace the beam of a cathode-ray tube linearly with time, first in one direction and then in the other direction from some fixed initial point. If the signal is transmitted through an ac coupling network whose low-frequency time constant is not very large in comparison with the interval Ti, the signal will distort into the form shown in *Fig.2.26.(b).* The principal defect in the waveform is that the two displacements will start from different places (A and B). In addition, the dc level VR has been lost. If, however, the signal is passed through the circuit of *Fig.2.27.* And if switch S is closed during time T_2 and is open during time T, the waveform will appear as in *Fig.2.26. (c).* The pips which appear when the voltage returns to the level V_R will be reduced to infinitesimally narrow spikes as the resistance of the switch (which is assumed to be R f) approaches zero.

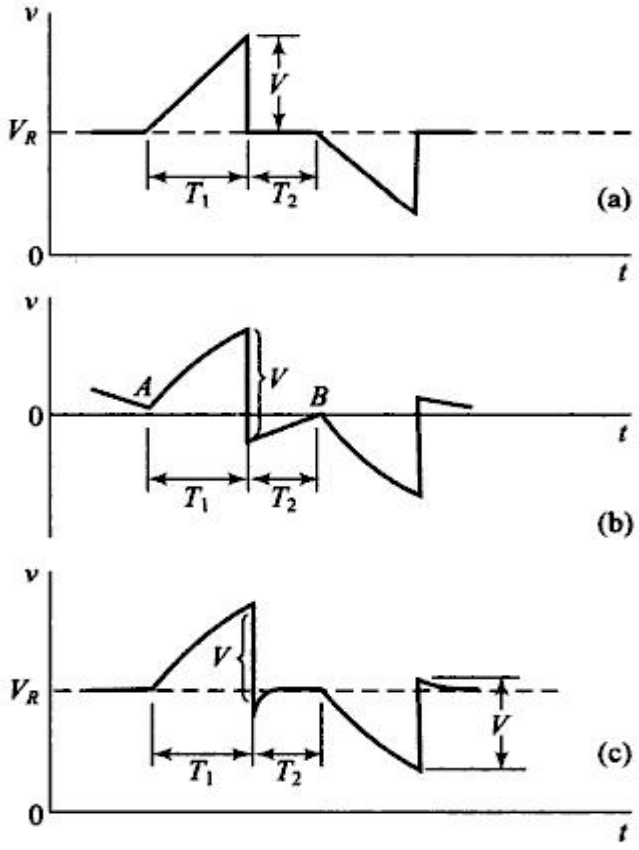


Fig.2.26.Illustrating the necessity for synchronized clamping for a signal which may vary in both directions from a voltage, which is to be established at same reverence level.

It is, of course, required that the switch S be open throughout the time interval T_1, but it is not necessary that the switch be closed for the entire interval T_2. It is only required that the switch be closed for a period long enough to allow the capacitor C to acquire or lose enough charge to bring the output terminal to the reference level V_R.

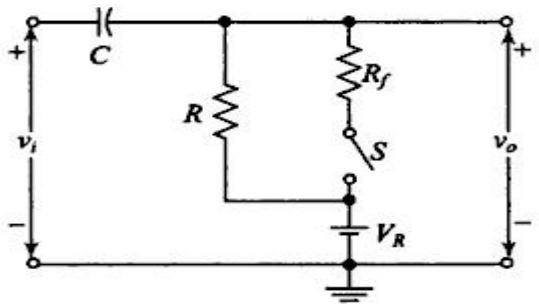


Fig.2.27.Switch S closes in synchronism with the signal during those intervals when it is desired that the output be clamped to V_R.

It is not possible to use synchronized clamping with a signal of arbitrary waveform. For example, the waveform were sinusoidal, it would necessarily be distorted every time the switch S is closed. Synchronous clamping may be used whenever the signal has periodically occurring intervals during which the input waveform is quiescent. Where synchronized clamping is feasible, it may be used to provide dc restoration even when the positive and negative excursions of the signal fluctuate from cycle to cycle.

A synchronous clamping circuit is shown in *Fig.2.28.* The signal is transmitted from input to output through the capacitor Cs. The two-diode circuit which is bridged between signal lead and ground serves the function of the switch S in *Fig.2.27*. Two control-signal pulse trains $V_l(t)$ and $V_2(t)$ are required. These waveforms are identical in all respects expect that one is the inverse of the other. The dc levels of the wave forms are of no consequences.

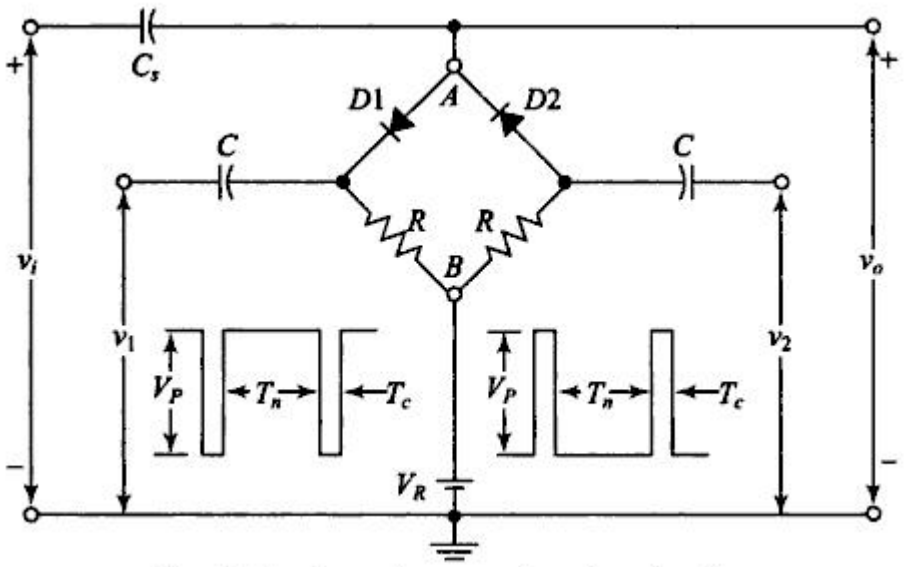


Fig2.28.A Synchronous Clamping Circuit.

This circuit may be analyzed in much the same manner as the dc-restorer circuit, for the two circuits have many features in common. Such an analysis reveals that, in the steady state, during the interval T_c the diodes are brought to conduction and that the voltage at the point A is the same as at point B. As in the dc restorer, the diodes conduct briefly to supply to the capacitors C the charge lost through the resistors R during the non-conducting interval T_n. During T_n both diodes are reverse-biased, and the output signal lead is entirely free to follow the input signal. Suppose that at the end of an interval T_n the voltage at A is not equal to V_R. Then when the diodes are brought to the point of conduction, if it should happen that $V_A > V_R$, diode D_1 will conduct, discharging capacitor C_s into capacitor C until $V_A = V_R$. If $V_A < V_R$, diode D_2 will conduct until $V_A = V_R$.

For proper operation of the circuit it is required that $C >> C_s$ and that $RC >> T$. There is, however, an upper limit on R which results from the fact that during the interval T_n, the capacitor must be able to discharge through R the charge it may have acquired from C, during the interval T_c When C_s discharges, it does so through a diode forward resistance R_f and through the output impedance R. of one of the generators that furnish the control signal. Hence it is also required that $C_S+(R_f+ R_s) << Tc$. The required minimum amplitude Vp of the clamping pulse is determined by the condition that neither diode is brought into conduction during the interval T_n, by the signal. This

condition leads to the restriction that $V_p > V_S$, where V_S is the peak signal excursion above or below the average value of the signal. Finally, we may note that if the clamping-pulse amplitudes are not equal or if the resistors R are not equal, the circuit will not clamp to V_R but to a somewhat different voltage.

UNIT-3

SWITCHING CHARACTERISTICS OF DEVICES

3.1 Switching Characteristics of a Diode:

Our main concern is to study the *switching behavior* of diodes and transistors. Diode is treated as a simple *self-activated* electronic switch. In switching. Applications, diode represents either a short-circuit or an open-circuit. In order to gain a good understanding of switching in a diode, it is necessary to begin our study with its charge control model.

3.2 Diode as a switch:

The *charge-control model* of a diode explains the operation of a *p-n* junction employing minority charge concentrations. This approach is very helpful in understanding the switching behavior of diodes and transistors. In switching applications, a semiconductor diode is used to represent a switch in CLOSED position and in an OPEN position respectively. The forward-bias and reverse-bias conditions of a diode are used for this purpose. The diode is said to be either in ON state or in OFF state in such applications. The

steady-state minority carrier concentrations at the *p-n* junction and across the bulk of the semiconductor diode depend on the biasing conditions. These concentrations, when the diode is unbiased, forward-biased, and reverse-biased are shown in *Fig. 3.1*. It should be remembered those holes are the minority carriers in n-type material, and electrons are the minority carriers in a p-type material. These minority carrier concentrations across the *p-n* junction place limitations on the maximum switching speed of the diode.

It is important to know how the minority carrier concentration around the *p-n* junction changes in a diode under different biasing conditions. This understanding is necessary to study the switching operation of a diode. The electron concentration at the junction in p-type semiconductor is $n_p(0)$. The hole concentration at the junction in n-type semiconductor is $p_n(0)$. The electron concentration at a distance *x* from the junction in p-type semiconductor is $n_p(x)$. The hole concentration at a distance *x* from the junction in n-type semiconductor is $p_n(x)$, the electron concentration in p-type semiconductor under thermal equilibrium is n_{po}. The hole concentration in n-type semi- conductor under thermal equilibrium is p_{no}. In the case of an unbiased semiconductor diode, the bias voltage V = O. Then the minority carrier concentrations at the junction $n_p(0)$ and $P_n(0)$ would be at their thermal equilibrium values. In other words $n_p(0) = n_{po}$ and $P_n(0) = p_{no}$. This is shown in Fig. (a). When the diode is forward-biased V = 0.7 V. The *law of junction* is expressed in terms of Eqs. (1) and (2).

$$n_p(0) = n_{p0}\, e^{V/V_T} \qquad (1)$$

$$p_n(0) = p_{n0}\, e^{V/V_T} \qquad (2)$$

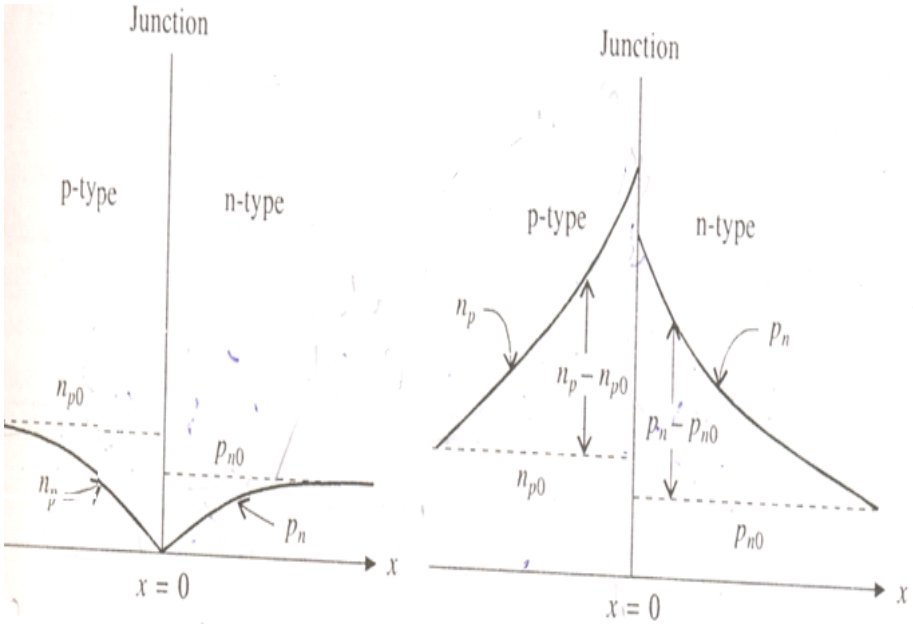


Fig. 3.1 minority carrier distribution when diode is a) forward biased b) reverse biased

These expressions are useful to find the minority charge concentrations at the *p-n* junction. We can see, by applying the law of the junction, that the minority charge concentrations at the junction rise to high levels during forward bias. These minority charge concentrations are indicated in *Fig. 3.1(b*). Similarly these concentrations drop almost to zero level when the reverse bias voltage -v appears across the diode junction. These concentrations are indicated in *Fig. 3.1(a).* Moreover the concentrations $n_p(x)$ and $p_n(x)$ exponentially vary as we move into regions away from the junction. These concentrations vary exponentially with distance *x* from the junction. They reach their thermal equilibrium values when *x* is large compared to the diffusion length. The shaded areas in these curves constitute the stored minority charge across the bulk of the diode. These results can be easily verified by substituting the values of V_T and the bias voltage V in Eqs. (1) and (2). It is known that the value of V_T is 26 mV at room temperature.

3.3. Piece-wise linear diode characteristics:

The piece-wise linear approximation for a semiconductor diode characteristic is shown in *Fig. 3.2.* The breakdown is at $V_{Y'}$ which is called the *offset* or *threshold* voltage. The diode behaves like an open-circuit if $v < V_y$. The characteristic shows a constant incremental resistance $r = dv/dt$ if $v > V_y$. Here *r* is called the forward resistance. The static resistance **R** =V/ I is not constant and is not useful.

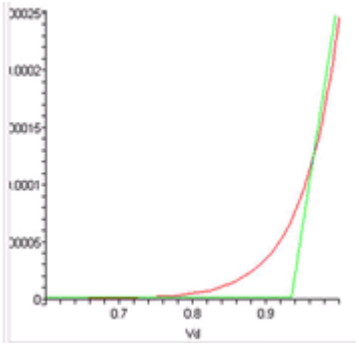


Fig. 3.2. A piesewise linear approximation of the diode characteristics

The numerical values Vy and R_j to be used depend upon the type of diode and the contemplated voltage and current swings. Typically:

For current swings from 'cut-off to 10 mA

For Ge, Vy = 0.2 V and R_j = 20 **Ω**

For Si, Vy = 0.6 V and R_j = 15 **Ω**

For current swings up to 50 mA

For Ge, Vγ = 0.3 V and R_f = 6 **Ω**

For Si, Vγ= 0.65 V and R_j = 5.5 **Ω**

For avalanche diodes, Vγ= V_z, and R_f is the dynamic resistance in the breakdown region.

3.4. Switching Times in a Diode:

The accumulation of charge in forward bias and depletion of charge in reverse bias do not allow the semiconductor diode to make abrupt ON-to -OFF and OFF-to-ON transitions. As these transitions involve transients, the diode cannot respond immediately to sudden changes occurring in the externally applied voltage.

3.4.1. Forward Recovery Time:

A finite time interval is required to recover the steady-state conditions of the diode. This is applicable when the diode is switching from forward bias to reverse bias and vice versa. The forward recovery time denoted by t_f of a semiconductor diode is negligible. 'Forward recovery time does not pose any limitation on switching speed of the diode in practice.

3.4.2. Reverse Recovery Time:

The reverse recovery time denoted by t_{rr} limits the switching speed of the diode. The reverse recovery time is specified in terms of typical operating conditions. Its value ranges from a fraction of a nanosecond to a microsecond.

Consider the circuit shown in *Fig. 3.3 (a)* containing a diode with a load resistance R_L. Let us assume that this diode is initially ON, that is, in the steady-state forward bias condition. The input signal that is applied to this circuit is shown in *Fig. 3.3 (b).*

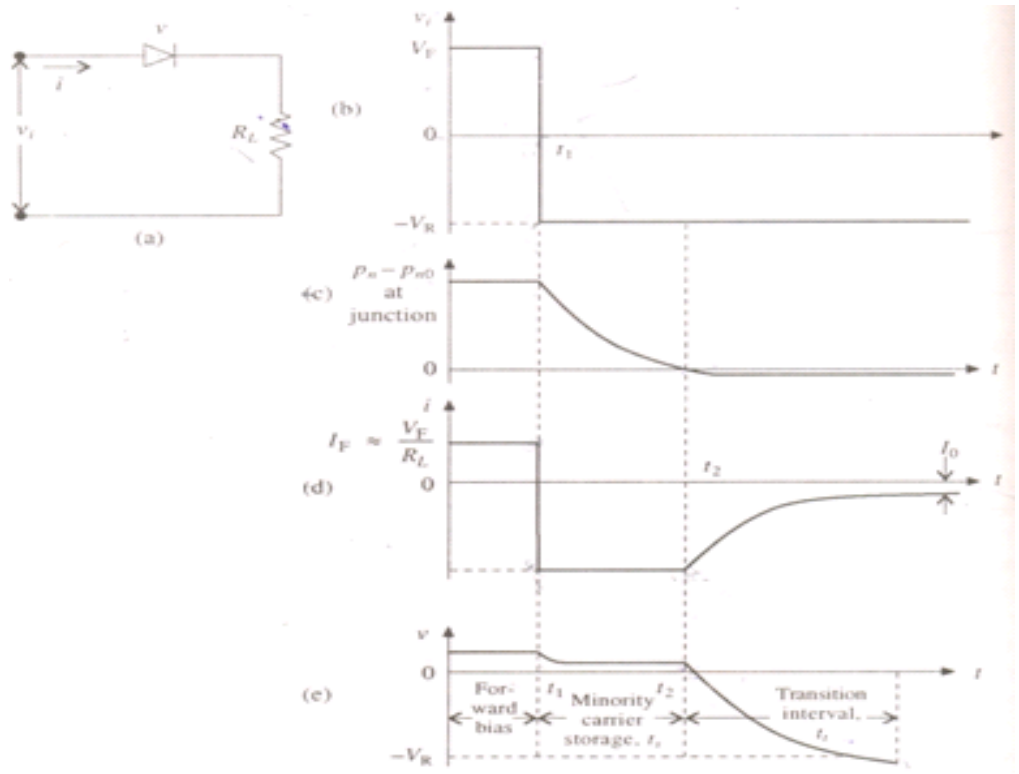


Fig. 3.3 (a)Applied voltage to the circuit (b) excess minority carriers (c) Charge carriers(d) diode current (e) diode voltage

The input voltage V_F almost appears across the load resistance R_L- Then the diode current $I \approx I_F = V_F/R_L$. To take the diode into OFF state, this input voltage to the circuit Vi is abruptly reversed from V_F to $-V_R$. At the time of this reversal in the diode state, current does not become zero. Instead, the diode current reverses and remains at $I_R = V_R/R_L$ for a duration t_s known as the storage time. This is due to the presence of the stored minority Charge carriers at the p-n junction indicated in *Fig. 3.3 (c).* These stored minority charge carriers allow the diode current to flow even after the external bias voltage is reversed from V_F to $-V_R$. The storage time is the time interval needed for the stored minority charge

concentrations to reach their thermal equilibrium values as required in steady-state reverse-bias conditions. After the lapse of the storage time, the stored minority charge at the p-n junction diminishes. Later the diode voltage and the diode current reverse their polarities. They exponentially reach their steady-state values $-V_R$ and I_0 respectively within a duration t_t known as the ***transition time***. The reverse recovery time t_{rr} is the sum of the storage time and the transition time. The variation of the input volt age during reverse recovery is shown along with the diode current in *Fig. 3.3(d).* In Fig. 3.3(e) we can see the variation of stored minority charge concentration and diode voltage.

3.5 Breakdown in p-n Junction diodes:

When the p-n junction diode is reverse biased, reverse saturation current Io flows due to minority carriers. There is a gradual increase in reverse current with increasing bias. When the reverse bias voltage approaches the breakdown voltage V_{BO}, there is a sudden increase in reverse current due to breakdown. Once breakdown occurs the diode no longer blocks current, and the diode current can now be controlled only by the resistance of the external circuit. .

3.5.1. Avalanche breakdown

Thermally generated minority carriers cross the depletion region and acquire sufficient kinetic energy from the applied potential to produce new carriers by removing valance electrons from other bonds. These new carriers will in turn collide with other atoms and thus increase the number of electrons and holes available for conduction. Because of the cumulative increase in carrier density after each collision, the process is known as *avalanche breakdown.*

3.5.2. Zener breakdown

Even if the initially available carriers do not gain enough energy to disrupt bonds, it is possible to initiate breakdown through a direct rupture of the bonds because of the existence of a strong electric field. Under these circumstances the breakdown is referred to as *zener breakdown.*

Zener breakdown occurs at voltages below 6 V. The operating voltages in avalanche breakdown are from several volts to several hundred volts with power rating up to 50 W.

True zener diode action displays a negative temperature coefficient, i.e. the breakdown voltage decreases with increase in temperature. True avalanche diode action exhibits a positive temperature coefficient,' i.e. the breakdown voltage increases with increase in temperature. The breakdown voltage for a particular diode can be controlled during manufacture by altering the doping levels in the junction. The breakdown voltage for silicon diodes can be made to occur at a voltage as low as 5 V with 10^{17} impurity atoms/crn^3 or as high as 1000 V when doped to a level of only 10^4 impurity atoms/cm.

3.6 Transistor as a Switch:

A transistor can be used as a switch. It has three regions of operation. When both emitter- base and collector-base junctions are reverse biased, the transistor operates in the cut-off region and it acts as an open switch. When the emitter base junction is forward biased and the collector base junction is reverse biased, it operates in the active region and acts as an amplifier. When both the emitter-base and collector-base junctions are forward biased, it operates in the saturation region and acts as a closed switch. When the transistor is switched from cut-off to saturation and from saturation to cut-off with negligible active region, the transistor is operated as a switch. When the transistor is in saturation junction, voltages are very small but the operating currents are large. When the transistor is in cut-off, the currents are zero (except small leakage current) but the junction voltages are large.

In the *Fig 3.4(a)* transistor Q can be used to connect and disconnect the load R_L from the source *Vcc.* When Q is saturated it is like a closed switch from collector to emitter and when Q is cut-off it is like an open switch from collector to emitter.

$$I_C = \frac{V_{CC} - V_{CE}}{R_L} \quad \text{and} \quad I_B = \frac{V_{BB} - V_{BE}}{R_B}$$

Referring to the output characteristics shown in *Fig 3.4(b)*, the region below the $I_B = 0$ curve is the cut-off region. The intersection of the load line with $I_B = 0$ curve is the *cut-off point.* At this point, the base current is zero and the collector current is negligible. The emitter diode comes out of forward bias and the normal transistor action is lost, i.e. Vce (cut-off) = Vcc- The transistor appears like an open switch.

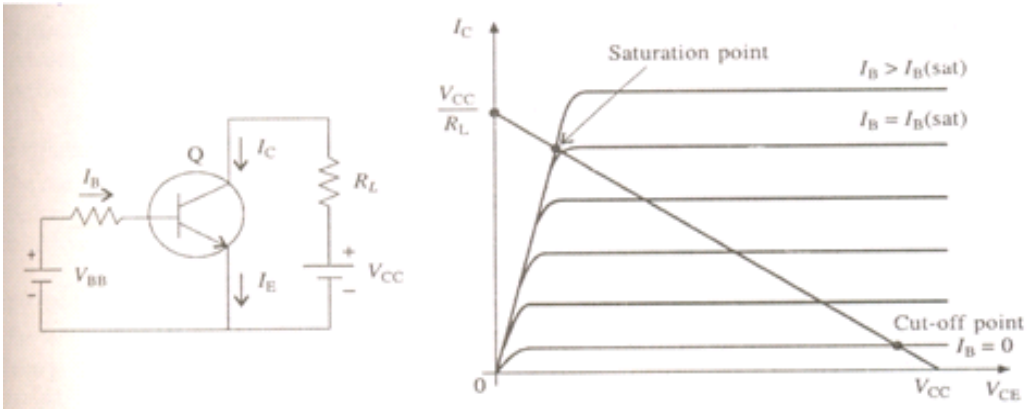


Fig. 3.4 (a) Transistor used as a switch (b) Output Characteristics with load line (dc)

The intersection of the load line with the $I_B = I_B(sat)$ curve is called the *saturation point.* At this point the base current is $I_B(sat)$ and the collector current is maximum. At saturation the collector diode comes out of cut-off and again the normal transistor action is lost, i.e. Ic(sat) = Vcc / R_L. I_B(sat) represents the minimum base current required to bring the transistor into saturation. For $0 < I_B < I_B$(sat), the transistor operates in the active region. If the base current is greater than IB(sat), the collector current approximately equals Vcc / R_L and the transistor appears like a closed switch.

3.6.1 Transistor Switching Times:

When the transistor acts as a switch, it is either in cut-off or in saturation. To consider the behavior of the transistor as it makes transition from one state to the other, consider the circuit shown in *Fig. 3.5 (a)* driven by the pulse waveform shown in *Fig. 3.5(b).* The pulse waveform makes transitions between the voltage levels V_2 and V1. At V_2 the transistor is at cut-off and at V_1 the transistor is in saturation. The input waveform *Vi* is applied between the base and the emitter through a resistor R_B.

The response of the collector current *ic* to the input waveform, together with its time relationship to that waveform is shown in Fig. 3.5(c). The collector current does not immediately respond to the input signal. Instead there is a delay, and the time that elapses during this delay, together with the time required for the current to rise to 10% of its maximum (saturation) value ($Ics = Vcc / R_L$) is called the delay time t_d. The current waveform has a nonzero rise time t_r, which is the rise time required for the current to rise from 10% to 90% of *Ics* . The total turn-on time t_{ON} is the sum of the *delay time* and the rise time, i.e. $t_{ON} = t_d + t_r$ .When the input signal returns to its initial state, the collector current

again fails to respond immediately. The interval which elapses between the transition of the input waveform and the time when *Ic* has dropped to 90% of Ics is called the *storage time* T_S. The storage interval is followed by the fall time t_f which is the time required for *Ic* to fall from 90 to 10% per cent of Ics. The turn-off time t_{OFF} is defined as the sum of the storage and fall times, i.e. $t_{OFF} = ts + t_f$.

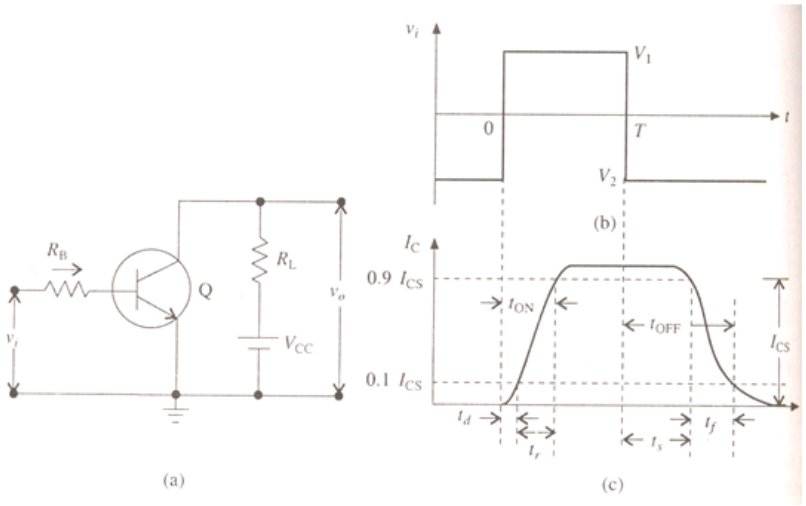


Fig. 3.5 (a) Transistor used as a switch (b) Pulse input (c) Rise time and fall times

3.6.2 The delay time:

There are three factors that contribute to the delay time. First there is a delay which results from the fact that, when the driving signal is applied to the transistor input, a nonzero time is required to charge up the junction capacitance so that the transistor may be brought from cut-off to the active region. Second, even when the transistor has been brought to the point where minority carriers have begun to cross the emitter junction into the base, a nonzero time is required before these carriers can cross the base region to the collector junction and be recorded as collector current. Finally, a nonzero time is required before the collector current can rise to 10% of maximum value.

3.6.3 Rise time and fall time:

The rise time and fall time are due to the fact that, if a base current step is used to saturate the transistor or to return it from saturation into cut-off, the collector current must traverse the active region. The collector current increases or decreases along an exponential curve.

3.6.4 Storage time:

The failure of the transistor to respond to the trailing edge of the driving pulse for the time interval *ts,* results from the fact that a transistor in saturation has a saturation charge of excess minority carriers stored in the base. The transistor cannot respond until the saturation excess charge has been removed.

3.7 Breakdown voltages of a transistor:

In a transistor switch, the voltage change which occurs at the collector with switching is nominally equal to the collector .supply voltage *Vee.* Since this voltage' will be used to operate other circuits and devices, then for the sake of reliability of operation, Vcc should be made as large as possible. The maximum allowable voltage depends not only on the characteristics of the transistor but also on the associated transistor base circuitry.

The maximum reverse biasing voltage which may be applied before breakdown between the collector and base terminals of the transistor, under the condition that the emitter lead be open-circuited is represented by the symbol BV_{CBO}. This breakdown voltage is a characteristic of the transistor alone. Breakdown occurs because of the avalanche multiplication of the current *lea* that crosses the collector junction. As a result of-this multiplication the current becomes *MIco,* in which *M* is the factor by which the original current I_{CO} is multiplied by the avalanche effect. At a high enough voltage, namely BV_{CBO}, the multiplication factor *M* becomes nominally infinite and the region of breakdown is then attained. Here the current rises abruptly and large changes in current accompany small changes in applied voltage.

The avalanche multiplication factor *M* depends on the voltage V_{CB} between the collector and the base, i.e.

$$M = \frac{1}{1 - \left(\frac{V_{CB}}{BV_{CBO}}\right)^n}$$

The parameter *n* lies in the range 2 to 10 and controls the sharpness of the onset of breakdown. When *n* is large, *M* continues at nearly unity until V_{CB} approaches very close to BV_{CBO} at which the point *M* soars upwards abruptly. When *n* is small, the onset of breakdown is gradual.

$$V_{CB} = BV_{CBO}\sqrt[n]{\frac{1}{h_{FE}}}$$

In *Fig.3.6 (a)* the CB characteristics have been extended into the breakdown region. The curve for I_E=0 is a plot, as a function of V_{CB} of the product of the reverse collector current *Ico* and the avalanche multiplication factor *M*. The abrupt growth in *Ic* as BV_{CBO} is approached, is shown along with the slower increase in *Ic* over the active region that results from the small but not negligible avalanche multiplication.

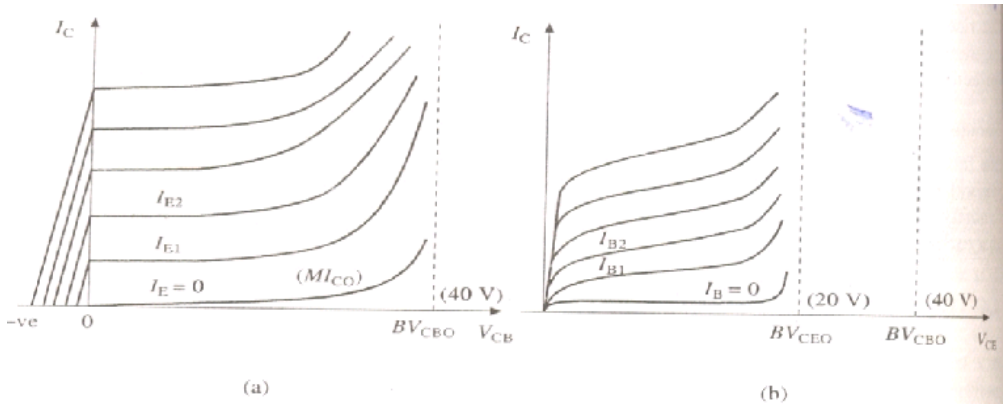


Fig. 3.6 a) CB characteristics extended into the breakdown region

b) Idealized CB characteristics extended into the breakdown region

If a current I_E is caused to flow through the emitter junction, then neglecting the avalanche effect, a fraction αI_E reaches the collector junction, where α is the common base current gain. Taking multiplication into account, *Ic* has the magnitude $M \propto I_E$. Consequently it appears that in the presence of avalanche multiplication, the transistor behaves as though its common base current gain were α* where α* = *Mα.*

The CE configuration

Since $h_{FE} = \alpha/(1 - \alpha)$, in the presence of avalanche multiplication the CE current gain is h^*_{FE}

$$h^*_{FE} = \frac{\alpha^*}{1-\alpha^*} = \frac{M\alpha}{1-M\alpha}$$

Now α is a positive number with a maximum magnitude less than unity but $M\alpha$ may equal unity in magnitude at which point h_{FE} becomes infinite. Accordingly, any base current no matter how small, will give rise to an arbitrarily large collector current whenever $M\alpha = 1$. It

means breakdown has occurred. Therefore, whenever the base current is kept fixed, breakdown occurs at the voltage V_{CB} which satisfies the equation,

or breakdown occurs at the voltage V_{CB} given by

$$M = \frac{1}{1 - \left(\frac{V_{CB}}{BV_{CBO}}\right)^n} = \frac{1}{\alpha}$$

Since V_{CB} at breakdown is much larger than the small forward base-to-emitter voltage V_{BE}, we may replace V_{CB} by V_{CE} in the above equation. Also

$$1-\alpha = \alpha/h_{FE} \approx 1/ h_{FE}$$

Therefore, the collector-to-emitter breakdown voltage, with open-circuited base, BV_{CEO} *is*

$$BV_{CEO} = BV_{CBO} \sqrt[n]{\frac{1}{h_{FE}}}$$

For an n-p-n Ge transistor, a reasonable value for *n* is 6. If $h_{FE} = 50$, then $BV_{CEO} = BV_{CBO} \sqrt{50} = 0.52BV_{cBo}$· If $BV_{CEO} = 40$ V, BV_{CBO} is about half of that, i.e. about 20 V.

3.8. Transistor in Saturation:

When a transistor switch is driven from saturation to cut-off, one of the factors which have an important effect on the speed of response is the time required to charge the capacitance which appears in shunt across the output terminals of the transistor. This capacitance must charge through the load resistance R_L and for this reason, in fast switching circuits, *RL* must be kept small. In saturation, the transistor current is nominally *Vcc / R_L*, and since" R_L is small, it may be necessary to keep *Vcc* correspondingly small in' order to stay within the limitations imposed by the transistor on the maximum current and, dissipation. The total voltage swing at the transistor switch is *Vcc* - *V* $_{CE}$(sat).f The largest possible output swing is desirable in order to reduce the sensitivity of the switching circuit to noise, supply voltage fluctuations, transistor ageing, and replacement.

For the transistor switch of Fig.3.7 (a), it is difficult to read V_{CE}(sat) from Fig. 3.7(b). By changing scale, *Fig. 3.7(b)* can be drawn as shown in *Fig.3.7 (c).* In these characteristics, the 0 to - 0.5 V region of *Fig 3.7(b)* has been expanded and the same load line is drawn. At I_B = - 0.15 mA, the transistor is in saturation and $|V_{CE}|$ = l75 mV. At I_B = -0.35mA, $|V_{CE}|$ has dropped to 100 mV. For a transistor operating in the saturation region, a quantity of interest

is the ratio $V_{CE}(sat)I$ I_c. This parameter is called the common emitter saturation resistance, RCE(sat).

The saturation voltage V_{CE}(sat) depends not only on the operating point but also on the semiconductor material (Ge or Si) and on the type of transistor construction. Alloy-junction transistors and epitaxial transistors give the lowest values for V_{CE}(sat), whereas the grown junction transistors yield the highest Germanium transistors have lower values for V_{CE}(sat) than those for silicon. An alloy-junction Ge transistor may allow, with adequate base currents, values for V_{CE}(sat) as low as tens of mill volts at collector currents which are some tens of mill amperes. Similarly, epitaxial silicon transistors may yield saturation voltage as low as 0,2 V with collector currents as high as an ampere. On the other hand, the grown junction Ge transistors have saturation voltages which are several tenths of a volt and silicon transistors of this type may have saturation voltages as high as several volts.

The dc current gain: (h_{FE} or β)

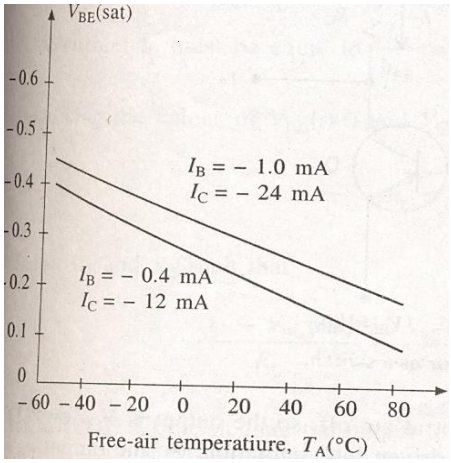
In the saturation region, h_{FE} is a useful parameter and is supplied by the manufacturer. Once we know, $Ic(= Vcc /R_L)$ and h_{FE}, the amount of base current $I_B = Ic / h_{FE}$ needed to saturate the transistor can be found.

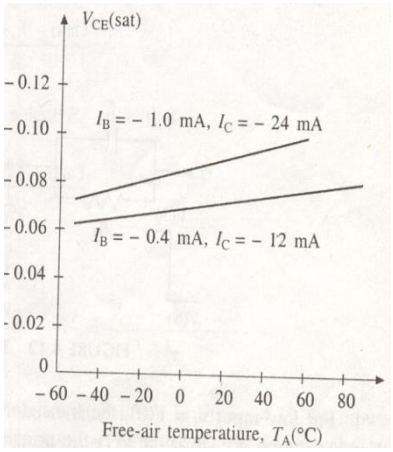
3.8. Temperature Sensitivity of Saturation Parameters:

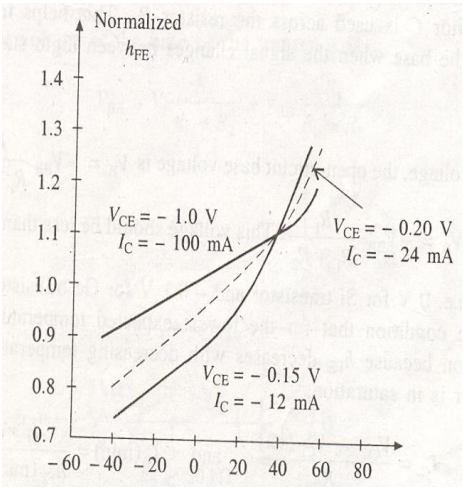
At constant base and collector currents, the forward base-to-emitter voltage $|V_{BE}|$ has typical temperature sensitivity in the range -1.5 to -2 mV/ºC. This applies both to Ge and Si transistors. A plot for Ge of V_{BE} versus the ambient temperature is shown in *Fig.3.7 (a).* A similar characteristic for silicon has approximately the same slope.

In saturation, the transistor consists of two forward-biased junctions' back-to-back, series opposing. It is consequently to be anticipated that the temperature induced voltage change in one junction will be cancelled in some measure by the change in the other junction. Such is the case for V_{BE} (sat) as well, as shown in *Fig.3.7 (b).*

The temperature dependence of h_{FE} is shown in *Fig. (c).* at small and moderate currents, h_{FE} increases substantially with temperature. At high currents, h_{FE} may well become rather insensitive to temperature.







3.7(a) &B a plot for Ge of VBE & VCE versus the ambient temperature (c) temperature dependence of hFE

3.9. Silicon-Controlled –Switch Circuits:

If we take the equivalent circuit for an SCR and add another external terminal, connected to the base of the top transistor and the collector of the bottom transistor, we have a device known as a silicon-controlled-switch, or SCS:

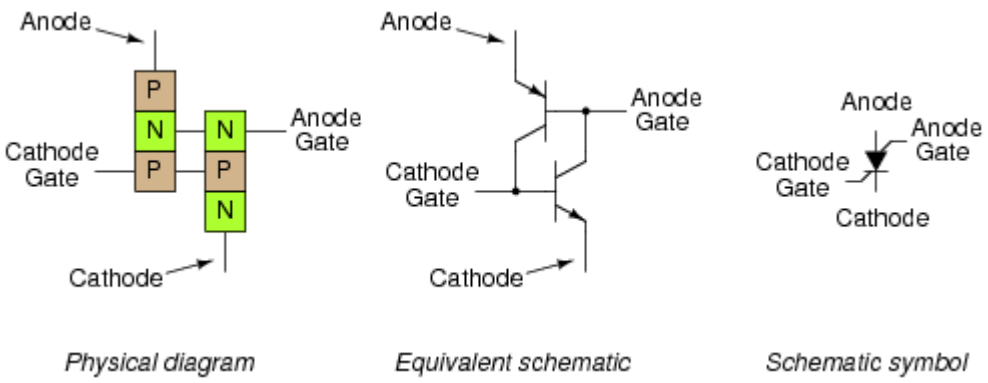


Fig.3.8 Silicon-Controlled Switch (SCS)

This extra terminal allows more control to be exerted over the device, particularly in the mode of forced commutation, where an external signal forces it to turn off while the main current through the device has not yet fallen below the holding current value. Note that the motor is in the anode gate circuit in Figure below. This is correct, although it doesn't look right. The anode lead is required to switch the SCS off. Therefore the motor cannot be in series with the anode.

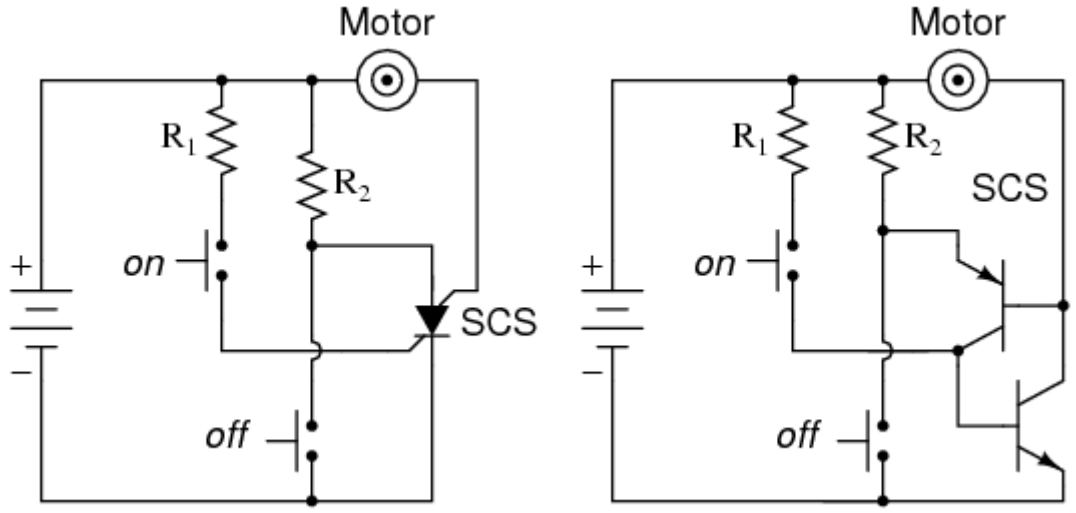


Fig.3.9.SCS: Motor start/stop circuit, equivalent circuit with two transistors.

When the "on" pushbutton switch is actuated, the voltage applied between the cathode gate and the cathode, forward-biases the lower transistor's base-emitter junction, and turning it on. The top transistor of the SCS is ready to conduct, having been supplied with a current path from its emitter terminal (the SCS's anode terminal) through resistor R2 to the positive side of the power supply. As in the case of the SCR, both transistors turn on and maintain

each other in the "on" mode. When the lower transistor turns on, it conducts the motor's load current, and the motor starts and runs.

The motor may be stopped by interrupting the power supply, as with an SCR, and this is called natural commutation. However, the SCS provides us with another means of turning off: forced commutation by shorting the anode terminal to the cathode. If this is done (by actuating the "off" pushbutton switch), the upper transistor within the SCS will lose its emitter current, thus halting current through the base of the lower transistor. When the lower transistor turns off, it breaks the circuit for base current through the top transistor (securing its "off" state), and the motor (making it stop). The SCS will remain in the off condition until such time that the "on" pushbutton switch is re-actuated.

UNIT-4

MULTIVIBRATORS

4.1 INTRODUCTION

Multivibrator is a switching circuit and may be defined as an electronic circuit that generates non-sinusoidal waves such as rectangular waves, saw tooth waves, square waves etc. Multivibrators are capable of storing binary number, counting pulses, synchronizing arithmetic operations and performing other essential functions used in digital systems.

Multivibrators are Sequential regenerative circuits either synchronous or asynchronous that are used extensively in timing applications. Multivibrators produce an output wave shape of a symmetrical or Asymmetrical square wave and are the most commonly used of all the square wave generators. Multivibrators belong to a family of oscillators commonly called relaxation oscillators.

A multivibrator is an electronic circuit used to implement a variety of simple two-state systems such as oscillators, timers and flip-flops. It is characterized by two amplifying devices (transistors, electron tubes or other devices) cross-coupled by resistors or capacitors. The name "multivibrator" was initially applied to the free-running oscillator version of the circuit because its output waveform was rich in harmonics. There are three types of multivibrator circuits depending on the circuit operation:

4.1.1 Basic configuration of a Multivibrator

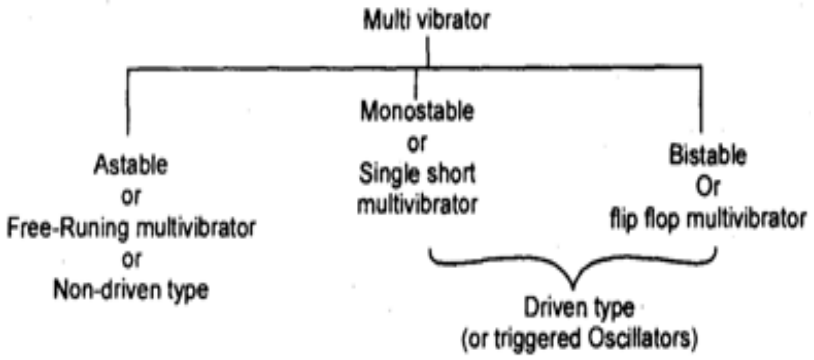


Fig. 4.1 Classification of Multivibrators

1. Generation of Non-sinusoidal waveform (square, Rectangular saw tooth, etc.)
2. Pulses occurring periodically, frequency division, synchronized generation of pulses and extended waveform, generation of time delays, storage of binary bit of information etc.

- **Astable**, in which the circuit is not stable in either state —it continually switches from one state to the other. It does not require an input such as a clock pulse.

- **Monostable**, in which one of the states is stable, but the other state is unstable (transient). A trigger causes the circuit to enter the unstable state. After entering the unstable state, the circuit will return to the stable state after a set time. Such a circuit is useful for creating a timing period of fixed duration in response to some external event. This circuit is also known as a **one shot**.
- **Bistable**, in which the circuit is stable in either state. The circuit can be flipped from one state to the other by an external event or trigger.

Multivibrators find applications in a variety of systems where square waves or timed intervals are required. For example, before the advent of low-cost integrated circuits, chains of multivibrators found use as frequency dividers. A free-running multivibrator with a frequency of one-half to one-tenth of the reference frequency would accurately lock to the reference frequency. This technique was used in early electronic organs, to keep notes of different octaves accurately in tune. Other applications included early television systems, where the various line and frame frequencies were kept synchronized by pulses included in the video signal.

4.2 ASTABLE MULTIVIBRATOR USING TRANSISTOR:

Regenerative switching circuits such as **Astable Multivibrators** are the most commonly used type of relaxation oscillator as they produce a constant square wave output waveform as well as their simplicity, reliability and ease of construction. Unlike the **Monostable Multivibrator** and the **Bistable Multivibrator** that require an "external" trigger pulse for their operation, the **Astable Multivibrator** switches continuously between its two unstable states without the need for any external triggering.

The **Astable Multivibrator** is another type of cross-coupled transistor switching circuit that has **NO** stable output states as it changes from one state to the other all the time. The astable circuit consists of two switching transistors, a cross-coupled feedback network, and two time delay capacitors which allow oscillation between the two states with no external trigger signal to produce the change in state. Astable multivibrators are therefore also known as **Free-running Multivibrator** that can produce a continuous square wave from its output or outputs, (two outputs no inputs) which can then be used to flash lights or produce a sound in a loudspeaker.

The basic transistor circuit for an **Astable Multivibrator** produces a square wave output from a pair of grounded emitter cross-coupled transistors is shown in Fig. 4.2. Both transistors either NPN or PNP, in the multivibrator are biased for linear operation and are operated as **Common Emitter Amplifiers** with 100% positive feedback. This configuration satisfies the condition for oscillation when: ($\beta A = 1\angle 0^o$). This results in one stage conducting "fully-ON" (Saturation) while the other is switched "fully-OFF" (cut-off) giving a very high level of mutual amplification between the two transistors. Conduction is transferred from one stage to the other by the discharging action of a capacitor through a resistor as shown below.

Basic Astable Multivibrator Circuit

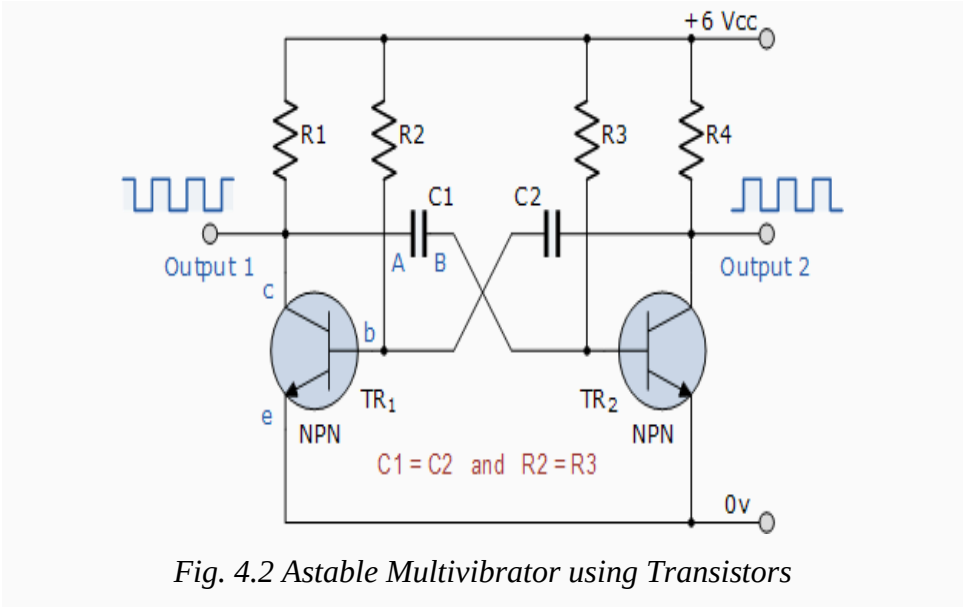


Fig. 4.2 Astable Multivibrator using Transistors

4.2.1 Operation:

Assume that transistor, TR_1 has just switched "OFF" and its collector voltage is rising towards Vcc, meanwhile transistor TR_2 has just turned "ON". Plate "A" of capacitor C1 is also raising towards the +6 volts supply rail of Vcc as it is connected to the collector of TR_1. The other side of capacitor, C1, plate "B", is connected to the base terminal of transistor TR_2 and is at 0.6v because transistor TR_2 is conducting therefore, capacitor C1 has a potential difference of 5.4 volts across it, 6.0 - 0.6v, (its high value of charge). The instant

that transistor, TR_1 switches "ON", plate "A" of the capacitor immediately falls to 0.6 volts. This fall of voltage on plate "A" causes an equal and instantaneous fall in voltage on plate "B" therefore plate "B" of the capacitor C1 is pulled down to -5.4v (a reverse charge) and this negative voltage turns transistor TR_2 hard "OFF", One unstable state.

Capacitor C1 now begins to charge in the opposite direction via resistor R3 which is also connected to the +6 volts supply rail, Vcc, thus the base of transistor TR_2 is moving upwards in a positive direction towards Vcc with a time constant equal to the C1.R3 combination. However, it never reaches the value of Vcc because as soon as it gets to 0.6 volts positive, transistor TR_2 turns fully "ON" into saturation starting the whole process over again but now with capacitor C2 taking the base of transistor TR_1 to-5.4v while charging up via resistor R2 and entering the second unstable state. This process will repeat itself over and over again as long as the supply voltage is present.

The amplitude of the output waveform is approximately the same as the supply voltage, Vcc with the time period of each switching state determined by the time constant of the RC networks connected across the base terminals of the transistors. As the transistors are switching both "ON" and "OFF", the output at either collector will be a square wave with slightly rounded corners because of the current which charges the capacitors. This could be corrected by using more components as we will discuss later.

If the two time constants produced by C2.R2 and C1.R3 in the base circuits are the same, the mark-to-space ratio (t1/t2) will be equal to one-to-one making the output waveform symmetrical in shape. By varying the capacitors, C1, C2 or the resistors, R2, R3 the mark-to-space ratio and therefore the frequency can be altered.

In the **RC Discharging**, the time taken for the voltage across a capacitor to fall to half the supply voltage, 0.5Vcc is equal to 0.69 time constants of the capacitor and resistor combination. Then taking one side of the astable multivibrator, the length of time that transistor TR_2 is "OFF" will be equal to 0.69T or 0.69 times the time constant of C1.R3. Likewise, the length of time that transistor TR_1 is "OFF" will be equal to 0.69T or 0.69 times the time constant of C2.R2 and this is defined as.

Periodic Time, T = t1 + t2

$t1 = 0.69R_1C_3$

$t2=0.69C_2R_2$

where R in ohms, and C in farads

By altering the time constants of just one RC network the mark-to-space ratio and frequency of the output waveform can be changed but normally by changing both RC time constants together at the same time, the output frequency will be altered keeping the mark-to-space ratios the same at one-to-one.

If the value of the capacitor C1 equals the value of capacitor C2, C1=C2 and also the value of the base resistor R2 equals the value of base resistor R3, R2=R3 then the total length of time of the multivibrators cycle is given below for a symmetrical waveform.

Frequency of Oscillation

$$f=1/T=1/1.38RC$$

where R in ohms, and C in farads, T is in seconds and f is in Hertz

\and this is known as the "Pulse repetition Frequency". So Astable Multivibrator can produce two very shot square wave output waveforms from each transistor or a much longer rectangular shaped output either symmetrical or non-symmetrical depending upon the time constant of the network as shown below.

Astable Multivibrator Output waveforms:

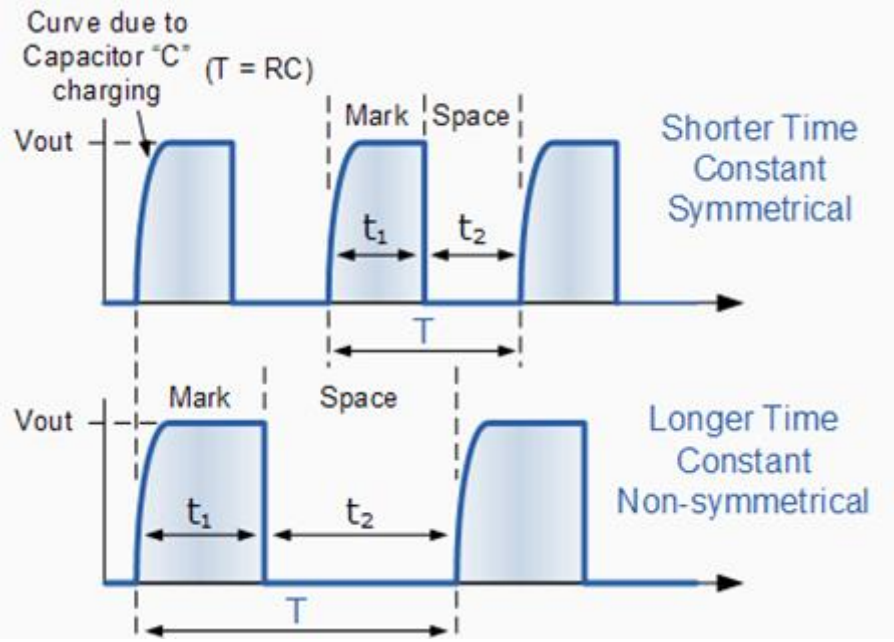


Fig. 4.3 Astable Multivibrator Output waveforms

4.3 MONOSTABLE MULTIVIBRATOR:

Monostable Multivibrators have only **one** stable state (hence their name: "Mono"), and produce a single output pulse when it is triggered externally. Monostable multivibrators only return back to their first original and stable state after a period of time determined by the time constant of the RC coupled circuit.

Monostable multivibrators or "One-Shot Multivibrators" as they are also called, are used to generate a single output pulse of a specified width, either "HIGH" or "LOW" when a suitable external trigger signal or pulse T is applied. This trigger signal initiates a timing cycle which causes the output of the monostable to change its state at the start of the timing cycle and will remain in this second state, which is determined by the time constant of the timing capacitor, C_T and the resistor, R_T until it resets or returns itself back to its original (stable) state. It will then remain in this original stable state indefinitely until another input pulse or trigger signal is received. Then, **Monostable Multivibrators** have only **ONE** stable state and go through a full cycle in response to a single triggering input pulse.

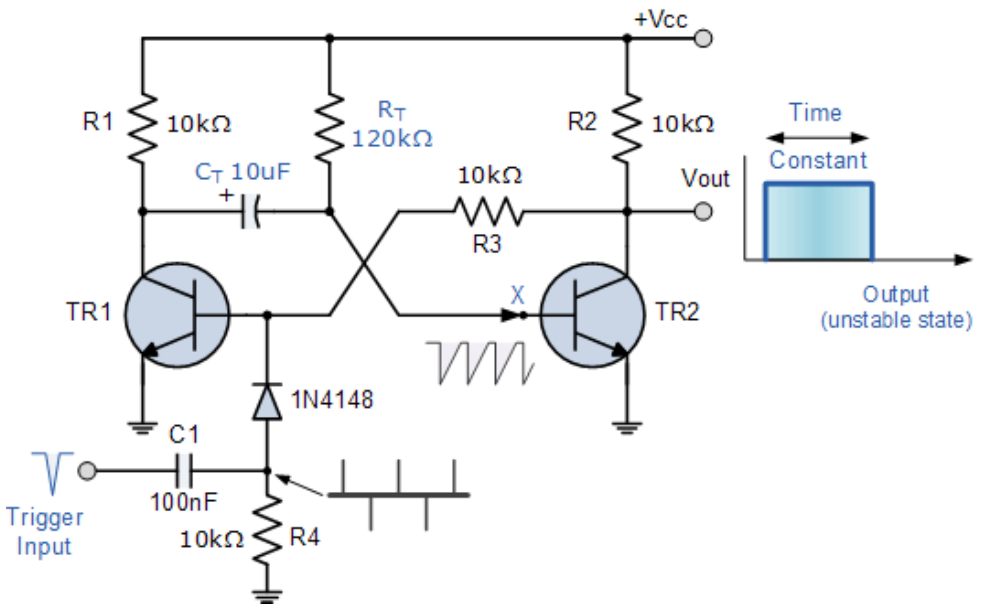


Fig. 4.4. Monostable Multivibrator using Transistor

4.3.1 Operation:

The basic collector-coupled **Monostable Multivibrator** circuit and its associated waveforms are shown in Fig. 4.4. When power is firstly applied, the base of transistor TR2 is connected to Vcc via the biasing resistor, R_T thereby turning the transistor "fully-ON" and into saturation and at the same time turningTR1 "OFF" in the process. This then represents the circuits "Stable State" with zero output. The current flowing into the saturated base terminal of TR2 will therefore be equal to Ib = (Vcc - 0.7)/R_T.

If a negative trigger pulse is now applied at the input, the fast decaying edge of the pulse will pass straight through capacitor, C1 to the base of transistor, TR1 via the blocking diode turning it "ON". The collector of TR1 which was previously at Vcc drops quickly to below zero volts effectively giving capacitor C_T a reverse charge of -0.7v across its plates. This action results in transistor TR2 now having a minus base voltage at point X holding the transistor fully "OFF". This then represents the circuits second state, the "Unstable State" with an output voltage equal to Vcc.

Timing capacitor, C_T begins to discharge this -0.7v through the timing resistor R_T, attempting to charge up to the supply voltage Vcc. This negative voltage at the base of transistor TR2 begins to decrease gradually at a rate determined by the time constant of

the R_T C_T combination. As the base voltage ofTR2 increases back up to Vcc, the transistor begins to conduct and doing so turns "OFF" again transistor TR1 which results in the monostable multivibrator automatically returning back to its original stable state awaiting a second negative trigger pulse to restart the process once again.

Monostable Multivibrators can produce a very short pulse or a much longer rectangular shaped waveform whose leading edge rises in time with the externally applied trigger pulse and whose trailing edge is dependent upon the RC time constant of the feedback components used. This RC time constant may be varied with time to produce a series of pulses which have a controlled fixed time delay in relation to the original trigger pulse as shown in Fig. 4.5.

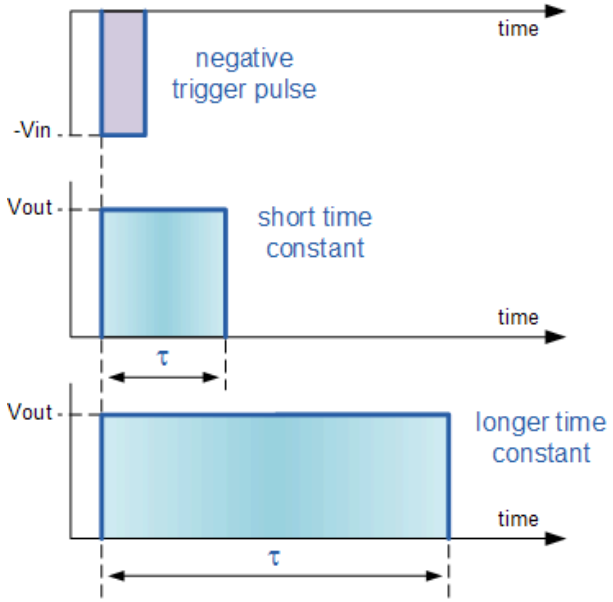


Fig. 4.5 Monostable Multivibrator Output waveforms

The time constant of **Monostable Multivibrators** can be changed by varying the values of the capacitor, C_T the resistor, R_T or both. Monostable multivibrators are generally used to increase the width of a pulse or to produce a time delay within a circuit as the frequency of the output signal is always the same as that for the trigger pulse input, the only difference is the pulse width.

4.4 Bistable Multivibrator:

Bistable Multivibrators are another type of two state devices similar to the Monostable Multivibrator we looked at in the last tutorial but the difference this time is that both states are stable. Bistable Multivibrators have TWO stable states (hence the name: "Bi"), and they can be switched over from one stable state to the other by the application of a trigger pulse. As Bistable Multivibrators have two stable states they are more commonly known as Flip-flops for use in sequential type circuits.

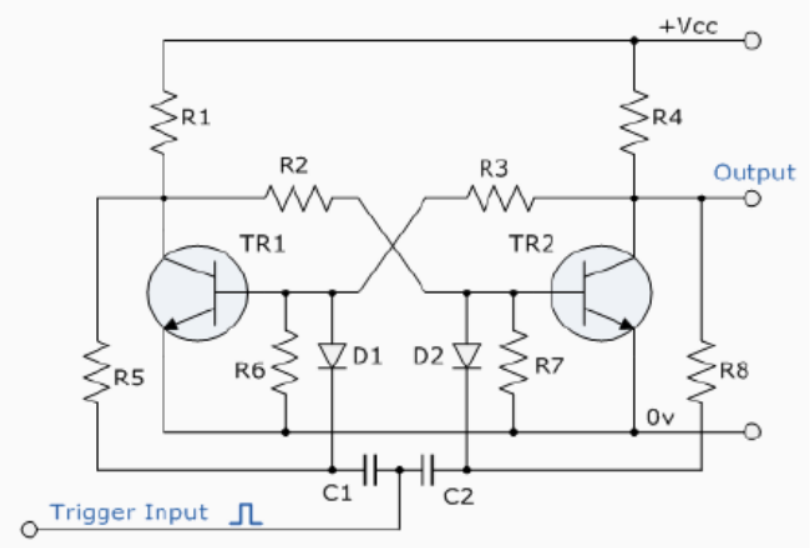


Fig. 4.6 Bistable Multivibrator using Transistor

Bistable Multivibrators are two state non-regenerative devices and in each state one of the transistors is cut-off while the other transistor is in saturation, this means that the bistable circuit is capable of remaining indefinitely in either stable state. To change over from one state to the other the circuit requires a suitable trigger pulse and to go through a full cycle, two triggering pulses, one for each stage are required. Its more common name or term of " Flip-flop " relates to the actual operation of the device, as it "Flips" into one logic state, remains there and then changes or "Flops" back into its first original state. The Bistable Multivibrator circuit above is stable in both states, either with one transistor "OFF" and the other "ON" or with the first transistor "ON" and the second "OFF". Switching between the two states is achieved by applying a trigger pulse which in turn will cause the "ON" transistor to turn "OFF". The circuit will switch sequentially by applying a pulse to each base in turn and this is achieved from a single input trigger pulse using biased diodes as a steering circuit. Equally, we could remove the diodes, capacitors and feedback resistors and apply individual

trigger pulses directly to the transistor Bases. Then unlike Monostable Multivibrators whose output is dependent upon the RC time constant of the feedback components used, the Bistable Multivibrators output is dependent upon the application of two individual trigger pulses. So Monostable Multivibrators can produce a very short output pulse or a much longer rectangular shaped output whose leading edge rises in time with the externally applied trigger pulse and whose trailing edge is dependent upon a second trigger pulse as shown below.

Bistable multivibrator waveform:

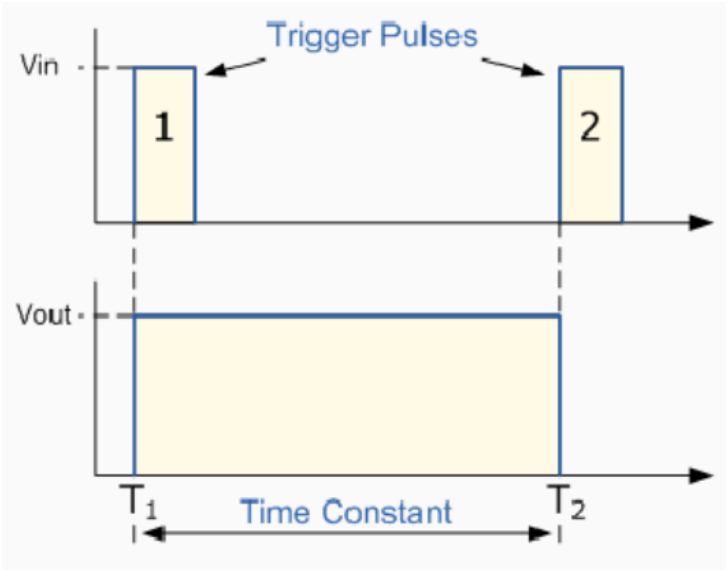


Fig. 4.7 Bistable multivibrator output waveform

Bistable Multivibrators have many applications such as part of a counting circuit, or as a one-bit memory device in a computer, or as frequency dividers because the output pulses have a frequency that are exactly one half (f/2) that of the trigger input pulse frequency due to them changing state from a single input pulse. In other words the circuit produces Frequency Division as it now divides the input frequency by a factor of two (an octave

Problems:

1. Design a fixed-bias bistable multivibrator using Ge transistors having $h_{FE(\min)} = 50$, $V_{CC} = 10$ V and $V_{BB} = 10$ V, $V_{CE(sat)} = 0.1$ V, $V_{BE(sat)} = 0.3$ V, $I_{C(sat)} = 5$ mA and assume $I_{B(sat)} = 1.5I_{B(min)}$.

Solution:

$$R_C = \frac{V_{CC} - V_{CE(sat)}}{I_{C2}} = \frac{10 - 0.1 \text{ V}}{5 \text{ mA}} = \frac{9.9 \text{ V}}{5 \text{ mA}}$$

$$= 1.98 \text{ k}\Omega$$

$$R_2 = \frac{V_\sigma - (-V_{BB})}{I_2}$$

$$\text{Choose } I_2 \approx \frac{1}{10} I_{C2}$$

$$= 0.5 \text{ mA}$$

$$\therefore R_2 = \frac{0.3 + 10}{0.5} = \frac{10.3 \text{ V}}{0.5 \text{ mA}} = 20.6 \text{ k}\Omega$$

$$I_{B2\min} = \frac{I_{C2}}{h_{FE\min}} = \frac{5 \text{ mA}}{50} = 0.1 \text{ mA}$$

If Q_2 is in saturation

$$I_{B2} = 1.5 I_{B2\min}$$

$$= 0.15 \text{ mA}$$

$$I_1 = I_2 + I_{B2}$$

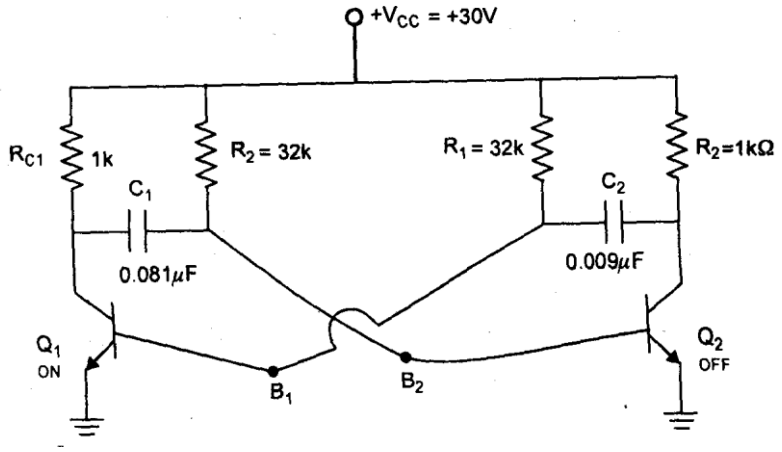
$$= 0.5 \text{ mA} + 0.15 \text{ mA} = 0.65 \text{ mA}$$

$$R_C + R_1 = \frac{V_{CC} - V_\sigma}{I_1} = \frac{10 - 0.3}{0.65 \text{ mA}} = \frac{9.7 \text{ V}}{0.65 \text{ mA}} = 14.92 \text{ k}\Omega$$

$$R_1 = (R_C + R_1) - R_C$$

$$= 14.92 - 1.98 = 12.94 \text{ k}\Omega.$$

Problem 4.2. Design an astable multivibrator the repetition rate is 500 Hz and pulse width is 0.2 ms. Use two transistors with h_{fe} = 50, $V_{CC} = V_{BB}$ = 20V $RC_1 = RC_2$ = 1 K.



Collector resistances

$$R_{C1} = R_{C2} = 1K\Omega$$

Repetition rate, $f = 500\ Hz$

Pulse width Pw=0.2ms

Transistors hfe = 50

$$V_{CC} = V_{BB} = 20V$$

Let the junction voltages be

$$V_{CE(sat)} = 0.3V \text{ and } V_{BE(sat)} = 0.7V$$

$$I_{CE(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{20 - 0.3}{1K\Omega} = 20mA.$$

$$I_{B(} = \frac{I_{C(sat)}}{R_C} = \frac{20 - 0.3}{1K\Omega} = 0.4\ mA$$

Let us take I_B (actual) 1.5 times I_B (min) = 1.5 x 0.4 mA =0.6 mA

Let us assume that the transistor are driven equally into saturation during their conducting period

$$\therefore \quad R_1 = R_2 = R$$

$$R = \frac{V_{BB(sat)} - V_{BE(sat)}}{I_B} = \frac{20 - 0.7}{0.6mA} = 32K\Omega$$

And

Time period, $$T = \frac{1}{f} = \frac{1}{500} = 2\ ms$$

Duty cycle $$\frac{\text{Pulse width}}{T} = \frac{0.2}{2} = 0.1$$

$\therefore$ $T_2 = 0.1T = 0.1 \times 2ms = 0.2ms$

and $T_1 = T - T2 = 2 - 0.2 = 1.8ms$

$\therefore$ $\frac{T_2}{T} = 0.1$

$$C_1 = \frac{T_1}{0.693R_2} = \frac{1.8 \times 10^{-3}}{0.693 \times 32 \times 10^3} = 0.081\ \mu F$$

and

$$C_2 = \frac{T_2}{0.693R_1} = \frac{0.2 \times 10^{-3}}{0.693 \times 32 \times 10^3} = 0.009\ \mu F.$$

4.5 Triggering in multivibrators:

Triggering is the process of applying an external signal to induce transition from one state to another. The signal used for triggering is either a pulse of short duration or a step voltage. There are two processes of triggering i.e. unsymmetrical triggering and symmetrical triggering.

In multivibrators there are two types of triggering

1. Unsymmetrical triggering
2. symmetrical triggering

Unsymmetrical triggering is a process in which the signal is effective in inducing transition only in one direction. If reverse transition is to be introduced, a second triggering signal from a separate source has to be introduced in a different manner.

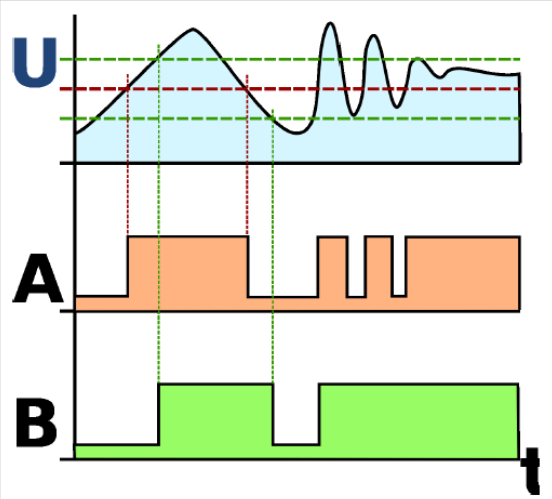
Symmetrical triggering is a process in which each successive triggering signal induces a transition, regardless of the state in which the binary happens to be. Thus, symmetrical triggering requires one source to produce transition whereas in unsymmetrical triggering, two separate sources are required. Triggering signals may be applied at the output of a stage or the input of a stage.

In case of transistors, these signals may be applied at the collector or at the base of the transistor. Symmetrical triggering is used in binary counting circuits and in other applications.

Unsymmetrical triggering is used in logic circuitry (in electronic registers, coding etc.) and is also used as a generator of a gate whose width equals the interval between triggers.

4.6. Schmitt Trigger:

In electronics, **Schmitt trigger** is a circuit with positive feedback and a loop gain >1. The circuit is named "trigger" because the output retains its value until the input changes sufficiently to trigger a change: in the non-inverting configuration, when the input is higher than a certain chosen threshold, the output is high; when the input is below a different (lower) chosen threshold, the output is low; when the input is between the two, the output retains its value. This dual threshold action is called *hysteresis* and implies that the Schmitt trigger possesses memory and can act as a bi-stable circuit (latch). There is a close relation between the two kinds of circuits: a Schmitt trigger can be converted into a latch and a latch can be converted into a Schmitt trigger. Schmitt trigger devices are typically used in open-loop controller configurations for noise immunity and closed loop negative feedback configurations to implement bi-stable regulators, triangle/square wave generators, etc.

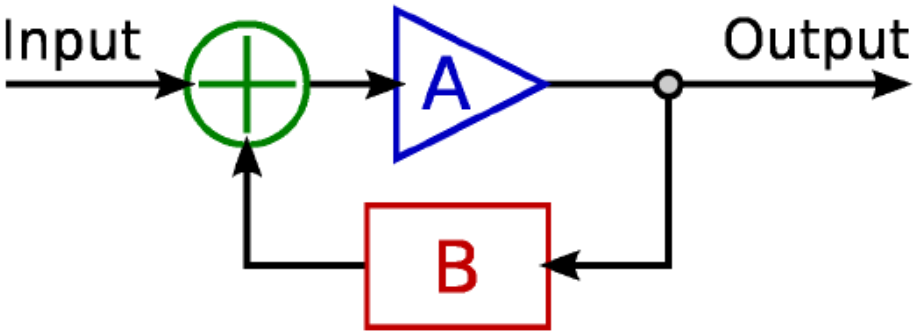


The effect of using a Schmitt trigger (B) instead of a comparator (A).

4.6.1. Fundamental Idea:

Circuits with hysteresis are based on the fundamental positive feedback idea: any active circuit can be made to behave as a Schmitt trigger by applying a positive feedback so that the loop gain is more than one. The positive feedback is introduced by adding a part of the output voltage to the input voltage; so, these circuits contain an attenuator (the B box in

the figure on the right) and a summer (the circle with "+" inside) in addition to an amplifier acting as a comparator. There are three specific techniques for implementing this general idea. The first two of them are dual versions (series and parallel) of the general positive feedback system. In these configurations, the output voltage increases the effective difference input voltage of the comparator by decreasing the threshold or by increasing the circuit input voltage; the threshold and memory properties are incorporated in one element. In the third technique, the threshold and memory properties are separated.



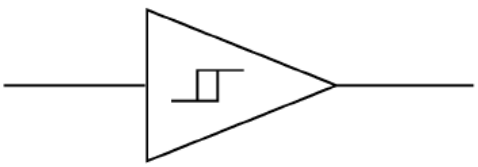
Schmitt trigger is a system with an avalanche-like positive feedback (B < 1; B.A > 1), in which the output helps the input

Dynamic threshold (series feedback):

When the input voltage crosses the threshold in some direction the very circuit changes its own threshold to the opposite direction. For this purpose, it subtracts a part of its output voltage from the threshold (it is equal to adding voltage to the input voltage). Thus the output affects the threshold and does not impact on the input voltage. These circuits are implemented by a differential amplifier with series positive feedback where the input is connected to the inverting input and the output - to the non-inverting input. In this arrangement, attenuation and summation are separated: a voltage divider acts as an attenuator and the loop acts as a simple series voltage summer. Examples: the classic transistor emitter-coupled Schmitt trigger, op-amp inverting Schmitt trigger, etc.

4.6.2. Modified input voltage (parallel feedback):

When the input voltage crosses the threshold in some direction the circuit changes the much input voltage in the same direction (now it adds a part of its output voltage directly to the input voltage). Thus the output "helps" the input voltage and does not affect the threshold. These circuits can be implemented by a single-ended non-inverting amplifier with parallel positive feedback where the input and the output sources are connected through resistors to the input. The two resistors form a weighted parallel summer incorporating both the attenuation and summation. Examples: the less familiar collector-base coupled Schmitt trigger, op-amp non-inverting Schmitt trigger, etc. Some circuits and elements exhibiting negative resistance can also act in a similar way: negative impedance converters (NIC), neon lamps, tunnel diodes (e.g., a diode with an "N"-shaped current–voltage characteristic in the first quadrant), etc. In the last case, an oscillating input will cause the diode to move from one rising leg of the "N" to the other and back again as the input crosses the rising and falling switching thresholds. **Two different unidirectional thresholds** are assigned in this case to two separate open-loop comparators (without hysteresis) driving an RS trigger (2-input memory cell). The trigger is toggled high when the input voltage crosses down to up the high threshold and low when the input voltage crosses up to down the low threshold. Again, there is a positive feedback but now it is concentrated only in the memory cell. Example: 555 timer, switch de-bounce circuit. The symbol for Schmitt triggers in circuit diagrams is a triangle with a symbol inside representing its ideal hysteresis curve.



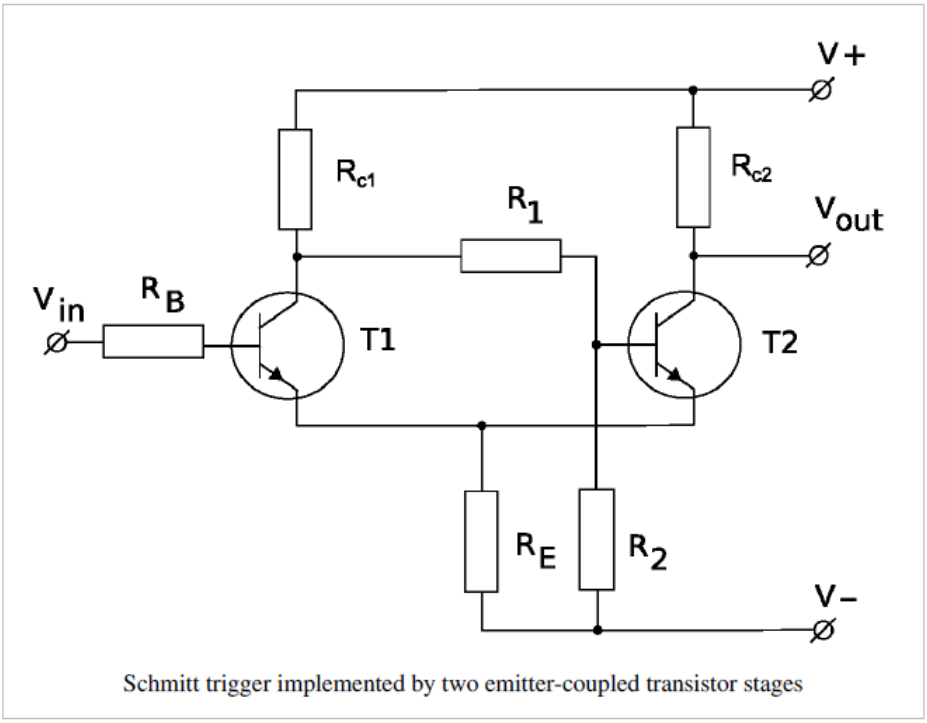
A symbol of Schmitt trigger shown with a non-inverting hysteresis curve embedded in a buffer. Schmitt triggers can also be shown with inverting hysteresis curves and may be followed by bubbles. The documentation for the particular Schmitt trigger being used must be consulted to determine whether the device is non-inverting (i.e., where positive output transitions are caused by positive-going inputs) or inverting (i.e., where positive output transitions are caused by negative-going inputs).

4.6.3. Schmitt triggers using transistor:

Classic emitter-coupled circuit

The original Schmitt trigger is based on the dynamic threshold idea that is implemented by a voltage divider with a switchable upper leg (the collector resistors Rc1 and Rc2) and a steady lower leg (RE). T1 acts as a comparator with a differential input (T1 base-emitter junction) consisting of an inverting (T1 base) and a non-inverting (T1 emitter) inputs. The input voltage is applied to the inverting input; the output voltage of the voltage divider is applied to the non-inverting input thus determining its threshold. The comparator output drives the second common collector stage T2 (an *emitter follower*) through the voltage follower R1-R2. The emitter-coupled transistors T1 and T2 actually compose an electronic double throw switch that switches over the upper legs of the voltage divider and changes the threshold in a different (to the input voltage) direction.

This configuration can be considered as a differential amplifier with series positive feedback between its non-inverting input (T2 base) and output (T1 collector) that forces the transition process. There is also a smaller negative feedback introduced by the emitter resistor RE. To make the positive feedback dominate over the negative one and to obtain a hysteresis, the proportion between the two collector resistors is chosen Rc1 > Rc2. Thus less current flows through and less voltage drop is across RE when T1 is switched on than in the case when T2 is switched on. As a result, the circuit has two different thresholds in regard to ground (V- in the picture).



Schmitt trigger implemented by two emitter-coupled transistor stages

4.6.3.1. Operation:

Initial state. For NPN transistors as shown, imagine the input voltage is below the shared emitter voltage (high threshold for concreteness) so that T1 base-emitter junction is backward-biased and T1 does not conduct. T2 base voltage is determined by the mentioned divider so that T2 is conducting and the trigger output is in the low state. The two resistors Rc2 and RE form another voltage divider that determines the high threshold. Neglecting VBE, the high threshold value is approximately

$$V_{HT} = \frac{R_E}{R_E + R_{c2}} V_+ .$$

The output voltage is low but well above the ground. It is approximately equal to the high threshold and may not be low enough to be a logical zero for next digital circuits. This may require additional shifting circuit following the trigger circuit.

Crossing up the high threshold:

When the input voltage (T1 base voltage) rises slightly above the voltage across the emitter resistor RE (the high threshold), T1 begins conducting. Its collector voltage goes down and T2 begins going cut-off, because the voltage divider now provides lower T2 base voltage. The common emitter voltage follows this change and goes down thus making T1 conduct more. The current begins steering from the right leg of the circuit to the left one. Although T1 is more conducting, it passes less current through RE (since Rc1 > Rc2); the emitter voltage continues dropping and the effective T1 base-emitter voltage continuously increases. This avalanche-like process continues until T1 becomes completely turned on (saturated) and T2 turned off. The trigger is transitioned to the high state and the output (T2 collector) voltage is close to V+. Now, the two resistors Rc1 and RE form a voltage divider that determines the low threshold. Its value is approximately

$$V_{LT} = \frac{R_E}{R_E + R_{c1}} V_+.$$

Crossing down the low threshold:

With the trigger now in the high state, if the input voltage lowers enough (below the low threshold), T1 begins cutting-off. Its collector current reduces; as a result, the shared emitter voltage lowers slightly and T1 collector voltage rises significantly. R1-R2 voltage divider conveys this change to T2 base voltage and it begins conducting. The voltage across RE rises, further reducing the T1 base-emitter potential in the same avalanche-like manner, and T1 ceases to conduct. T2 becomes completely turned-on (saturated) and the output voltage becomes low again.

Variations:

Non-inverting circuit.

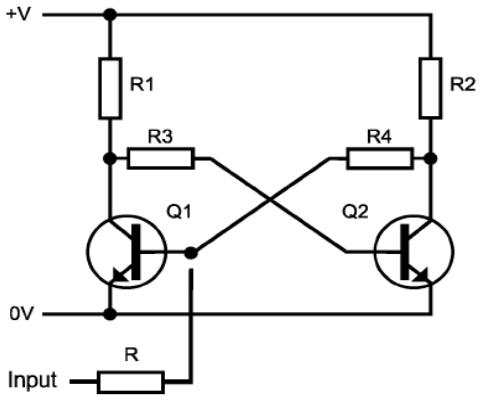
The classic non-inverting Schmitt trigger can be turned into an inverting trigger by taking Vout from the emitters instead from T2 collector. In this configuration, the output voltage is equal to the dynamic threshold (the shared emitter voltage) and both the output levels stay away from the supply rails. Another disadvantage is that the load changes the thresholds; so, it has to be high enough. The base resistor RB is obligatory to prevent the impact of the input voltage through T1 base-emitter junction on the emitter voltage.

Direct-coupled circuit:

To simplify the circuit, the R1 –R2 voltage divider can be omitted connecting T1 collector directly to T2 base. The base resistor RB can be omitted as well so that the input voltage source drives directly T1 base.[6] In this case, the common emitter voltage and T1 collector voltage are not suitable for outputs. Only T2 collector should be used as an output since, when the input voltage exceeds the high threshold and T1 saturates, its base-emitter junction is forward biased and transfers the input voltage variations directly to the emitters. As a result, the common emitter voltage and T1 collector voltage follow the input voltage. This situation is typical for over-driven transistor differential amplifiers and ECL gates.

4.6.4. Collector-base coupled circuit:

Like every latch, the fundamental collector-base coupled bistable circuit possesses a hysteresis. So, it can be converted to a Schmitt trigger by connecting an additional base resistor R to some of the inputs (Q1 base in the figure). The two resistors R and R4 form a parallel voltage summer (the circle in the block diagram above) that sums output (Q2 collector) voltage and the input voltage, and drives the single-ended transistor "comparator" Q1. When the base voltage crosses the threshold (VBE0 ∞ 0.65 V) in some direction, a part of Q2 collector voltage is added in the same direction to the input voltage. Thus the output modifies the input voltage by means of parallel positive feedback and does not affect the threshold (the base-emitter voltage).



BJT bistable collector-base coupled circuit can be converted to a Schmitt trigger by connecting an additional base resistor to some of the bases

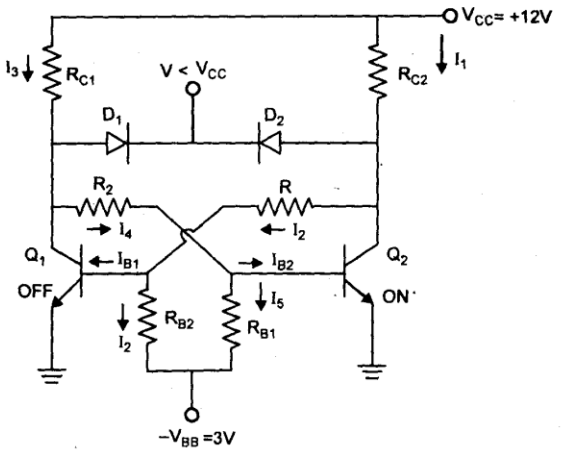
4.6.5. Comparison between emitter- and collector-coupled Circuits:

The emitter-coupled version has the advantage that the input transistor is backward-biased when the input voltage is quite below the high threshold; so, the transistor is surely cut-off. It was important when germanium transistors were used for implementing the circuit and this advantage has determined its popularity. The input base resistor can be omitted since the emitter resistor limits the current when the input base-emitter junction is forward-biased. The emitter-coupled Schmitt trigger has not low enough level at output *logical zero* and needs an additional output shifting circuit. The collector-coupled trigger has extremely low (almost zero) output level at output *logical zero*.

Problem 4.3: A fixed bias binary uses npn silicon transistors with h_k = 20, Vcc = 12V, V_{bb} = 3V, Rc =1 K, R1 = 5K, R2 = 10K. Verify that one transistor is cut off and other transistor is in saturation. Find stable currents and voltages if V_{ce} (sat) = 0.4 V, $V_{BE}(sat) = 0.8V$.

Ans:

For a bistable multivibrator, assume transistor Q_2 in "ON" state and transistor Q_1 in "OFF" state in one of the stable states. Neglecting junction voltages, diode D_1 is "ON" and diode D_2 is "OFF". The currents are shown in circuit diagram.



R_{C1} = 1 KΩ
R_{C2} = 1 KΩ
R_2 = 5 KΩ
R_1 = 5 KΩ
R_{B1} = 10 KΩ
R_{B2} = 10 KΩ
R = 0.4 V
$V_{CE}(sat)$ = 0.8 V
$V_{BE}(sat)$ = 20

Current $$I_1 = \frac{V_{CC} - V_{C2}}{R_{C2}} = \frac{V_{CC} - V_{CE2\,(sat)}}{R_{C2}} = \frac{12 - 0.4}{1K\Omega}$$ =11.6mA

Current $$I_2 = \frac{V_{C2} - (-V_{BB})}{R_1 + R_{B2}} = \frac{V_{CE2(sat)} - (-V_{BB})}{R_1 + R_{B2}}$$

$$= \frac{0.4 - (-3)}{(5+10)K\Omega} = \frac{3.4}{15}$$ mA = 0.2267mA

Collector current of $Q_{2'}$

$$I_{C2} = I_1 - I_2 = 11.6 - 0.22667 = 11.373333 \text{ mA}$$

Minimum base current required for Q_2 to be "ON"

$$I_{B2}(min) = \frac{I_{C2}}{h_{fe}} = \frac{11.373333}{20} = 0.56867 \text{ mA}$$

Base voltage of $Q_{1'}$

$$V_{B1} = V_{C2} - I_2R_1 = 0.4 - (0.2267)5 = —0.7335 \text{ V}$$

Also, $$V_{B1} = -V_{BB} \times \frac{R_1}{R_1 + R_{B2}} = \frac{-3 \times 5}{5+10} = -1V.$$

Since base to emitter voltage of 'Q1' is negative (transistor being N-P-N type), transistor is in cut-off.

Since the diode D_1 is "ON"

Current $$I_3 = \frac{V_{CC} - V_{C1}}{R_{C1}} = \frac{12 - 12}{1K\Omega} = 0$$

Current $I_4 = \frac{V_{C1} - V_{B2}}{R_2} = \frac{V_{C1} - V_{BE2}(sat)}{R_2}$

$= \frac{12 - 0.8}{5K}$ =2.24mA

Diode current, $I_D = I_3 - I_4$ = 0 — 2.24

= (-2.24) mA

Current $I_5 = \frac{V_{B2} - (-V_{BB})}{R_{B1}} = \frac{V_{BE2}(sat) - (-V_{BB})}{R_{B1}}$

$= \frac{0.8 - (-3)}{10K} = \frac{3.8}{10}$ =—=0.38mA

Current I_{B2} (actual) $= I_4 - I_5$

= 2.24 - 0.38 = 1.86mA

Since I_{B2} (actual) is much larger than I_{B2} (min) transistor Q_2 is really "ON" and the stable state with Q_2 "ON" and Q1 "OFF" is confirmed.

The stable state voltages and current are

V_{C1} =12V

V_{C2} =O.4V

V_{B1} = -1V

V_{B2} =0.8V

$I_{C1} = I_3 - I_4$ = 0 mA

I_{C2} = 11.3733 mA

I_{B1} = 0 mA

I_{B2} =1.86 mA

UNIT-5

TIME BASE GENERATORS

5.1 Introduction

A linear time-base circuit is one that provides an output waveform, a portion of which exhibits a linear variation of voltage with time. An application of first importance of such a waveform is in connection with a cathode-ray oscilloscope. The display on the screen of a scope of the variation with respect to time of an arbitrary waveform requires that there be applied to one set of deflecting plates a voltage which varies linearly with time. Since this waveform is used to ***sweep*** the electron beam horizontally across the screen, it is called a ***sweep voltage***. There are in addition many other important applications for time-base circuits such as in radar and television indicators, in precise time measurements, and in time modulation.

5.2 General Features Of time-base Signa1

The typical form of a time-base voltage is as shown in Fig 5.1. Here it appears that the voltage, starting from some initial value, increases linearly with time to a maximum value, after which it returns again to its initial value. The time required for the return to the initial value is called the ***restoration time***, the ***return time***, or the ***fly back time***. Very "frequently the shape of the waveform during the restoration time and the restoration time itself are matters of no special consequence. In some cases, however, a restoration time is desired which is very short in comparison with the time occupied by the linear portion of the waveform. If it should happen that the restoration time is extremely short and that a new linear voltage is initiated at the instant the previous one is terminated, then the waveform will appear as in Fig 5.2. The output waveform is saw tooth waveform or ramp.

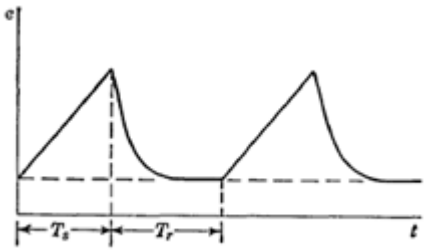


Fig 5.1 Typical form of a time-base voltage

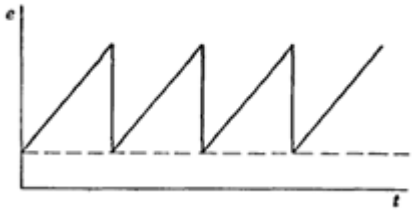


Fig 5.2 Waveform

We shall see that generators of time-base signals do not ordinarily provide sweep voltages which are precisely linear. Additionally a nominally linear sweep may be distorted in the course of transmission through a coupling network. The three most useful ways of

expressing the deviation from linearity, and the correlation between them, are given in the following.

The Slope or Sweep Speed Error (es):

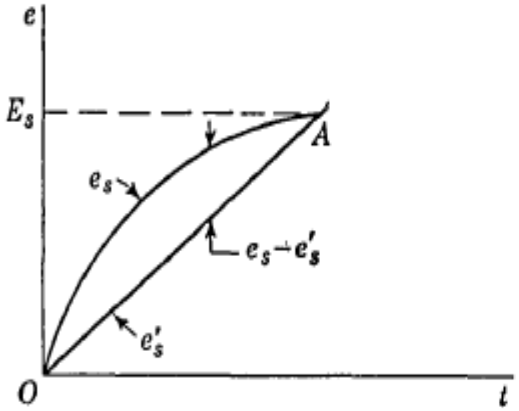
In the case of a general-purpose cathode-ray oscilloscope an important requirement of the sweep is that the sweep speed (i.e., the rate of change of sweep voltage with time) be constant. A reasonable definition of the deviation from linearity is

$$\epsilon_s \equiv \frac{\text{difference in slope at beginning and end of sweep}}{\text{initial value of slope}}$$

The Displacement Error (ed):

In connection with other timing applications a more important criterion of linearity is the maximum difference between the actual sweep voltage and linear sweep which passes through the beginning and end points of the actual sweep as in Fig 5.3. Here we may define

$$\epsilon_d \equiv \frac{(e_s - e'_s)_{\max}}{E_s}$$



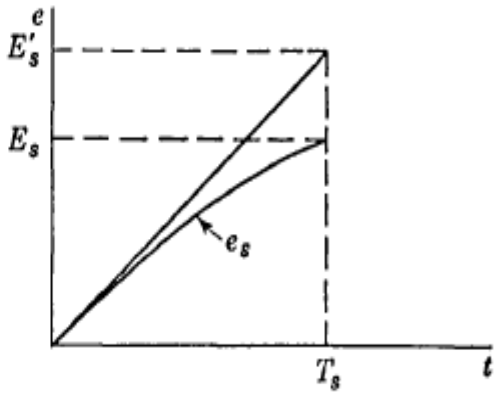


Fig 5.3 Displacement error *Transmission error*

The Transmission Error (et):

If a ramp voltage is transmitted through a high-pass *RC* network, the output falls away from the input, as indicated the ***transmission error*** is defined as the difference between the input and output divided by the input.

$$\epsilon_t = \frac{E_s' - E_s}{E_s'}$$

If the deviation from linearity is small so that the sweep voltage may be approximated by the sum of a linear and a quadratic term in *t*, then it can be shown from the above definitions that

$$\epsilon_d = \tfrac{1}{8}\epsilon_s = \tfrac{1}{4}\epsilon_t$$

5.3 Methods of generating time base waveforms

There are seven basic sweep circuits by which sweep linearity can be achieved. These are as follows

1.Exponential charging

A capacitor is charged through a resistor to a voltage which is small in comparison with supply voltage.

2.const current charging

A capacitor is charged with a constant current source.as it is charged with constant current,it is charged linearly.

3.Miller circuit

Integrator is used to convert,a step waveform in to ramp waveform.

4.Phantastron circuit

It is modified miller circuit which requries only pulse input to get ramp output.

5.Bootstrap circuit:

A constant current is obtained by maintaining nearly constant voltage across a fixed resistor in series with a capacitor.

6.Compensating network:

Compensated networks are added to improve the linearity of the bootstrap and miller time base circuits.

7.Inductor circuit:

Linear capacitor charging is achieved by introducing RLC series circuit.

Exponential sweep circuit

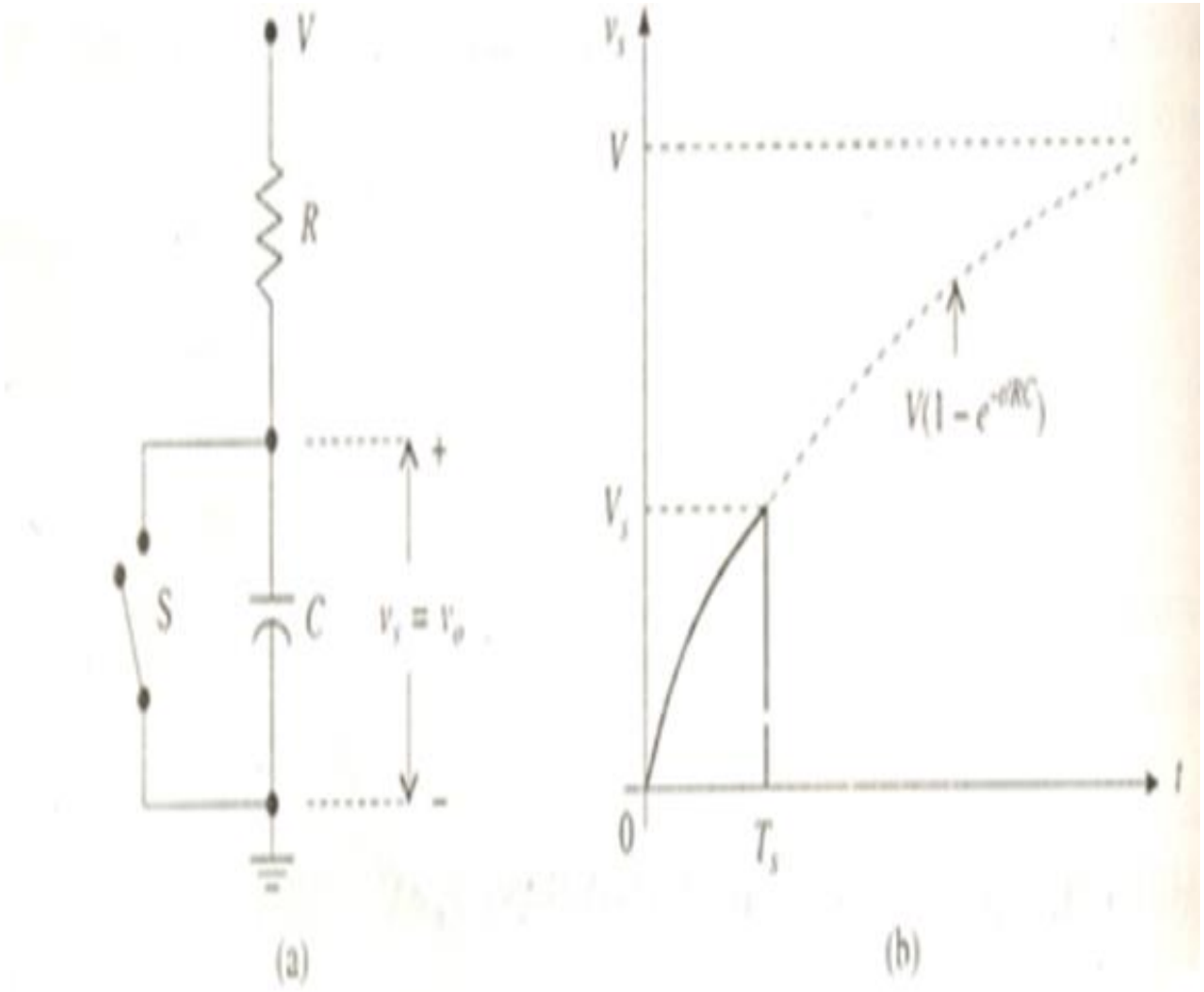


Fig 5.4(a) Charging a capacitor through a resistor from a fixed voltage & (b) the resultant exponential waveform across the capacitor

In exponential sweep circuit when the switch is closed the capacitor charges. When the switch is open the capacitor discharges and this can be shown in Fig 5.4 (a).The output waveform is saw tooth as shown in Fig 5.4 (b).

Derivation of es, et, ed:

Slope or sweep speed error, e_s

We know that for an exponential sweep circuit of Figure 7.3(a),

$$v_o(t) = V(1 - e^{-t/RC})$$

∴ Rate of change of output or slope is

$$\frac{dv_o}{dt} = 0 - V(e^{-t/RC})\left(\frac{-1}{RC}\right) = \frac{Ve^{-t/RC}}{RC}$$

$$\therefore \text{Slope error, } e_s = \frac{\left.\frac{dv_o}{dt}\right|_{t=0} - \left.\frac{dv_o}{dt}\right|_{t=T_s}}{\left.\frac{dv_o}{dt}\right|_{t=0}} = \frac{\frac{V}{RC} - \frac{Ve^{-T_s/RC}}{RC}}{\frac{V}{RC}}$$

$$= 1 - e^{-T_s/RC}$$

$$= 1 - \left(1 - \frac{T_s}{RC} + \left(\frac{-T_s}{RC}\right)^2 \frac{1}{2} + \ldots\right)$$

For small T_s, neglecting the second and higher order terms

$$e_s = \frac{T_s}{RC}$$

Also, $v_o = V(1 - e^{-t/RC})$

At $t = T_s$, $v_o = V_s$

$$\therefore \quad V_s = V(1 - e^{-T_s/RC}) = V\left[1 - \left(1 - \frac{T_s}{RC} + \left(-\frac{T_s}{RC}\right)^2 \frac{1}{2!} + \ldots\right)\right]$$

Neglecting the second and higher order terms

$$V_s = V\frac{T_s}{RC} \quad \text{or} \quad \frac{V_s}{V} = \frac{T_s}{RC} = e_s$$

The transmission error, e_t

From Figure 7.2(b),

$$v_s = V(1 - e^{-t/RC})$$

At $t = T_s$,

$$v_s = V_s = V(1 - e^{-T_s/RC})$$

$$= V\left[1 - \left(1 - \frac{T_s}{RC} + \left(-\frac{T_s}{RC}\right)^2 \frac{1}{2!} + \ldots\right)\right]$$

$$\therefore \quad V_s = V\left(\frac{T_s}{RC} - \frac{1}{2}\left(\frac{T_s}{RC}\right)^2\right)$$

The initial slope, $\left.\frac{dv_o}{dt}\right|_{t=0} = \frac{V}{RC}$

If the initial slope is maintained at $t = T_s$, $v_s = V_s' = T_s \times \frac{V}{RC}$

$$\therefore \quad e_t = \frac{V_s' - V_s}{V_s'} = \frac{\frac{VT_s}{RC} - \left(\frac{VT_s}{RC} - \frac{V}{2}\left(\frac{T_s}{RC}\right)^2\right)}{\frac{VT_s}{RC}} = \frac{T_s}{2RC} = \frac{e_s}{2}$$

Displacement error (ed):

At $t = \frac{T_s}{2}$ $\quad v_s = V(1 - e^{-T_s/2RC})$

$$= V\left[1 - \left\{1 - \frac{T_s}{2RC} + \left(-\frac{T_s}{2RC}\right)^2 \frac{1}{2!} + \ldots\right\}\right]$$

$$= V\left[\frac{T_s}{2RC} - \left(\frac{T_s}{RC}\right)^2 \frac{1}{8}\right]$$

At $t = T_s$, $\quad v_O = V_s$

$\therefore$ $\quad V_s = V(1 - e^{-T_s/RC})$

$$= V\left[1 - \left\{1 - \frac{T_s}{RC} + \left(-\frac{T_s}{RC}\right)^2 \frac{1}{2!} + \ldots\right\}\right]$$

$$= V\left[\frac{T_s}{RC} - \frac{1}{2}\left(\frac{T_s}{RC}\right)^2\right]$$

$\therefore$ The displacement error e_d is given by

$$e_d = \frac{(v_s - v_s')_{max}}{V_s} = \frac{V\left[\frac{T_s}{2RC} - \frac{1}{8}\frac{T_s^2}{(RC)^2}\right] - \frac{V}{2}\left[\frac{T_s}{RC} - \frac{T_s^2}{2(RC)^2}\right]}{V\left[\frac{T_s}{RC} - \left(\frac{T_s}{RC}\right)^2 \frac{1}{2}\right]}$$

$$= \frac{\frac{V}{2}\left[-\frac{T_s^2}{4(RC)^2} + \frac{T_s^2}{2(RC)^2}\right]}{V\left[\frac{T_s}{RC}\right]}$$

$$= \frac{1}{2}\left[\frac{\frac{1}{4}\left(\frac{T_s}{RC}\right)^2}{\frac{T_s}{RC}}\right] = \frac{1}{8}\frac{T_s}{RC} = \frac{e_s}{8}$$

$e_d = \frac{e_s}{8} = \frac{e_t}{4}$

UJT SWEEP CIRCUIT

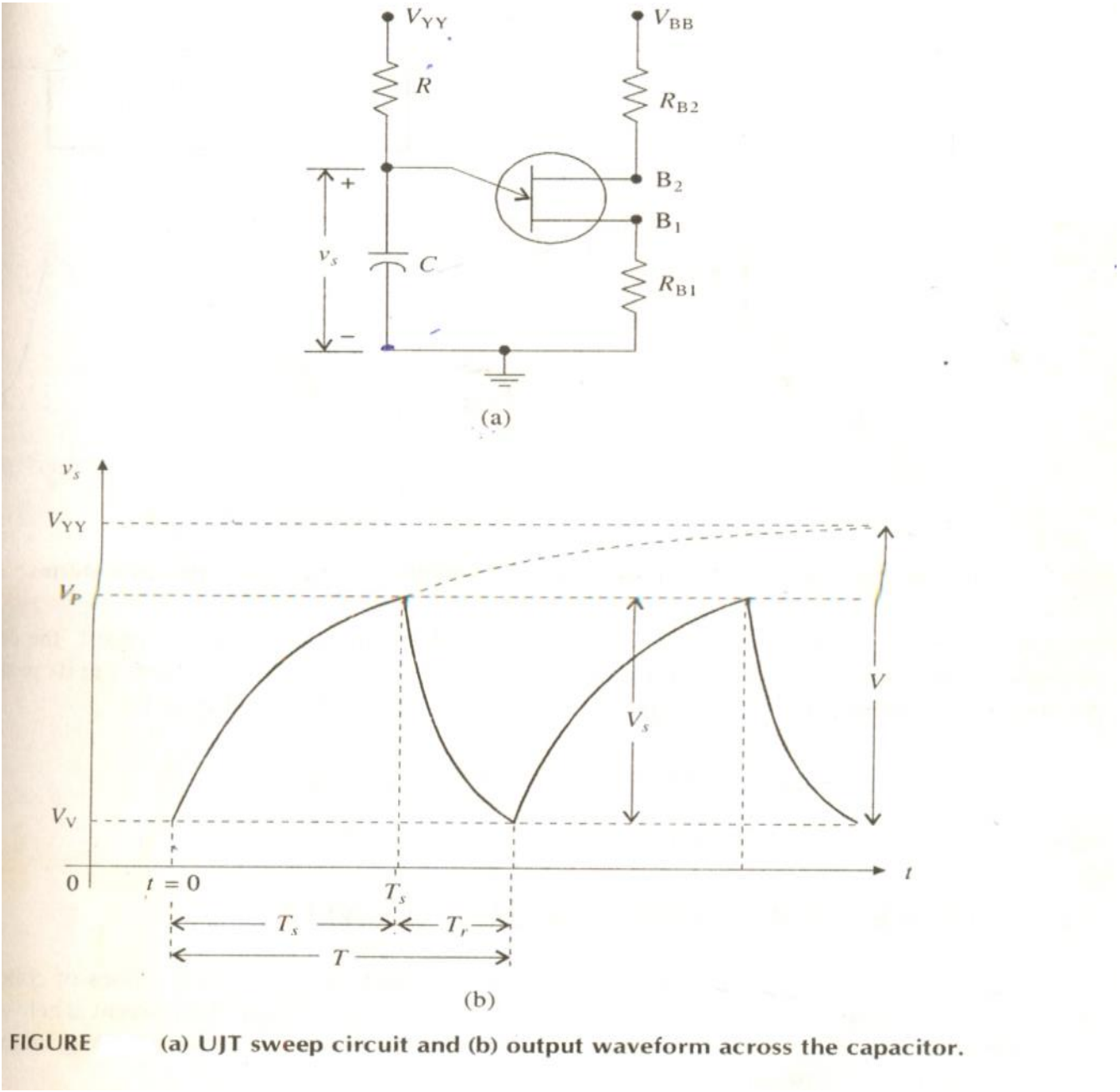


FIGURE (a) UJT sweep circuit and (b) output waveform across the capacitor.

Fig shows UJT sweep generator or relaxation oscillator. When UJT is in off condition capacitor charges to the peak voltage v_p when the capacitor voltage reaches to v_p UJT is in on condition so the capacitor discharges through the UJT and the output of this circuit is a saw tooth waveform.

Derivation for sweep time of UJT

For $0 < t < T_s$, $v_s = V_{YY} - (V_{YY} - V_V)\, e^{-t/RC}$

At $t = T_s$, $v_o = v_s = V_P$

$\therefore$ $V_P = V_{YY} - (V_{YY} - V_V)e^{-T_s/RC}$

i.e. $(V_{YY} - V_V)e^{-T_s/RC} = V_{YY} - V_P$

or $$e^{T_s/RC} = \frac{V_{YY} - V_V}{V_{YY} - V_P}$$

$\therefore$ $$T_s = RC \ln \frac{V_{YY} - V_V}{V_{YY} - V_P}$$

For good linearity, $V_s = V_P - V_V$ must be much smaller than $V = V_{YY} - V_V$. Since usually $V_P >> V_V$ and $V_{YY} >> V_V$, we require that $V_P >> V_{YY}$. Also, $V_{YY} >> V_{BB}$.

When V_V is very small,

$$e_s = \frac{T_s}{RC}, \quad e_t = \frac{T_s}{2RC} \quad \text{and} \quad e_d = \frac{T_s}{8RC}$$

5.4 Miller and Boot strap sweep circuit

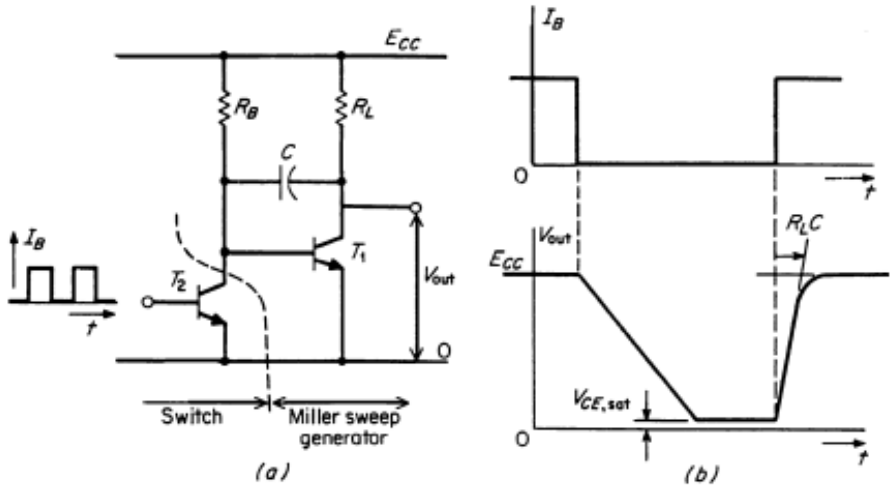


Fig 5.5 (a) Miller sweep circuit (b) input and output waveform

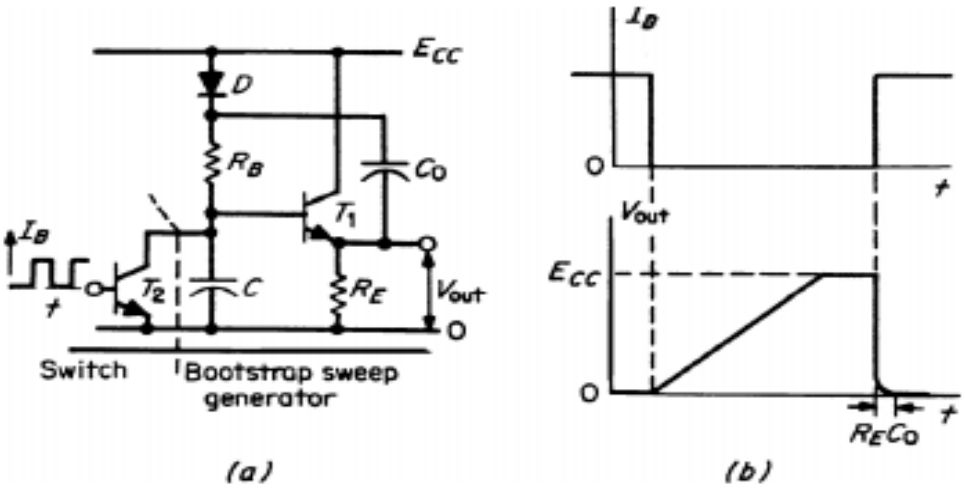


Fig 5.6(a) Bootstrap sweep circuit (b) input and output waveforms

Circuits delivering a linear voltage sweep fall into two categories,

5.5 Miller time base and bootstrap time base

A simple Miller circuit (Fig.5.5) comprises a capacitor C in a feedback loop around the amplifier formed by T1. Transistor T2 acts like a switch. When it is on, all the current flowing through the base resistor R_B is driven to ground, keeping T 1 blocked, since the voltage drop across T2
is lower than the normal base-to-emitter voltage of T1 . The output signal VCE of T1 is thereby clamped at the level of the power-supply voltage E cc, and the voltage drop across the capacitor C is approximately the same. When T2 is turned off, it drives T1 into the active region and causes collector current to flow through $R_{L.}$ The resulting voltage drop across R L is coupled capacitive to the base of T 1, tending to minimize the base current; i.e., the negative-feedback loop is closed. The collector-to-emitter voltage VCE of T 1 subsequently undergoes a linear voltage sweep downward, as illustrated in Fig 5.5 (b).
Fig 5.6(a) shows a typical bootstrap time-base circuit. It differs from the Miller circuit in that the capacitor C is not a part of the feedback loop. Instead the amplifier is replaced by an emitter-follower delivering an output signal V_{out} which reproduces the voltage drop across the capacitor. C is charged through resistor R_B from a floating voltage source formed by the capacitor C0 (C0 is large compared with C). First, we consider that the switch T_2 is on. Current then flows through the series combination formed by the diode D, the resistor $R_{B,}$ and the saturated transistor T_2 . The emitter follower T_1 is blocked since T 2 is saturated. Moreover, the capacitor C0 can charge through the path formed by the diode D and

the emitter resistor R_E. And the voltage drop across its terminals is equal to ECC . When T 2 is cut off, the current through R_B flows into the capacitor C, causing the voltage drop across its terminals to raise gradually, driving T1 into the active region

Because T1 is a unity-gain amplifier, V out is a replica of the voltage drop across C. Since C0 acts as a floating dc voltage source, diode D is reverse-biased immediately. The current flowing through R_B is supplied exclusively by C0. Since C0 >> C, the voltage across R B remains practically constant and equal to the voltage drop across C0 minus the base-to-emitter voltage of T 1. Considering that the base current of T1 represents only a small fraction of the total current flowing through RB , it is evident that the charging of capacitor C occurs under constant-current and that therefore a linear voltage ramp is obtained as long as the output voltage of T 1 is not clamped to the level of the power-supply voltage ECC.

The corresponding output waveforms are shown in Fig. 5.6 b. After T2 is switched on again, C discharges rapidly, causing Vout to drop, while the diode D again is forward-biased and the small charge lost by C0 is restored. In practice, C0 should be at least 100 times larger than C to ensure a quasi-constant voltage source.

5.6 Current time base generator

Transistor Q is used as a switch. An inductor L is connected in series with the transistor Q. A diode D with resistance Rd in series is connected across the inductor L.A rectangular waveform is applied at the base which is called gating waveform. The simple current time base generator circuit can be shown in Fig 5.7.

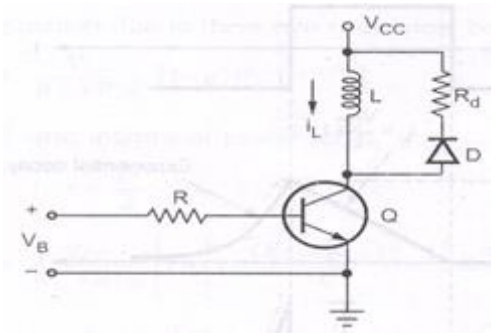


Fig5.7 Simple current time base generator

When transistor Q is on then neglecting the effect of saturation current I_L will be increased linearly with time. This increases continues till t=Ts where the sweep ends as the

gating waveform makes the transistor Q cut-off. As long as the current increases linearly with time, the diode is reverse biased act as open circuit.

But t=Ts when the sweep ends transistor Q is cut-off and diode becomes forward biased. The inductor current then continues to flow through the diode D and resistance Rd till it becomes zero. This current decay is exponential in nature. This decay current has time const Ť=L/Rd. At time t=Ts the inductor current attains max value and then start decaying exponentially.

The **gating waveform, inductor current waveform and the collector voltage** waveform are shown **in the Fig 5.8**

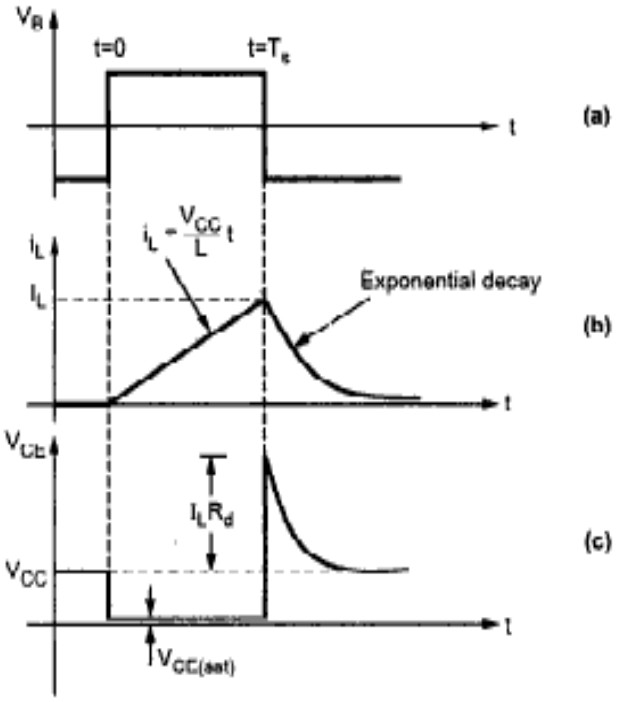


Fig5.8 Waveforms of simple current time base generator

$$i_L = \frac{Vcc}{R_L + R_{CS}}\left[1 - e^{-(R_L+R_{CS})t/L}\right]$$

$$i_L = \frac{Vcc}{R_L + R_{CS}}\left[1 - \left[1 - \frac{(R_L + R_{CS})t}{L} + \frac{(R_L + R_{CS})^2 t^2}{2L^2} - \cdots\right]\right]$$

$$i_L = \frac{Vcc}{R_L + R_{CS}}\left[\frac{(R_L + R_{CS})t}{L} - \frac{(R_L + R_{CS})^2 t^2}{2L^2} + \cdots\right]$$

$$i_L = \frac{Vcc}{R_L + R_{CS}} \cdot \frac{(R_L + R_{CS})t}{L}\left[1 - e^{-(R_L+R_{CS})t/L}\right]$$

$$i_L = \frac{Vcc}{R_L + R_{CS}}\left[1 - \frac{(R_L + R_{CS})t}{2L}\right]$$

$$i_L = \frac{Vcc\ t}{L}\left[1 - \frac{(R_L + R_{CS})t}{2L}\right]$$

From this equation it is clear that current departs feom a linear increase in time. Thus produces slope error.

$$e_S = \frac{\frac{di_L}{dt} \mid t = 0 - \frac{di_L}{dt} \mid t = T_S}{\frac{di_L}{dt} \mid t = 0}$$

$$i_L = \frac{Vcc}{R_L + R_{CS}}\left[1 - e^{-(R_L + R_{CS})t/L}\right]$$

$$\frac{di_L}{dt} = \frac{V_{CC}}{R_L + R_{CS}}\left(-e^{-(R_L + R_{CS})\,t/L}\right)\left[-\frac{(R_L + R_{CS})}{L}\right]$$

$$\frac{di_L}{dt} = \frac{V_{CC}}{L}\,e^{-(R_L + R_{CS})\,t/L}$$

$$\therefore \quad \left.\frac{di_L}{dt}\right|_{t=0} = \frac{V_{CC}}{L}$$

and $$\left.\frac{di_L}{dt}\right|_{t=T_s} = \frac{V_{CC}}{L}\,e^{-(R_L + R_{CS})\,T_s/L}$$

$$e_s = \frac{\frac{V_{CC}}{L} - \frac{V_{CC}}{L}\,e^{-(R_L + R_{CS})\,T_s/L}}{\frac{V_{CC}}{L}}$$

$$\therefore \quad e_s = 1 - e^{-(R_L + R_{CS})\,T_s/L}$$

$$\therefore \quad e_s = 1 - \left\{1 - \frac{(R_L + R_{CS})\,T_s}{L}\right\}$$

$$\therefore \quad e_s = \frac{(R_L + R_{CS})\,T_s}{L}$$

But $$\frac{T_s}{L} = \frac{I_L}{V_{CC}}$$

$$\therefore \quad \boxed{e_s = \frac{I_L\,(R_L + R_{CS})}{V_{CC}}}$$

5.7 Linearization using const current circuit

As inductor current increases, the drop across internal resistance increases. This reduces overall voltage across the inductor. The voltage across the inductor is given by L di/dt.so as voltage across the inductor decreases, the rate of change of current decreases. This produces nonlinearity in the waveform of current with respect to time.

To compensate for decrease in voltage across the inductor, it is necessary to apply trapezoidal voltage across the inductor.

Circuit used to generate trapezoidal voltage can be shown in Fig 5.9 (a) & (b)

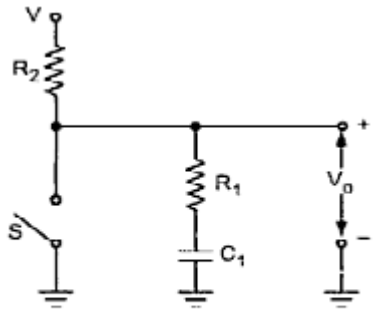


Fig 5.9(a)

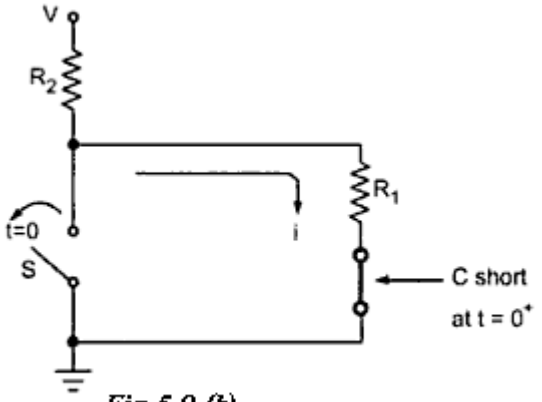


Fig 5.9 (b)

$I=V/R_1+R_2$ this is when t=0

At t=0+ capacitor start charging, so the voltage across the resistor R_1 decreases exponentially.

Output voltage = $V-iR_2-V_o=0$

$V_0=V-IR_2$

t>0 it is evident that the current decreases exponentially with time const $(R_1+R_2)C_1$

$$\therefore \quad V_o = \frac{VR_1}{R_1+R_2}\, e^{-t/(R_1+R_2)C_1} + V\left(1-e^{-t/(R_1+R_2)C_1}\right)$$

$$\therefore \quad V_o = \frac{VR_1}{R_1+R_2}\, e^{-t/(R_1+R_2)C_1} + V - V\, e^{-t/(R_1+R_2)C_1}$$

$$= V - V\, e^{-t/(R_1+R_2)C_1}\left(1-\frac{R_1}{R_1+R_2}\right)$$

$$\therefore \quad V_o = V - \frac{VR_2}{R_1+R_2}\, e^{-t/(R_1+R_2)C_1}$$

Using power series expansion of exponential term $\left(e^{-x} = 1 - x + \frac{x^2}{2} - \ldots.\right)$

We get, $$V_o = V - \frac{VR_2}{R_1+R_2}\left[1 - \frac{t}{(R_1+R_2)C_1} + \frac{t^2}{2(R_1+R_2)^2 C_1^2} - \ldots.\right]$$

$$= V\left[1-\frac{R_2}{R_1+R_2}\right] + \frac{VR_2\, t}{(R_1+R_2)^2 C_1} - \frac{VR_2\, t^2}{2(R_1+R_2)^3 C_1^2}$$

Neglect higher order terms.

$$\therefore \quad V_o = \frac{V R_1}{R_1+R_2} + \frac{V t R_2}{(R_1+R_2)^2 C_1}\left[1 - \frac{t}{2(R_1+R_2)C_1}\right]$$

As practically $R_2 >> R_1$ so neglecting R_1 from denominator,

$$V_o = \frac{VR_1}{R_2} + \frac{V t R_2}{R_2^2 C_1}\left[1 - \frac{t}{2 R_2 C_1}\right]$$

Due to large R_2, $\frac{t}{2R_2C_1} << 1$ so neglecting it,

$$\boxed{V_o = \frac{VR_1}{R_2} + \frac{V \cdot t}{R_2 C_1}}$$

This is the required trapezoidal waveform with a step of $\frac{V_{R1}}{R_2}$ at t = 0 and then linear increase with the slope $V / R_2 C_1$.

UNIT-6

SAMPLING GATES

6.1 Introduction

An ideal ***transmission gate*** is a circuit in which the output is an exact reproduction of an input waveform during a selected time interval and is zero otherwise. The time interval for transmission is selected by an externally impressed signal which is called the ***gating signal***

and is usually rectangular in wave shape. These gates are also referred to as ***time selection circuits***. In many applications, a less than ideal gate is entirely acceptable. It may be, for example, that the input signal consists essentially of a unidirectional pulse. In such a case a gate will be required to respond to an input signal of only one polarity. Furthermore, it is frequently required only that output pulses appear in response to an input pulse, and the preservation of the input wave shape is not critical. Under such circumstances it is not even required that the gate operate linearly during its transmission interval. It will be recognized that the *AND* circuit is just such a unidirectional gate. In the other applications on the other hand, a gate is required which will not only handle signal input excursions of both polarities, but additionally, linearity of transmission is of prime importance.

6.2 Basic Operating Principle of Sampling Gates

The basic principle of a linear gate is illustrated in Fig 6.1 (a) and (*b).* In switch *S* is normally open and is closed during the desired transmission interval. In Fig 6.1 (*b),* switch *S* is normally closed and is opened during the desired transmission interval. In practice, the switches will be replaced by diodes (thermionic or semiconductor), triodes, or multi grid tubes or transistor which will be biased in the conducting or non conducting direction as required. Ideally, the switches should have zero resistance when closed and infinite resistance when open, but, of course, in practice such will not be the case.

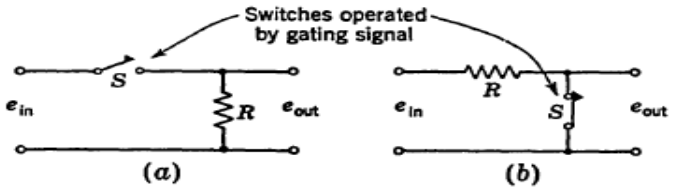


Fig 6.1 (a) & (b) Basic principle of a linear gate

Fig 6.1(a) is usually favored over the circuit of Fig 6.1(b). The reason for this preference is that in the non conducting direction a thermionic device may be counted on to have a nominally infinite resistance.

Hence in Fig 6.1(a) when *S* is open, the output will be zero as required. In Fig 6.1 (b) the output should be zero when *S* is closed. Since, however, the con-ducting or forward resistance *Rf* will range from several hundred to several thousand ohms, it will be necessary that *R* be quite large; that is, it is required that *R* » *Rf* in order for the shunting effect of the

switch to be effective. In this latter case, some small residual output will continue to persist. Also, during the transmission interval, the input and output will be separated by the large resistance *R.* If then there is some stray capacitance shunting the output, it will not be possible to transmit fast waveforms without deterioration of the waveform.

The advantage of the circuit of Fig 6.1(a) over the circuit of Fig 6.2 is, however, by no means clean-cut. In Fig 6.1 (a) we shall have to take into account the inevitable stray capacitance across *S,* which will permit some signal transmission when *S* is opened. Additionally, in Fig 6.1 (a) the signal is transmitted through *S,* and hence there will be attenuation and distortion introduced by the nonlinearity of the tubes used for this switch. In Fig 6.1 (b) the nonlinearity of the switch in its closed position has no effect on the transmission of the signal.

6.3 Unidirectional Sampling Gates

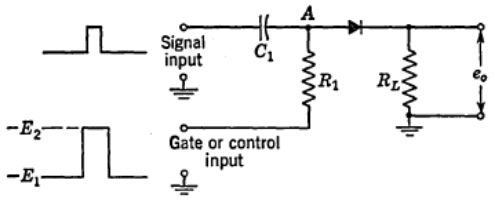


Fig 6.2 Unidirectional sampling gate

Semiconductor diodes do not have infinite back resistance and their forward resistance may lie in the range of only several ohms. When such diodes are employed, there is no generally apparent advantage in either circuit and the decision with respect to the circuit of choice must depend on the particular application. Fig 6.2 shows a Unidirectional Diode Gate. The gate signal (also called a *control* pulse, a *selector* pulse, or an *enabling* pulse) is a rectangular waveform which makes abrupt transitions between the negative levels -El and -*E2+*

When the gate voltage is -El, the diode is heavily back-biased and there will be no response at the output to an input signal unless the peak amplitude of the input signal is larger than the magnitude of the back-biasing voltage. (Actually, because of the capacitive coupling, the signal input voltage will appear at point *A* with an average value of zero.

Hence the peak positive excursion of the signal at *A*, with respect to zero voltage will be smaller than the peak-to-peak voltage of the input signal. For simplicity, we shall neglect this feature and consider simply that the input signal consists, say, of a very low duty-cycle pulse train, in which case this effect would be negligible.) When the gate rises to its higher level - *E 2,* a time-coincident signal input pulse may be transmitted to the output. The effect on the output of the level (- *E2)* attained by the gate waveform is illustrated in Fig 6.3. In Fig 6.3 (a), *-E2* = -5 volts and for a 10-volt input pulse a 5-volt output pulse appears.

Operation:

When the gate voltage is -El, the diode is heavily back-biased and there will be no response at the output to an input signal unless the peak amplitude of the input signal is larger than the magnitude of the back-biasing voltage. (Actually, because of the capacitive coupling, the signal input voltage will appear at point *A* with an average value of zero.

In this manner is often advantageous when the base line of the input signal has some noise signal superimposed. The level *-E2* may be adjusted so that only that part of the signal above the noise threshhold appears at the output. When used in this manner, the circuit is referred to as a threshhold gate. In Fig 6.3 (b), - *E2* = 0 and the entire input pulse is transmitted to the output, while in Fig 6.3 (c), *-E2* is positive and the signal appears superimposed on a ***pedestal***.

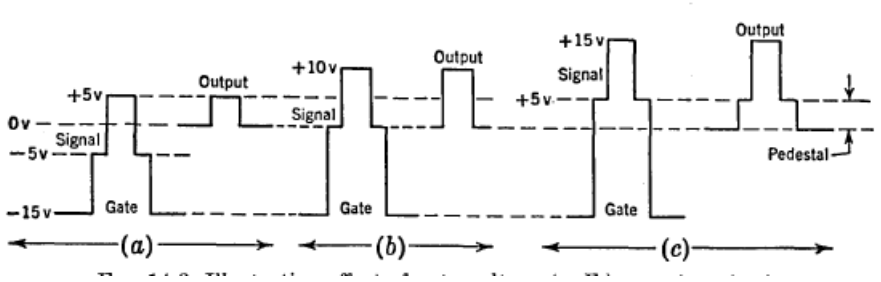


Fig 6.3 Gate waveforms

The waveforms of Fig 6.3 are unrealistic in that they have neglected the fact that the *Rl - C1* network constitutes an integrating network for the gate waveform. Hence, the gate voltage will not appear abruptly at *A* as required, but rather will rise exponentially with a time constant *Rl -Cl* and fall at a similar rate. Hence, this type of gate is not particularly suitable for selecting a portion of a continuous waveform. If, however, the signal is a pulse whose duration is reasonably smaller than the gate width, the result may be entirely satisfactory.

The advantages of this gate are the following:

(1) It is extremely simple.

(2) There is very little time delay through the gate since the input is coupled directly to the output through Cl and the diode.

(3) The gate draws no current in its quiescent condition (i.e., no "stand-by" current). This feature becomes very important in a system requiring many gates. In this respect also, the present gate should be compared with the *AND* gate which will accomplish the same general result as the present gate but which does draw stand-by current.

(4) The gate is easily extended into a multi-input *OR* circuit with an *INHIBITOR* terminal.

The disadvantages of the gate are the following:

(1) There will be interactions between the signal source and control-voltage source.

(2) The gate is of limited use because of the slow rise of this control voltagelower (negative) level -*Ell* tube T_l is driven below cutoff and *T2* then operates as an amplifier.

Other Forms of the Unidirectional Diode Gate

The unidirectional diode gate may be adapted to accept more than one signal input, as in Fig 6.4. Here two signal inputs $es_1$and $e\ s_2$ are indicated but, of course, more than two may be used.

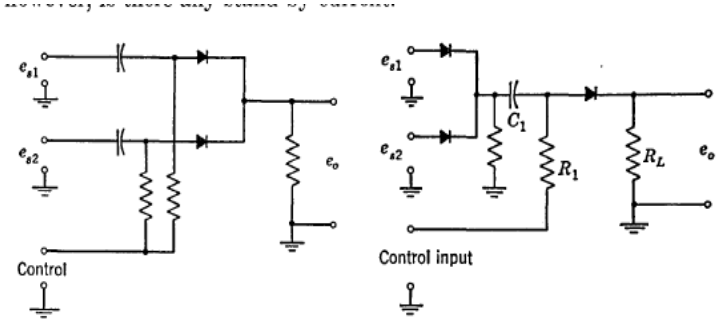


Fig 6.4 unidirectional sampling gate using multiple inputs

6.4 Bidirectional Sampling Gate using Transistor

The Fig 6.5 shows a linear bidirectional sampling gate using transistors. As shown in Fig 6.5, the signal voltage Vs and the gate or control voltage Vc are applied through summing resistors R1 and R2 to the base of a transistor. The gate signal is a pulse waveform having levels V1 and V2 and duration tp equal to the required transmission of duration.

When the gate voltage is at its lower level VI ', the transistor is biased well below the cutoff. Hence there is no conduction and transmission of input signal at the output. However when the gate voltage is at its higher level V_2, the transistor is biased well above the cut-off to drive it in the active region. Since transistor in the active region, input signal is readily sampled for the duration of the gate pulse, and it appears in an amplified form at the output. Thus, this gate can handle the excursion of the input signal both positive and negative directions.

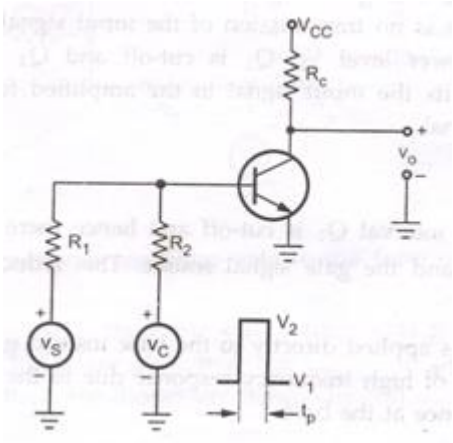


Fig 6.5 Bidirectional sampling gate using transistor

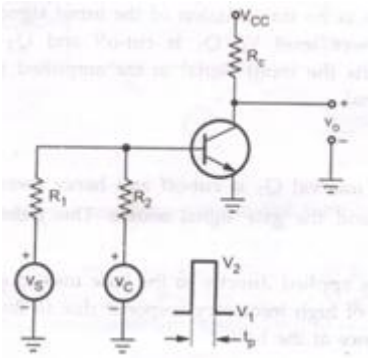


Fig 6.6 Bidirectional Diode Sampling Gate

Fig 6.6 shows bidirectional diode sampling gate using diode instead of transistors. Such diode gates have following advantages

- They ensures the linearity of operation and
- Ease of adjustment to get zero pedestals

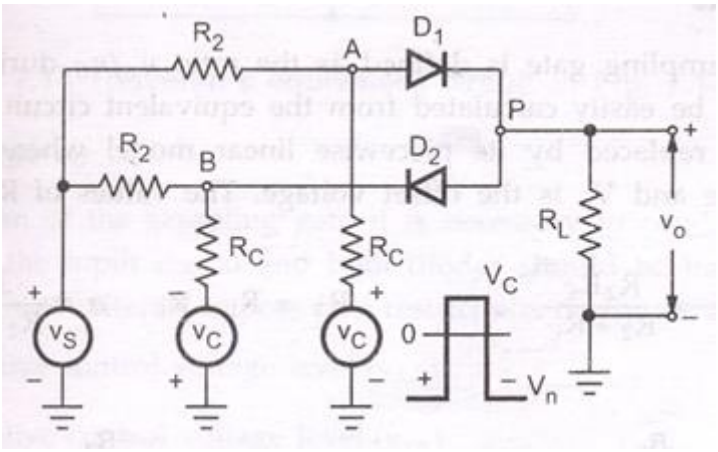


Fig 6.7 Bidirectional sampling gate using diodes

As shown in the Fig 6.7 there are two symmetrical gate signals +Vc and-Vc when the gate voltage levels are such that the voltage at point A is negative and the voltage at point B is positive, the diodes are no conducting and there is no transmission signal Vs. When the gate signal voltages are such that the voltage at a point A is positive and the voltage at point B is negative. Both diodes conduct.

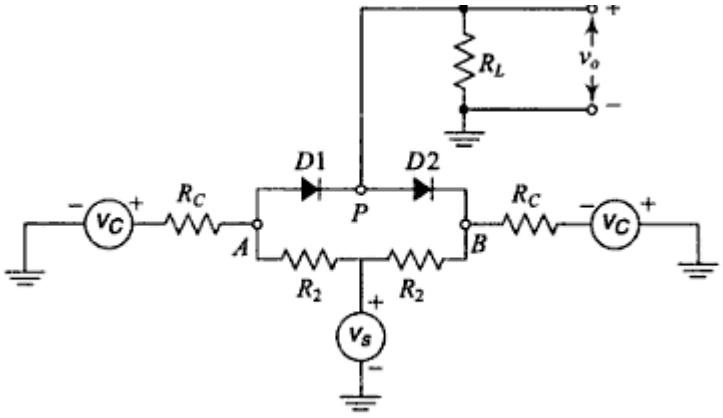


Fig 6.8 Bidirectional sampling gate using diodes in the form of a bridge

Gain of Sampling Gate

The gain of the sampling gate is defined as the ratio v o/vs during the transmission interval. The gain can be easily calculated from the circuit. Here, the diodes are replaced by its piecewise linear model where R, is forward resistance of the diode and Vr is cut-in voltage.

$$R_1 \equiv \frac{R_2 R_C}{R_2 + R_C}$$
$$R_3 \equiv R_1 + R_f$$
$$\alpha \equiv \frac{R_C}{R_2 + R_C}$$

Control voltage v_C

For proper operation of the sampling gate it is necessary to conduct both the diodes over the full range of the input signal and both diodes should be back biased when no sampling takes place. These criteria's impose two restrictions on the control voltage levels:

Minimum positive control voltage level (v_{Cp})

Minimum negative control voltage level (v_{Cn})

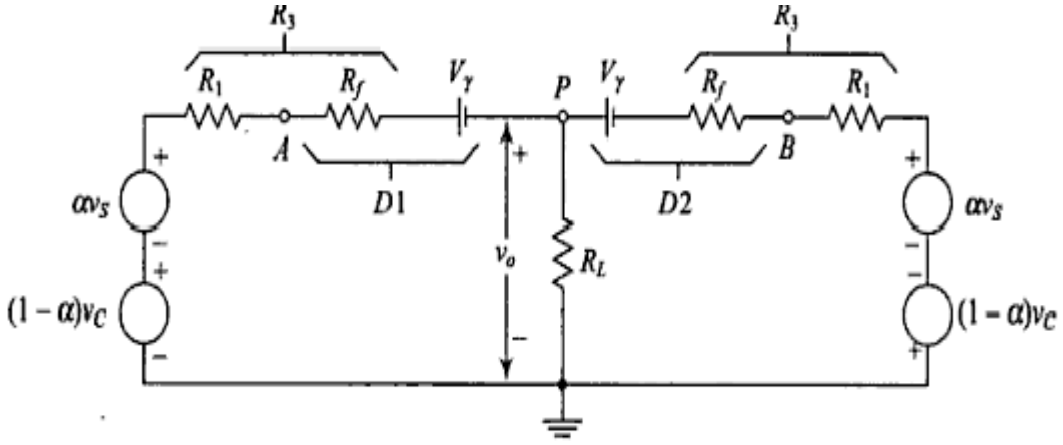


Fig 6.9 an equivalent circuit for Bidirectional sampling gate of fig 6.8

From the equivalent circuit of gate (Fig 6.9) it can be observed that as signal voltage goes minimum value the forward bias of diode D2 decreases. To maintain conduction of diode D2, the forward bias should not reach to zero. So the min control voltage required is as shown below

$$v_0 = -\propto V_S - (1-\propto)V_C$$
$$v_0 = [\propto V_S + (1-\propto)V_C]\frac{R_L}{R_L + R_3}$$

Equating two equations for we get,

$$[\propto V_S + (1-\propto)V_C]\frac{R_L}{R_L + R_3} = -\propto V_S - (1-\propto)V_C$$

Which we find

$$V_C = \frac{R_C}{R_2}\frac{R_3}{R_3 + 2R_L} V_S = V_{CP(min)}$$

6.5 Four Diode Sampling Gate

Some of the disadvantages of the two-diode sampling gate are:

1. Its gain is low
2. It is sensitive to control voltage imbalance
3. There is a possibility that (V_n)min
4. There may be appreciable leakage through the diode capacitance

The four-diode sampling gate shown in Fig 6.10 improves these features. This is obtained by adding two more diodes to the two-diode sampling gate. Two balanced voltages +V and –V are also required.

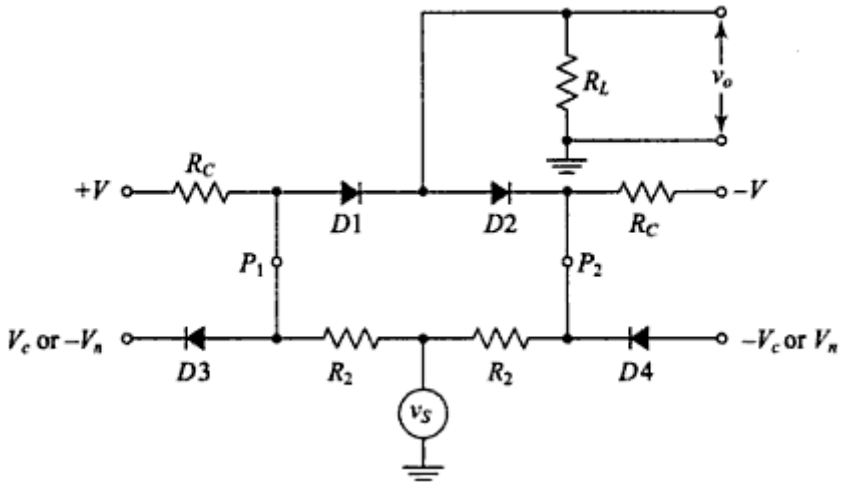


Fig 6.10 A four diode gate

When the control voltages are V_n and $-V_n$, the diodes D4 and D3 conduct and the points P2 and P1 are clamped to these voltages. So, diodes D1 and D2 are reverse biased. Under these circumstances, the output is zero.

Let us now compute the gain A and the required minimum values of V, V_c , and V_n .

During transmission,diodes D3 and D4 are OFF and the circuit of Fig 6.10 is identical

to the circuit of Fig 6.7 except that the voltages V_c and $-V_c$ are replaced by +V and –V respectively. Hence the gain of this circuit is the same as the gain of the gate of Fig 6.7 and is given by

$$A = \frac{R_C}{R_C + R_2} \frac{R_L}{R_L + (R_3/2)}$$

Also, the V_{min} of this circuit is the same as (V_c) min of the gate of Fig 6.7 and is given by

$$V_{min} = \frac{R_C}{R_2} \frac{R_3}{R_3 + 2R_L} V_S$$

The voltage (V_c) min is computed as follows. Assuming that $R_f \ll R_L$, for a positive going signal of amplitude V_s, the voltage at point P1 is the same as the output voltage v_0 given by AV_S where A is the circuit gain. If the diode D3 is to continue to be reverse biased, V_c must be at least equal to the voltage at P1. Hence

$$(V_C)_{min} = AV_S$$

The voltage V_n must be selected not only to keep the transmission diodes D1 and D2 reverse biased but also to keep the clamp diodes D3 and D4 conducting in the presence of the signal V_s by applying superposition theorem is

$$(V_n)_{min} = V_S \frac{R_C}{R_C + R_2} - V \frac{R_2}{R_2 + R_C}$$

6.6 Reduction of Pedestal in Gate Circuits

We have seen bidirectional transistorized sampling gates and observed the output waveforms of such sampling gates. Now we find the existence of pedestal in the waveform. This is illustrated in Fig 6.12.

Such pedestal can be largely suppressed by the symmetrical arrangement shown in Fig 6.11. Here, for simplicity, the gating and input signal voltages are shown directly in series. A pair of transistor is used and the bases of transistors are driven by the gating signal of opposite polarity. During no sampling time, Q2 draws current and Q1 does not. The bias voltages -V_{BB1} and -V_{BB2} and the gate signal amplitude are adjusted so that the two transistor currents are identical.

If the gate voltage has finite rise time then the circuit shown in Fig. 6.11 does not completely solve the problem of pedestal. This is illustrated in Fig. 6.12. It is assumed that the gate pulse is large compared with the active region base-voltage range, so that each transistor, when it is not conducting is biased far below cut-off. Then when the gate appears, Q2 will be driven to cut-off before Ql starts to conduct. On the other the end of the gate, Ql will be cut-off before Q2 starts to conduct. As a result, voltage spikes appear in the output. These spikes may not be objectionable if the gate waveform from rise gate waveform from rise time is small in comparison with the gate duration.

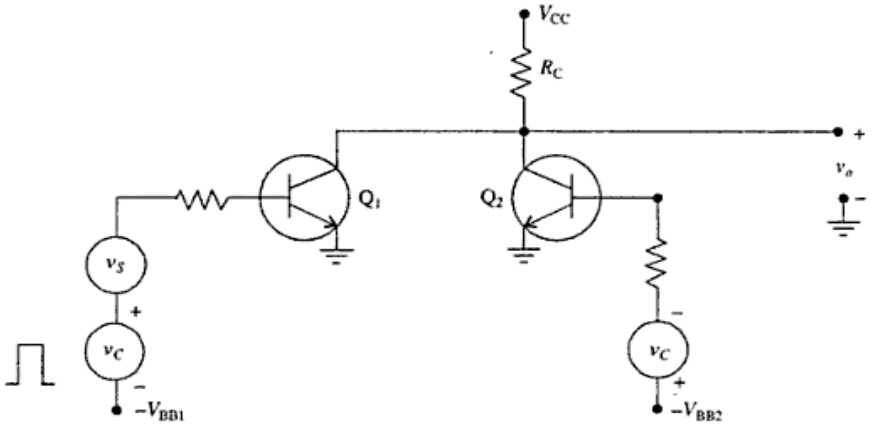


Fig 6.11 a sampling gate with provision to cancel the pedestal

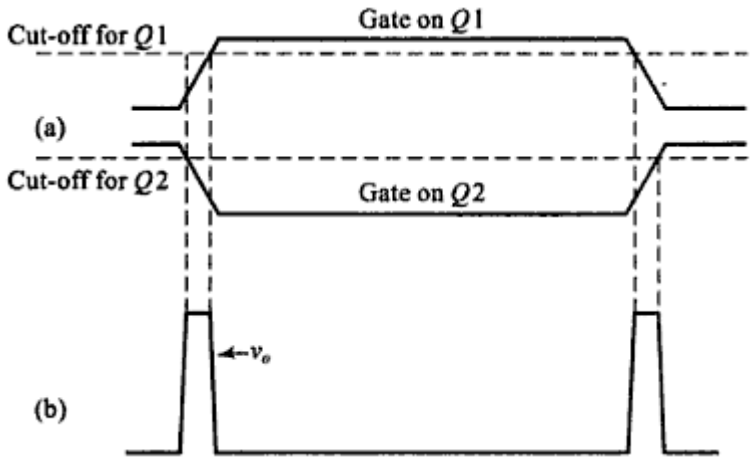


Fig 6.12(a) the gating waveforms of Fig 6.11drawn with non-zero rise time and (b)Spikes which may occur in the output of Fig 6.11 due to the gating waveform with non-zero rise time

1. The circuit shown in Fig 6.11 has following disadvantages:
2. If the gating waveforms have finite rise and fall times, voltage spikes appear at the
   output.
3. The power required by the circuit is more, since there is a continuous flow of current through Rc
4. The circuit requires two biasing voltages - V_{BB1} and - V_{BB2}, and two gating signals
   with opposite polarities.

6.7 Six Diode Gate

Fig 6.13 shows six-diode sampling gate. When the control voltages are V_n and $-V_n$, the diodes D6 and D5 conduct and the points P2 and P1 are clamped to these levels. Hence D4 and D3 are back biased and no signal trnsmission takes place. In the six-diode gate. The control signals need not be balanced. When the control signals are at levels V_c and $-V_c$, the diodes D5 and D6 are OFF and the six-diode gate becomes equivalent to the four-diode gate. The only change is that the control voltages V_c and $-V_c$ are replaced by the fixed voltages V and –V. the signal transmission takes place. Hence the minimum value of V, asssuming that $R_f \ll R_L \; or \; R_C$, is given by

$$V_{min} = V_S\left(2 + \frac{R_C}{R_L}\right)$$

$$V_{min} = V_S\left(2 + \frac{R_C}{R_L}\right)\left(1 + \frac{R}{4R_f}\right)$$

From Fig 6.13 we see that if the clamping diodes D_5 and D_6 are to remain reverse biased for signal amplitude V_s, then V_c must be at least equal to $(V_c)_{min} = V_s$. On the other hand, if the points P_1 and P_2 are clamped at voltage V_n, then none of the transmission diodes will conduct until V_s exceeds V_n. hence the minimum required value of V_n is $(V_n)_{min} = V_s$.

$$(V_c)_{min} = (V_n)_{min} = V_s$$

Again if R_C and $R_L >> R_f$ and R, the gain will be very close to unity, i.e. A ≈1.

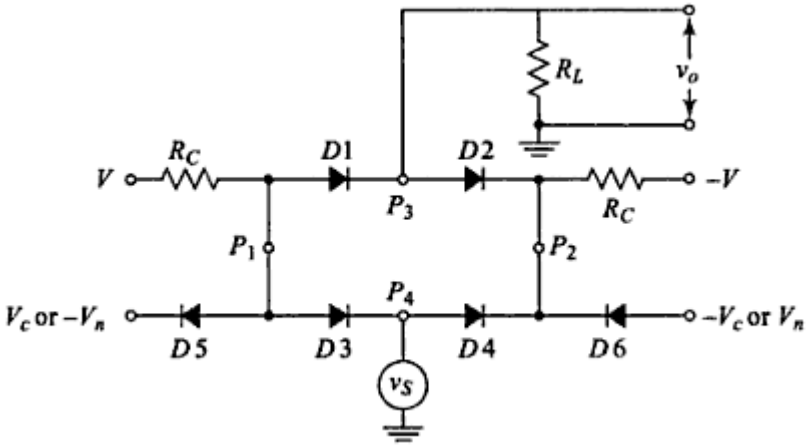


Fig 6.13 Six diode gate

6.8 Applications of Sampling Gates

The important applications of sampling gates are:

1. Multiplexers
2. Sample and hold circuits
3. Digital to analog converters
4. Chopper stabilized amplifiers
5. Sampling scopes

One of the application of sampling gate is it is used in chopper amplifier.

Chopper Stabilized Amplifier

Suppose it is required to amplify a small signal (say of the order of mill volts) and the signal v(t) is one in which dv / dt is very small. Such signal cannot be amplified using

ac amplifier because the required coupling capacitors will be impractically large. If we

use

dc amplifier for the amplification, we would not be able to distinguish between a change in output voltage as the result of a change in input voltage or as the result of a drift in some active device or component. In such cases the solution is to use chopper amplifier.

The Fig shows the chopper stabilized amplifier. The input signal is a low frequency signal and it is shown in Fig. 6.15 (a). The switch Sl in the amplifier circuit being driven so that it is alternately open and closed. As a result, the signal Vi at amplifier input will appear as in Fig. 6.15 (b). When Sl is open Vi = v, and when S1 closed Vi = O. It can be" seen that the Vi is a chopped version of the waveform *v*, hence the circuit consisting of R and S_1 is called a chopper.

The frequency of operation-of switch (chopping frequency) is very large in comparison

with the frequency of the signal v. Therefore, no appreciable change takes place in v during the interval when Sl is open. Accordingly, it is possible to describe the waveform Vi as a square wave of amplitude proportional to v and having an average value (shown by dashed line) that is also proportional to the signal v.

The low frequency cut-off of ac amplifier is such that it passes high frequency square wave signal but blocks the low frequency input signal. As a result, we get only modulated waveform' at .the output as shown in Fig. 6.15 (c). Because of this process of

modulation, the chopper is often called a modulator.

The capacitor C and switch S2 constitutes a recovery circuit at the output. 'The switch S2, closes and opens in synchronism with S1.. Thus, during the interval T1' the negative extremity of v_A is restored to zero, whereas during T2 the positive extremity is restored to

zero as a result, the output voltage Vo takes the form of signal Vi. Now we can get the amplified replica of the original signal by passing signal v_o through a low-pass filter with

cut-off frequency such that it rejects the square and transmits the signal frequency. The combination of the capacitor C, the switch S2 and the filter constitutes a synchronous demodulator

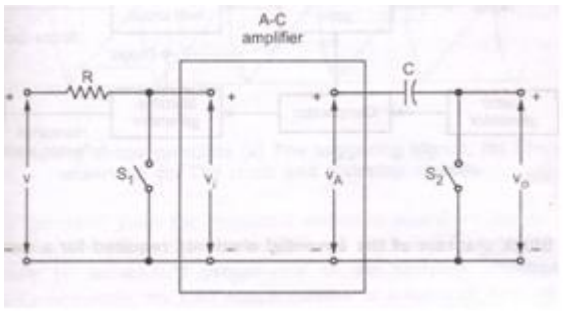


Fig 6.14 chopper stabilized amplifier

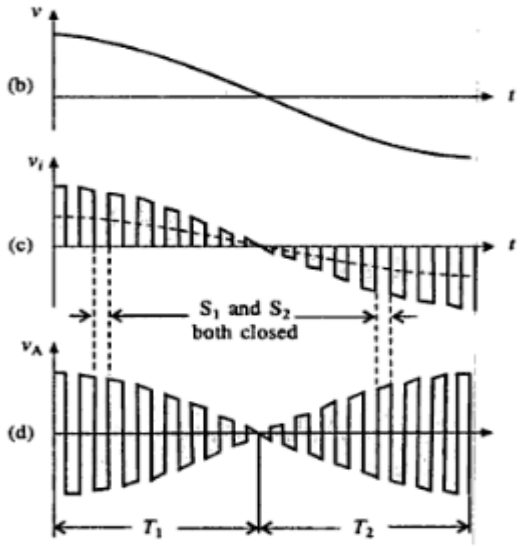


Fig 6.15(a) input signal (b) chopped signal (c) signal modulated square waveform

Sampling Scope

Sampling scope is another important application of sampling gate. It consists of sequence of samples of the input waveform, each sample taken at a time progressively delayed with respect to some reference point in the waveform.

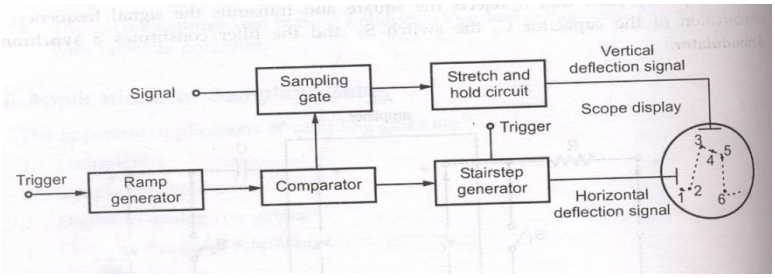


Fig 6.16 sampling scope block diagram

The Fig. 6.16 shows the block diagram of essential elements required for a sampling scope display. We assume that a train of triggers shown in Fig. 6.17 (a) is available and we

have to display the pulse train shown in Fig. 6.17 (b). As shown in Fig. 6.17 (a), a time of

occurrence of a train of triggers precedes the pulses shown in Fig 6.17 (b). The Fig 6.17 (c) shows the stair step and ramp signals. These are applied to a comparator. The stair step

serves' as the reference voltage, and in each cycle, whenever the ramp attains the stair step .

level, the comparator gives a pulse output which is used as the gate signal of the sampling

gate. At each such gate signal, the sampling gate gives the sample of the signal at it's output. The sample of input signal has duration equal to the width of the gate pulse The width of the gate signal is kept so short that during its interval no sensible change takes place in the input signal. Thus the gate output, at each gate signal, is a voltage equal

to the signal voltage at the time of sampling. The sampled points are marked as 1,2,3 on the waveform shown in Fig 6.17 (b). It is important to note that the samples are taken at a time which is progressively delayed by equal increments. The amplitude of the sampled signal is determined by the magnitude of the input signal at the sampling time. The stretch and hold circuit is used to hold the current sampled signal amplitude till then occurrence of the next sample. The holding operation may be performed by using the gate output to charge a capacitor through a diode to the peak value of the sample in a manner that when the sample is completed the capacitor holds its charge. If sampled

signal is insufficient to charge the capacitor within the small interval, the sampled signal is
amplified before applied to hold circuit.

The stair step generator gives the horizontal deflection signal for the scope. Thus the CRT spot moves horizontally across the screen and at each new position, the spot is deflected
vertically by an amount proportional to the sampled amplitude and it is displayed there. Consequently, the CRT screen consists of a series of dots which trace out the form of the original signal, as shown in Fig 6.17. The waveform shown in Fig 6.17 is not exactly represents the original signal, but if samples (dots) are spaced sufficiently closed we can observe quite precise original waveform on the CRT screen.

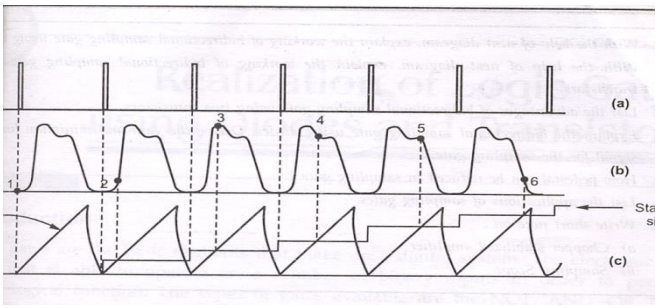


Fig 6.17 waveforms

UNIT-7

SYNCHRONIZATION AND FREQUENCY DIVISION

7.1 Introduction

A pulse or digital system may involve several different basic waveform generators. Such a system may require that these generators run synchronously, that is, in step with one another, so that each generator arrives at some reference point in its cycle at the same time. The frequency stability of waveform generators is never adequate to ensure synchronism

Even a very small frequency difference between generators will eventually causes the accumulation of a large error. In many pulse systems it is required that the individual generators be synchronized but be permitted to operate at different frequencies. We may require, say, that one generator complete exactly some integral number of cycles while a second generator executes only one cycle. Such a situation is described as synchronization with frequency division. In this unit we will discuss the mechanism of synchronization on a one to one basis and also synchronization with frequency division. The two processes are basically so nearly alike that no clear-cut distinction will be drawn between them.

The counting circuits may, of course, be used for frequency division. These counting circuits, with the exception of the storage counters, do not depend for their operation on the regularity of recurrence of the input waveform. If, say, the input signal consists of pulses, the counters will divide correctly, independently of whether the pulses occur regularly or in a random fashion. In the present unit, however, we contemplate only the case of an input waveform of a nominally fixed recurrence rate. This feature, as we shall see, permits considerable economy in the circuits which may be used to achieve division

7.2 Pulse Synchronization of Relaxation Devices

The term" relaxation circuit" is applied to any circuit in which a timing interval is established through the gradual charging of a capacitor, the timing interval being terminated by a relatively abrupt discharge (relaxation) of the capacitor.

The mechanism of synchronization and frequency division is basically the same for all of these relaxation devices. In the mono stable form, the matter of synchronization (1: 1

division) to a pulse-type waveform is a trivial one. The circuit normally remains in a quiescent condition and awaits the arrival of a triggering pulse to initiate a single cycle of operation. It is only necessary that the interval between triggers be larger than the timing interval and recovery period combined. The important features of pulse synchronization of an astable relaxation device may be exposed by examining the mechanism in connection with any of the circuits mentioned above.

UJT SWEEP CIRCUIT

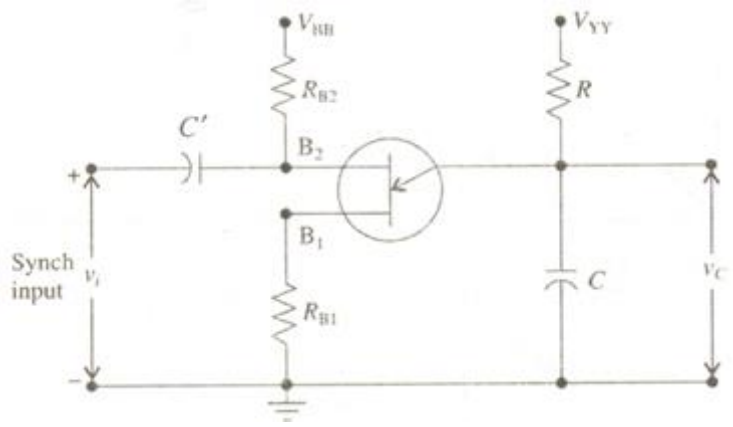


Fig 7.1 a seep generator with synchronization signal

Let us select the UJT sweep generator for examination since it is a slightly simpler circuit than the others. A UJT sweep generator is as shown in Fig 7.1. *In* the absence of synchronizing pulses the capacitor stop charging when the voltage $V_{c,}$ reaches the peak V_p of the UJT. There after the capacitor discharges abruptly through V_v the negative resistance device UJT. When the capacitor voltage Vc falls to the valley voltage Vv the resistance device, UJT goes OFF and the capacitor begins to recharge. When synchronization pulse is applied.

In order that synchronization may result, it is necessary that each pulse shall occur at a time when it may serve to terminate the cycle *prematurely.* This requirement means that the interval between pulses, T_p, must be *less* than the natural period, *To,* of the sweep generator. Additionally, even if the requirement $T_p < T_o$ is met, synchronization cannot result unless the pulse amplitude is at least large enough to bridge the $Tp > To$. Synchronization of each cycle does not occur. The pulses do serve to establish that four sweep cycles shall occur during the

course of three pulse periods, but synchronization of this type is normally of no: value. In Fig. we have the seen where *T p* is less than *To* as required, but the pulse amplitude is too small and again synchronization does not result.

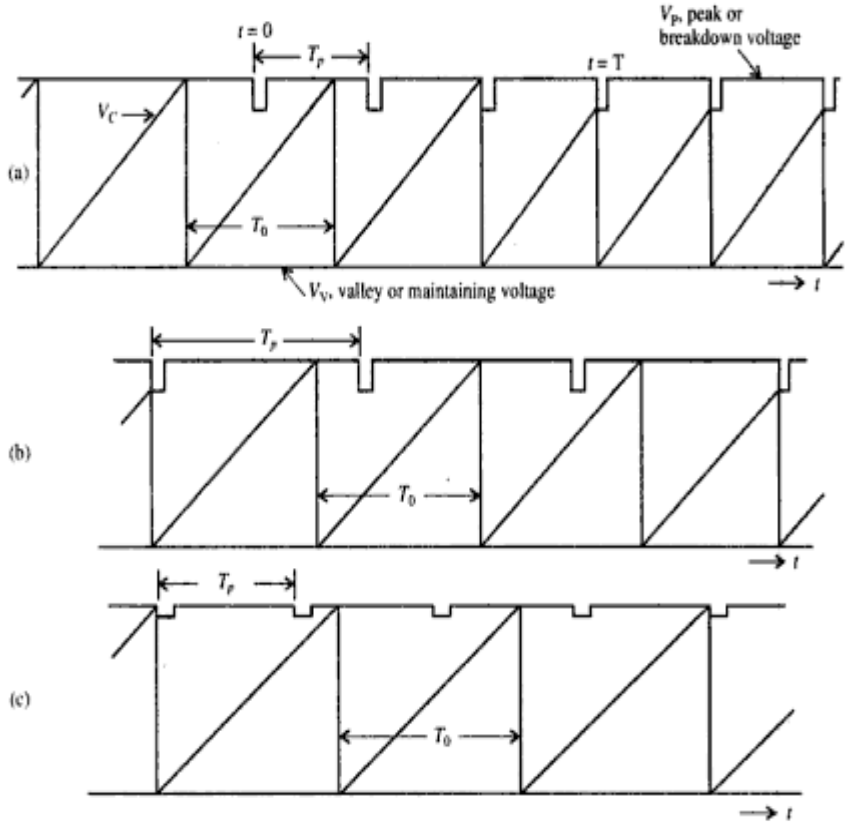


Fig 7.2 (a) T p < To: synchronization results, (b) T p > To: no synchronization results and (c) T p < To but amplitude of synch pulse is small, hence no synchronization results

7.3 Frequency Division in the UJT Sweep

In Fig 7.1 we have a case in which *T p < To* but in which the pulse amplitude is too small to permit each pulse to terminate a cycle. The sweep cycles are therefore terminated only by the alternate pulse marked "2" in the figure. The pulses marked" 1" would be required to have an amplitude should be large and it is at least equal to E .where E is the amplitude of the sweep after synchronization is less than the unsynchronized amplitude *E.* Suppose, referring again to Fig 7.3, that *T p* is progressively decreased. Eventually a point would be reached where even the alternate pulses

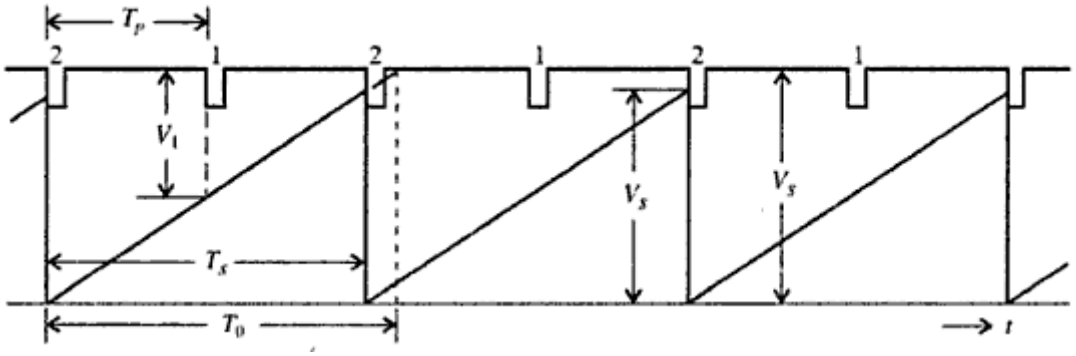


Fig 7.3 frequency division by a factor of 2 in a sweep generator

7.4 Astable Multivibrator

The astable multivibrator in Fig 7.4 may be synchronized or used as a divider by applying positive or negative triggering pulses to either transistor or to both transistors simultaneously. These pulses may be applied either to the base or to the collector. If, for example, positive pulses are applied to the base of the transistor Q1 it is seen that the cycle would have terminated naturally at t=T0 since at that instant the base voltage equals the cut in voltage Vr.as a result, the cycles gets terminated prematurely at the sixth pulse. Thus the generator voltage completes one full cycle for six cycles of the triggering pulses. The astable multivibrator therefore functions as a divider, with a division factor of

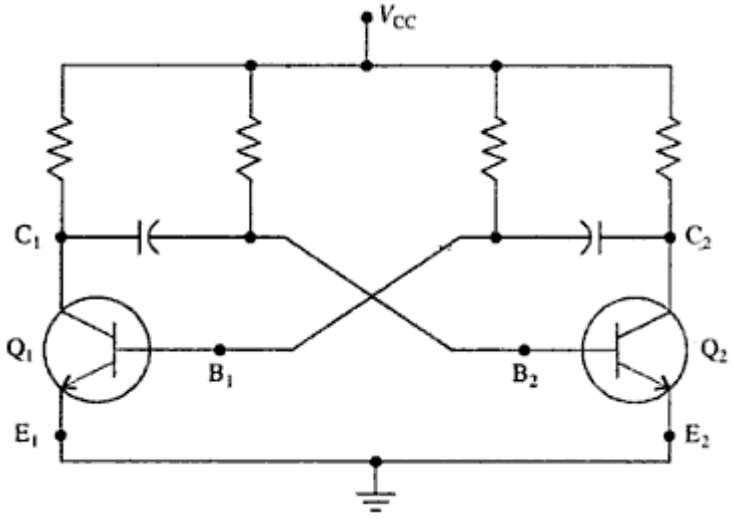


Fig 7.4 a astable multivibrator

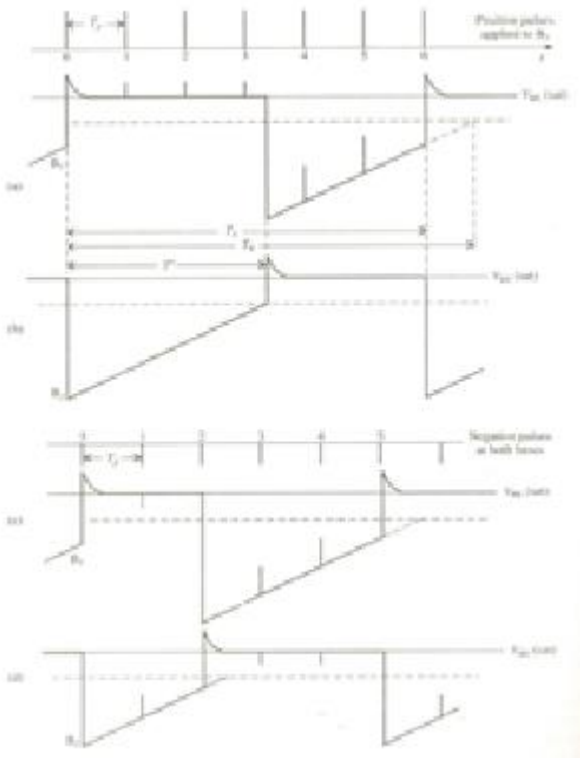


Fig 7.5 (a) and (b) base waveforms for division by 6 through the application of positive pulses to one base (c) and (d) base waveforms for division by 5 through the application of negative pulses to both bases

7.5 MONOSTABLE RELAXATION CIRCUIT

Fig shows the monostable multivibrator. It can be used as a divider by applying pulses at B1 or C1.depending on the polarity. Fig a and b shows the waveforms indicating the voltage at B2.when positive pulses are applied at B1 through a small capacitance from a low impendence source, the input pulses terminates the timing cycle prematurely as shown in Fig 7.6.

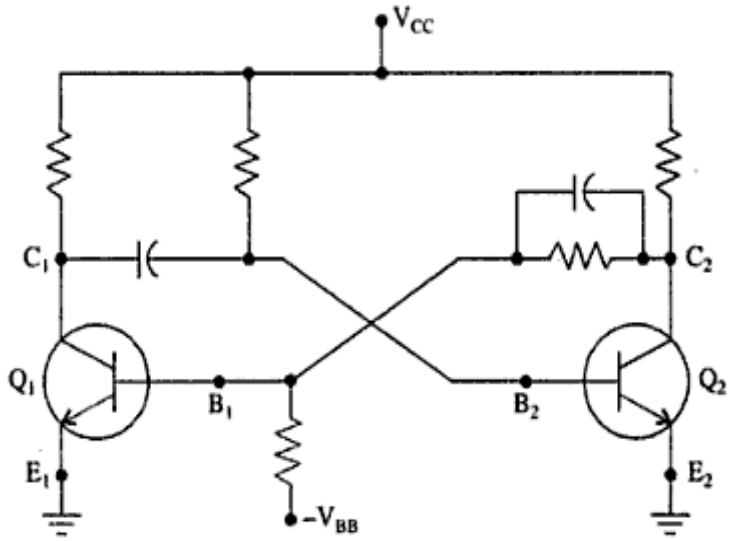


Fig 7.6 a monostable multivibrator

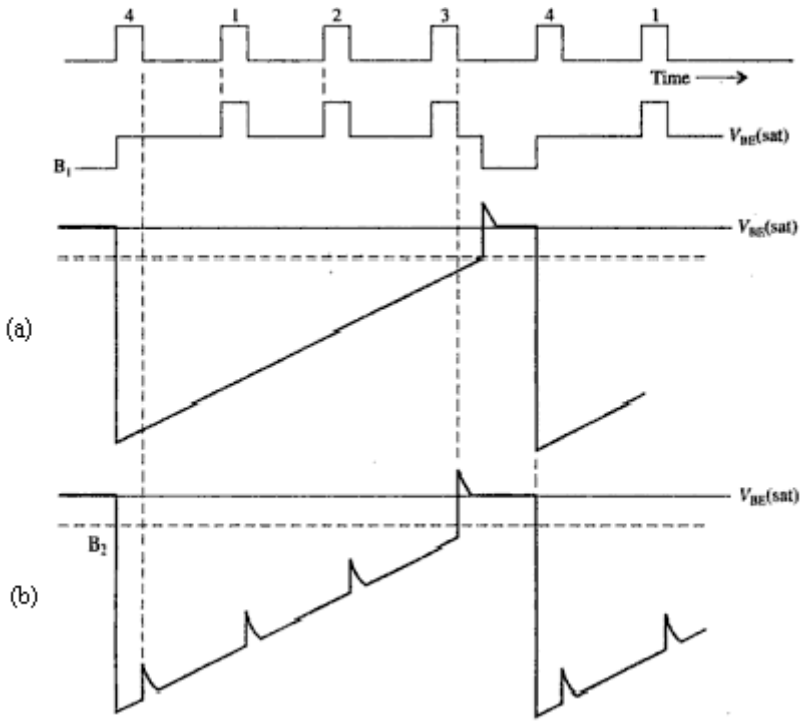


Fig 7.7 (a) waveform at B2 with no pulse overshoot and (b) waveform at B2 with pulse overshoot

7.6 Stability of Relaxation Dividers

There will normally be some small delay between an input pulse to a divider and the output pulse. This delay is referred to as a *phase delay* and results from the finite rise time of the input trigger pulse and the finite response time of the relaxation device. The phase delay itself is subject to variation with time due to variations in device characteristics, supply voltages, etc.

Occasionally some extraneous signal may be coupled unintentionally into the divider. Such a signal may have an influence on the exact moment at which a device waveform say, reaches cutoff. In this case the phase delay may be subject to periodic variations. All these factors which affect the phase delay give rise to what is termed *phase jitter.* Even in the absence of an extraneous signal it is found experimentally that in the divider circuits phase jitter is of the order of 0.1 Ilsec.

In a large-scale counter consisting of many stages, the phase jitter is, of course, compounded. In many applications phase jitter is of no particular consequence, while sometimes, particularly in connection with mill microsecond pulses, it constitutes an important difficulty. A method for achieving division without phase jitter is illustrated schematically in Fig. 12-9 together with the waveforms depicting the operation. The train of regularly spaced input pulses (I) is applied to the divider input. The output of the divider consists of the pulses shown in waveform *(D).* These latter pulses trigger a gating waveform generator (say, a monostable multi) which provides a gate of duration *To* adequate to encompass each pulse labeled" I." This waveform is applied to a gating or coincidence circuit which is opened for transmission for the duration *To.* The input pulse train is applied to the gating circuit, and its output, waveform 0, then consists of each pulse labeled" 1." We may take advantage of the phase delay between waveform I and *D* (not shown in the figure) together with the finite rise time of the gating waveform to ensure that pulse *n* does not pass through the gating circuit. The duration of the gate is not critical, since it is only required that the duration be longer than the interval between pulses and shorter than the interval between alternate pulses *(T p < To < 2T p).* Of course, the coincidence circuit must introduce no phase delay.

A much more commonly encountered jitter in dividers and synchronized relaxation oscillators results from the instability of the natural timing period of the oscillator. This instability of period is caused principally by the variability of tube characteristics and may result either in a loss of synchronism ur an incorrect division ratio in a divider. For example, in an *n:* 1 divider a change in natural timing period can cause the relaxation oscillator to fire at the *(n* - l)st or the *(n* + l)st pulse rather than at the nth pulse. Similarly, in a 1: 1 synchronized device, if the natural period *To* should drift and become smaller than the interval between pulses, then synchronization of each cycle will be lost.

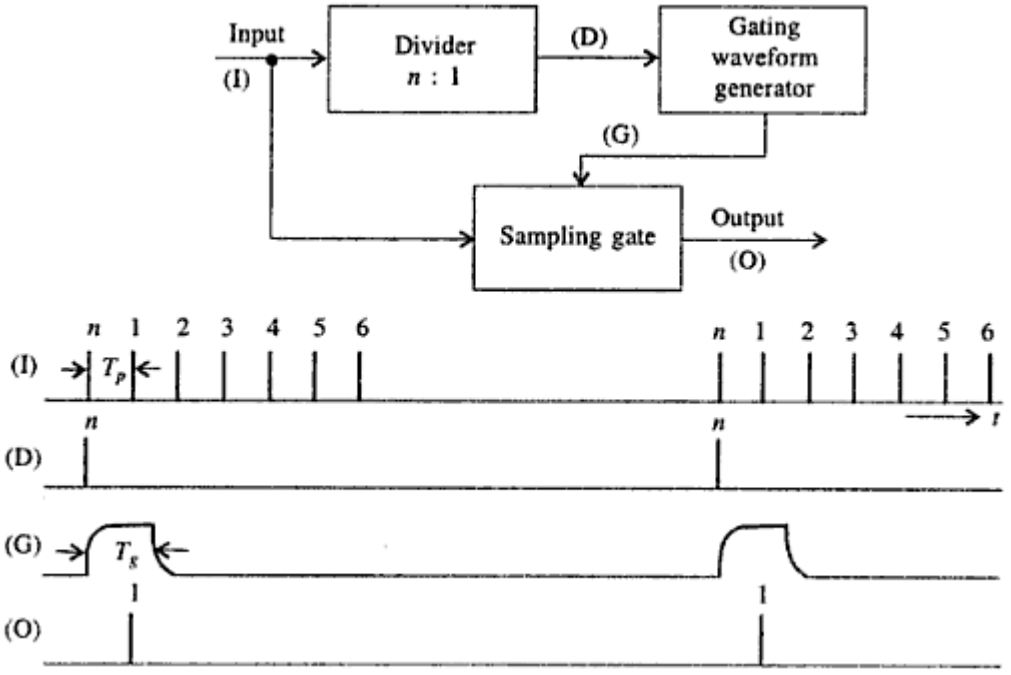


Fig7.8 block diagram and wavefrom for a divider without phase jitter

7.7 Synchronization of a sweep circuits with Sinusoidal Signals

Up to the present we have considered the phenomenon of synchronization only for the case of pulse-type synchronizing signals. We have assumed that the synchronizing signal consists of a train of waveforms with leading edges which rise abruptly. We shall now consider the case in which the voltage variation of the sync signal is gradual rather than abrupt. We shall discuss explicitly only the case of a sinusoidal sync signal, but the results

will easily be seen to apply to any gradually varying waveform. Again, the mechanism of synchronization is so nearly identical for all types of relaxation oscillators that we may without loss of generality select anyone of them, say, the sweep generator, for detailed consideration. Let us start then by considering the case of a UJT sweep generator .*if sinusoidal sync pulses are* applied a sinusoidal sync signal whose period *T* is exactly equal to the natural period *To* of the UJT sweep. For a positive value of the sync signal, the breakdown voltage is lowered, as indicated in Fig 7.9.

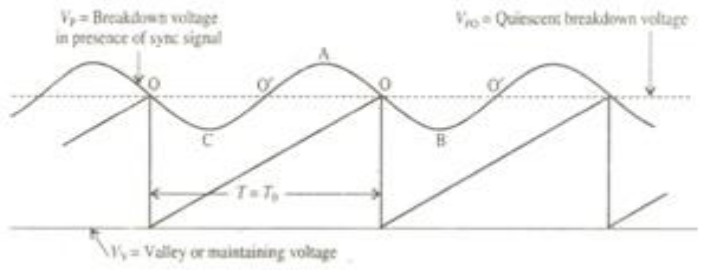


Fig 7.9 the timing relationship that must exist between Vp and the seep voltage in a synchronized sweep when T=To

In the case of pulse synchronization we noted that synchronism could result only if the sync signal period was equal to or less than the natural period. This feature resulted from the fact that a pulse could serve reliably only to terminate timing cycle prematurely and not to lengthen it. In the present case, however, synchronization is possible both when *Tp* < *To* and when *Tp* > *To.* The sweep voltage drawn as a solid line has a natural period T~ > *T.* The sweep voltage meets the o curve at a point below E_{bo} and is consequently prematurely terminated. The dashed sweep voltage has a natural period T~' < *T.* This sweep meets the *Eb* curve at a point above *Ebo* and is consequently lengthened. In each case the synchronized period *Ts* equals the period *T.* The general situation may be described by reference to Fig.. When *T* = *To,* the sweep is terminated at voltage and the breakdown voltage for both cases is shown in Fig 7.10(a).

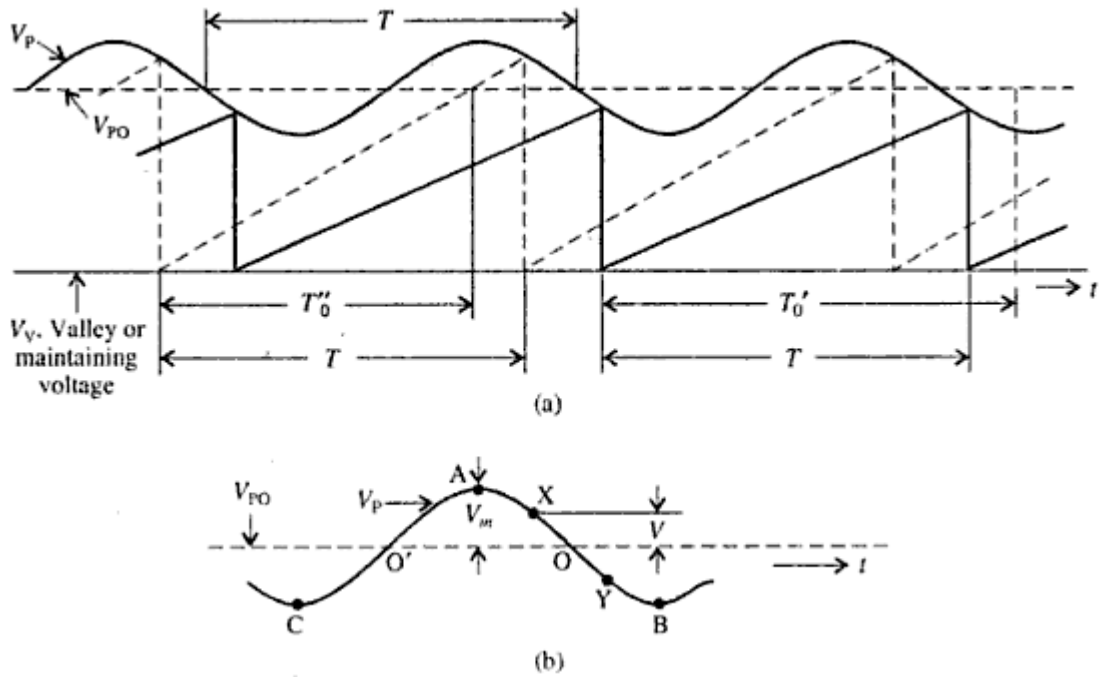


Fig 7.10 (a) shows the timing of the sweep voltage with respect to Vp for case in which T<To"(dasahed line) and (b) pertains to the general case, T≠To

The sweep voltage drawn as a solid line has a natural period T~ > *T*. The sweep voltage meets the *Eb* curve at a point below *E bo* and is consequently prematurely terminated. The dashed sweep voltage has a natural period T~' < *T*. This sweep meets the *Eb* curve at a point above Ebo and is consequently lengthened. In each case the synchronized period *Ts* equals the period *T*.

The general situation may be described by reference to Fig 7.10 (b). When *T* = *To*, the sweep is terminated at point 0, leaving the period unaltered. When *T* > *To*, the sweep terminates at a point such as X between 0 and the positive maximum *A*. When *T* < *To*, the sweep terminates at a point such as *Y* between 0 and the negative maximum *B*. When the period *T* is such that the sweep terminates either at the point *A* or *B*, the limits of synchronization have been reached, since at *A* the sweep period has been lengthened to the maximum extent possible, while at *B* the shortening is at maximum.

REALIZATION OF LOGIC GATES USING DIODES & TRANSISTORS

8.1 Introduction to Digital Logic Gates

A **Digital Logic Gate** is an electronic device that makes logical decisions based on the different combinations of digital signals present on its inputs. A digital logic gate may have more than one input but only has one digital output. Standard commercially available digital logic gates are available in two basic families or forms, **TTL** which stands for ***Transistor-Transistor Logic*** such as the 7400 series, and **CMOS** which stands for ***Complementary Metal-Oxide-Silicon*** which is the 4000 series of chips. This notation of TTL or CMOS refers to the logic technology used to manufacture the integrated circuit, (IC). **TTL** IC's use NPN (or PNP) type ***Bipolar Junction Transistors*** while **CMOS** IC's use ***Field Effect Transistors*** or FET's for both their input and output circuitry.

Digital Logic States

In digital logic design only two voltage levels or states are allowed and these states are generally referred to as Logic "1" and Logic "0", High and Low.

Most *digital logic gates* and logic systems use "Positive logic", in which a logic level "0" or "LOW" is represented by a zero voltage, 0v or ground and a logic level "1" or "HIGH" is represented by a higher voltage such as +5 volts, There also exists a complementary "Negative Logic" system in which the values and the rules of a logic "0" and a logic "1" are reversed but in this tutorial section about digital logic gates we shall only refer to the positive logic convention as it is the most commonly used.

Some important points to be remembered

Propagation delay is the average transition delay time for a pulse to propagate from input to output of a switching circuit

- Fan-in is the number of inputs to the gate which it can handle.
- Fan-out is the number of loads the output of a gate can drive without effecting its operation.
- Power dissipation is the supply voltage required by the gate to operate with 50% duty cycle at a given frequency
- RTL, DTL, DTL are the logic families which are now obsolete.
- TTL is the most widely used logic family.
- TTL gates may be:

  (a) Totem pole

  (b) Open collector

  (c) Tri-state
- TTL is used in SSI and MSI Integrated circuits and is the fastest of all standard logic families.
- Totem pole TTL has the advantage of high speed and low power dissipation but its Dis advantage is that it cannot be wired ANDed because of current spikes generation.
- Tri-state has three states :

  (a) High

  (b) Low

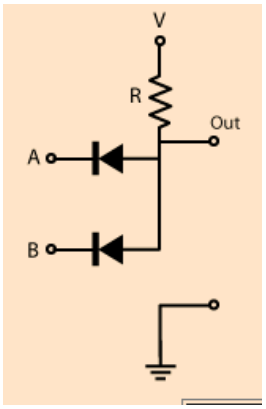
  (c) High Impedance
- ECL is the fastest of all logic families because its propagation delay is very small i.e. of

  about 2 nsec.
- ECL can be wired ORed.
- MOS logic is the simplest to fabricate.
- MOS transistor can be connected as a resistor.
- MOSFET circuitries are normally constructed from NMOS devices because they are 3 times faster than PMOS devices.
- CMOS uses both P-MOS and N-MOS.
- CMOS needs less power as compared to ECL as they need maximum power.
- Both NMOS and PMOS are more economical than CMOS because of their greater

packing densities.

- Speed of CMOS gates increases with increase in VDD.
- CMOS has large fan-out because of its low output resistance.

8.2 Two Input AND Gate using diodes with Truth table

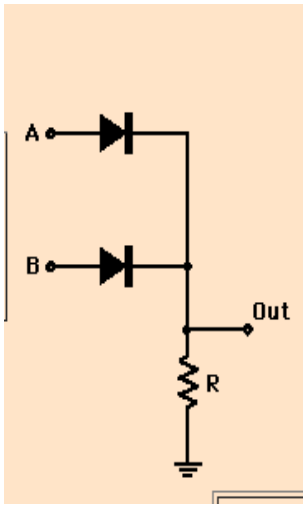


2 Input AND gate		
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

Fig 8.1 two input AND gate using diodes

When the input is logic 1 both the diodes are reverse biased so the output voltage is logic 1.when any one of the diode is forward biased output voltage is logic zero

8.3 Two Input OR Gate Using Diodes with Truth table



2 Input OR gate		
A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

Fig 8.2 two input OR gate using diodes

When any one of the diode is forward biased output is logic 1.when both the diodes are reverse biased output voltage is logic 0

8.4 Basic NOT Gate Using Transistor

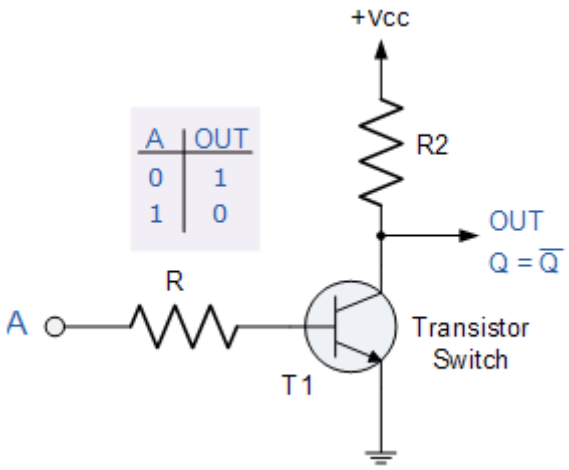


Fig 8.3 Basic NOT gate using Transistor

When the input voltage is positive and it is more than the cut-in voltage (0.7)transistor is operated in saturation region. When the input voltage is negative and 0 transistor is operated in cut-off so output is $V_{cc.}$

8.5 Different logic families

RTL (Resistor transistor logic)

DCTL (Direct coupled transistor logic)

DTL (Diode transistor logic)

TTL (transistor transistor logic)

ECL (Emitter coupled logic)

CMOS (Complementary metal oxide semiconductor)

8.5.1 RTL NOR GATE

By connecting additional base resistors (R_3 and R_4) to the inverter it is expanded to the simplest RTL NOR gate. It is interesting fact that the basic input logical operation OR is performed by applying consecutively the two arithmetic operations addition and comparison

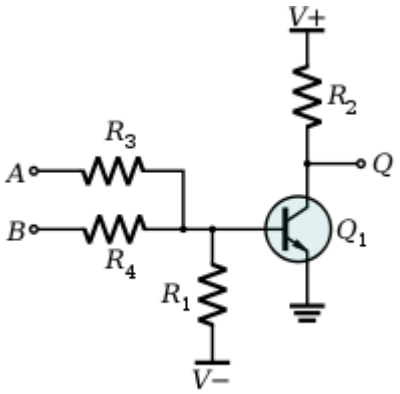


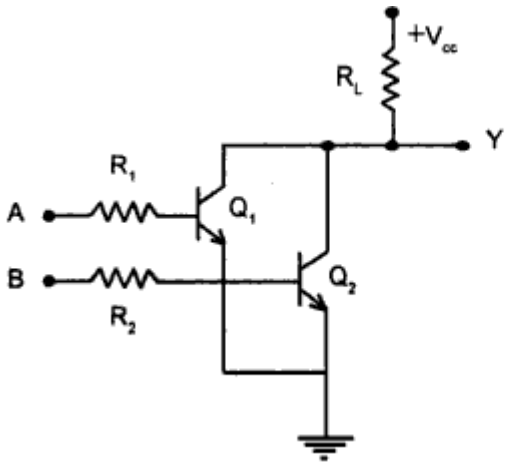
Fig 8.4 two input RTL NOR gate

LIMITATIONS OF RTL

The obvious disadvantage of RTL is its high power dissipation when the transistor is switched on (the power is dissipated mainly by the base resistors connected to logical "1" and by the collector resistor). This requires that more current be supplied to and heat be removed from RTL circuits. In contrast, TTL circuits with "totem-pole" output stage minimize both of these requirements. Another limitation of RTL was its limited fan-in and It has a low noise margin.

8.5.2 DIRECT COUPLED TRANSISTOR LOGIC

Figure shows the circuit for DCTL-NOR gate and DCTL-NAND gates



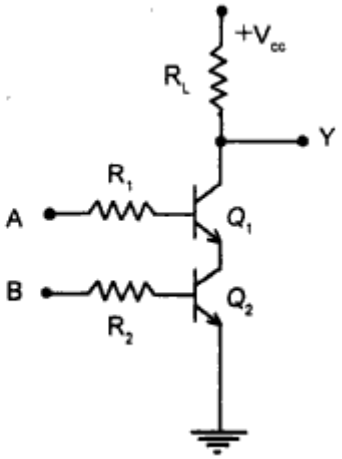


Fig 8.5 (a) DCTL-NOR GATE *(b) DCTL-NAND GATE*

In DCTL – two input NOR gate of Fig 8.5 (a), there are two transistors Q1 and Q2 which share a common load resistor R_1. If any one or both inputs A and B are high at level "1", then base current will be supplied to one or both the transistors, causing them to conduct and thus collector current will flow through load resistor R_L. This makes output voltage at Y to go low. Whereas when both A and B are low, both transistors Q_1 and Q_2 remain in cut-off state and thus the output at Y approaches that of the supply voltage V_{cc} at high level.

In the DCTL- two input NOR gate of Fig 8.5(b), both the transistors Q_1 and Q_2 are connected in series. Only when both inputs A and B are high, both transistors Q_1 and Q_2 will conduct, as they are in series. This causes output voltage at Y to go low. When any one or both inputs A and B are low, both transistors Q_1 and Q_2 cannot conduct. Therefore the output voltage at Y remains high.

DCTL is a very simple logic as it requires few components and can be easily manufactured in IC form. But it suffers from two serious drawbacks of currents hogging and low noise margin. Current hogging exists due to variations in the input characteristics of the transistors used. When two or more identical transistors are fed from the same output, equal sharing of current does not take place due to non-linearity of input characteristics. The transistor with lower input impedance draws more current than the other transistors. The transistors which draw less current will not turn on properly and give rise to malfunctioning of the circuit. This phenomenon is known as current hogging or more precisely as base current hogging.

8.5.3 THREE INPUT DTL NAND GATE

The DTL NAND gate combines the DTL inverter with a simple Diode Logic (DL) AND gate. Thus, any number of inputs can be added simply by adding input diodes to the circuit. The problem of signal degradation caused by Diode Logic is overcome by the transistor, which amplifies the signal while inverting it. This means DTL gates can be cascaded to any required extent, without losing the digital signal.

In addition, the use of diodes in this configuration permits the construction of NAND gates; something that was not practical with RTL because there was no practical way to allow any single logic 0 input to override multiple logic 1 inputs. Therefore, DTL offers more possible configurations as well as better performance than RTL.

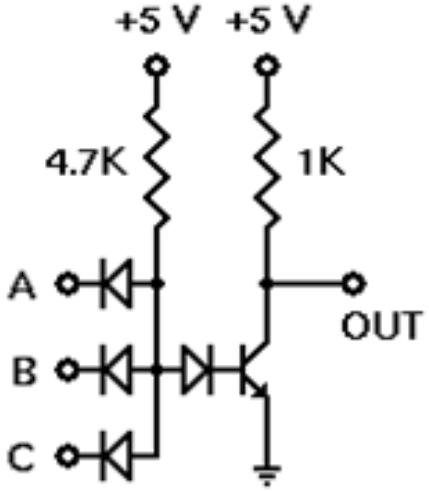


Fig 8.6 three input DTL NAND gate

8.5.4 STANDARD TTL-NAND GATE ANLYSIS AND CHARACTERISTICS

In standard TTL (transistor-transistor logic) IC's there is a pre-defined voltage range for the input and output voltage levels which define exactly what is a logic "1" level and what is a logic "0" level and these are shown below.

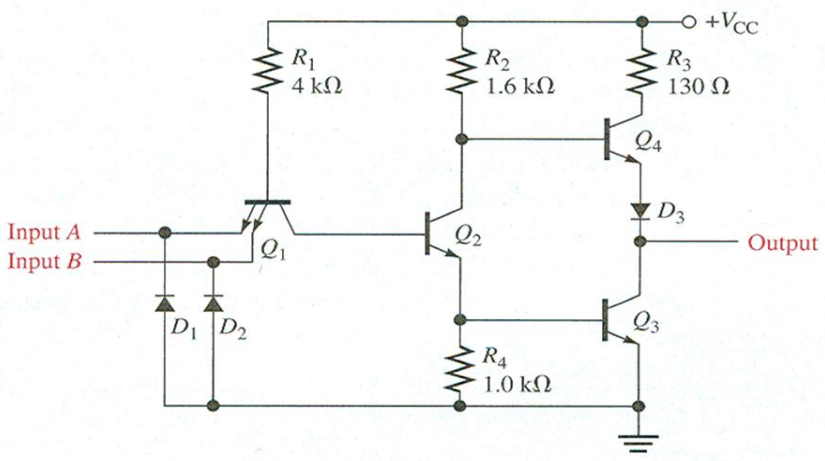


Fig 8.7 two input TTL NAND gate

Transistor–transistor logic (**TTL**)

It is a class of digital circuits built from bipolar junction transistors (BJT) and resistors. It is called *transistor–transistor logic* because both the logic gating function (e.g., AND) and the amplifying function are performed by transistors (contrast with RTL and DTL).

TTL inputs are the emitters of a multiple-emitter transistor. This IC structure is functionally equivalent to multiple transistors where the bases and collectors are tied together.[11] The output is buffered by a common emitter amplifier.

Input logical ones

When all the inputs are held at high voltage, the base–emitter junctions of the multiple-emitter transistor are backward-biased. In contrast with DTL, small (about 10 μA) "collector" currents are drawn by the inputs since the transistor is in a reverse-active mode (with swapped collector and emitter). The base resistor in combination with the supply voltage acts as a substantially constant current source. It passes current through the base–

collector junction of the multiple-emitter transistor and the base–emitter junction of the output transistor thus turning it on; the output voltage becomes low (logical zero).

Input logical zero

If one input voltage becomes zero, the corresponding base–emitter junction of the multiple-emitter transistor connects in parallel to the two connected in series junctions (the base–collector junction of the multiple-emitter transistor and the base–emitter junction of the second transistor). The input base–emitter junction steers all the base current of the output transistor to the input source (the ground). The base of the output transistor is deprived of current causing it to go into cut-off and the output voltage becomes high (logical one). During the transition the input transistor is briefly in its active region; so it draws a large current away from the base of the output transistor and thus quickly discharges its base. This is a critical advantage of TTL over DTL that speeds up the transition over a diode input structure.
The main disadvantage of TTL with a simple output stage is the relatively high output resistance at output logical "1" that is completely determined by the output collector resistor. It limits the number of inputs that can be connected (the fan-out). Some advantage of the simple output stage is the high voltage level (up to V_{CC}) of the output logical "1" when the output is not loaded.

TTL OPEN COLLECTOR OUTPUTS

An **open collector** is a common type of output found on many integrated circuits (IC). Instead of outputting a signal of a specific voltage or current, the output signal is applied to the base of an internal NPN transistor whose collector is externalized (open) on a pin of the IC. The emitter of the transistor is connected internally to the ground pin. If the output device is a MOSFET the output is called **open drain** and it functions in a similar way.

In the single-input (inverter) circuit, grounding the input resulted in an output that assumed the "high" (1) state. In the case of the open-collector output configuration, this "high" state was simply "floating." Allowing the input to float (or be connected to V_{cc}) resulted in the output becoming grounded, which is the "low" or 0 state. Thus, a 1 in resulted in a 0 out, and vice versa.

Since this circuit bears so much resemblance to the simple inverter circuit, the only difference being a second input terminal connected in the same way to the base of transistor

Q_2, we can say that each of the inputs will have the same effect on the output. Namely, if either of the inputs are grounded, transistor Q_2 will be forced into a condition of cutoff, thus turning Q_3 off and floating the output (output goes "high"). The following series of illustrations shows this for three input states (00, 01, and 10):

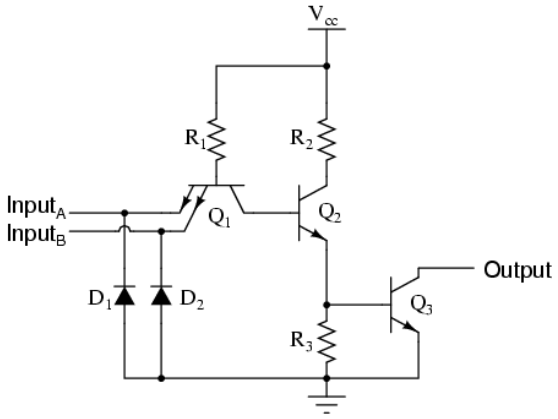


Fig 8.8 open collector inverter circuit

When Q_3 is OFF, the output is pulled up to V_{cc} through the external resistor. When Q_3 is ON, the output is connected to near-ground through the saturated transistor

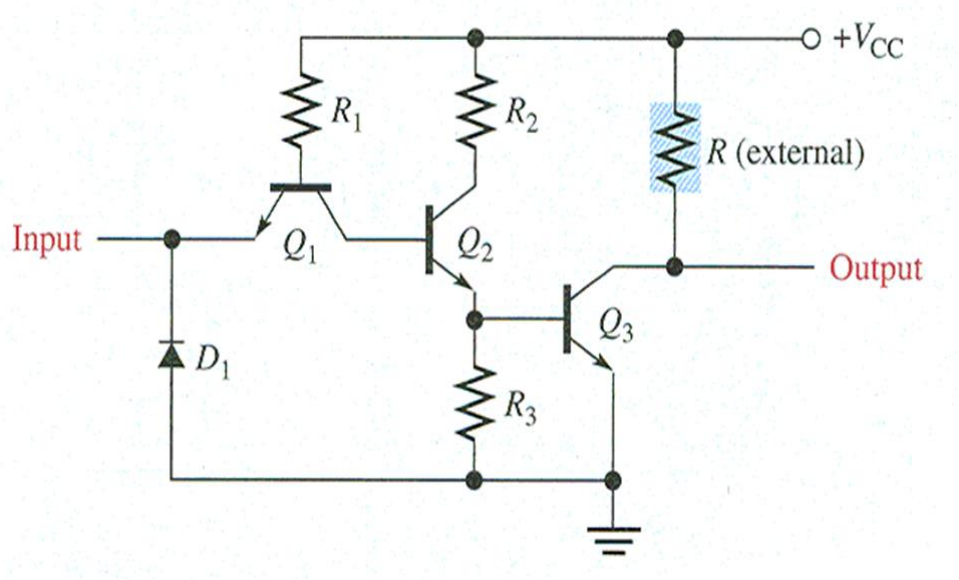


Fig.8.9 With external pull-up resistor

Tristate TTL GATES:

In digital electronics **three-state**, **tri-state**, or **3-state** logic allows an output port to assume a high impedance state in addition to the 0 and 1 logic levels, effectively removing the output from the circuit. This allows multiple circuits to share the same output line or lines (such as a bus).

INPUT		OUTPUT
A	B	C
0	1	0
1		1
X	0	Z

Three-state outputs are implemented in many registers, bus drivers, and flip-flops in the 7400 and 4000 series as well as in other types, but also internally in many integrated circuits. Other typical uses are internal and external buses in microprocessors, memories, and peripherals. Many devices are controlled by an active-low input called OE (Output Enable) which dictates whether the outputs should be held in a high-impedance state or drive their respective loads (to either 0- or 1-level).

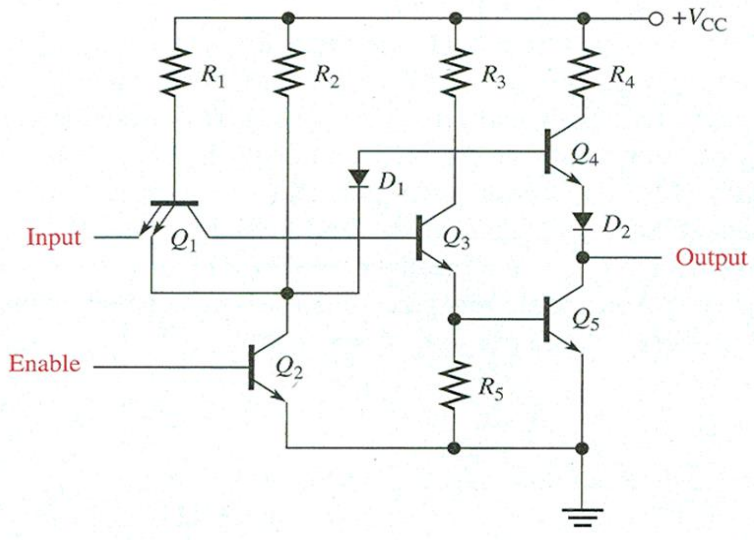


Fig.8.10 Tristate TTL gate

8.5.5 Emitter-coupled logic (ECL)

It is a logic family that achieves high speed by using an overdriven BJT differential amplifier with single-ended input whose emitter current is limited to avoid the slow saturation region of transistor operation. As the current is steered between two legs of

an emitter-coupled pair, ECL is sometimes called ***current-steering logic*** **(*current-mode logic*** **(CML) or *current-switch emitter-follower*** **(CSEF)** logic.

In ECL, the transistors are never in saturation, the input/output voltages have a small swing (0.8 V), the input impedance is high and the output resistance is low; as a result, the transistors change states quickly, delays are low, and the fan out capability is high. In addition, the essentially-constant current draw of the differential amplifiers minimizes delays and glitches due to supply-line inductance and capacitance, and the complementary outputs decrease the propagation time of the whole circuit by saving additional inverters.

ECL's major disadvantage is that each gate continuously draws current, which means it requires (and dissipates) significantly more power than those of other logic families, especially when quiescent.

The ECL circuit operation is considered below with assumption that the input voltage is applied to T1 base, while T2 input is unused or a logical "0" is applied. During the transition, the core of the circuit – the emitter-coupled pair (T1 and T3) – acts as a differential amplifier with single-ended input. The "long-tail" current source (R_E) sets the total current flowing through the two legs of the pair. The input voltage controls the current flowing through the transistors by sharing it between the two legs, steering it all to one side when not near the switching point. The gain is higher than at the end states (see below) and the circuit switches quickly.

At low input voltage (logical "0") or at high input voltage (logical "1") the differential amplifier is overdriven. The one transistor (T1 or T3) is cut-off and the other (T3 or T1) is in active linear region acting as a common-emitter stage with emitter degeneration that takes all the current, starving the other cut-off transistor.

The active transistor is loaded with the relatively high emitter resistance R_E that introduces a significant negative feedback (emitter degeneration). To prevent saturation of the active transistor so that the diffusion time that slows the recovery from saturation will not be involved in the logic delay, the emitter and collector resistances are chosen such that at maximum input voltage some voltage is left across the transistor. The residual gain is low ($K = R_C/R_E < 1$). The circuit is insensitive to the input voltage variations and the transistor stays firmly in active linear region. The input resistance is high because of the series negative

feedback.

The cut-off transistor breaks the connection between its input and Output. As a result, its input voltage does not affect the output voltage. The input resistance is high again since the base-emitter junction is cut-off.

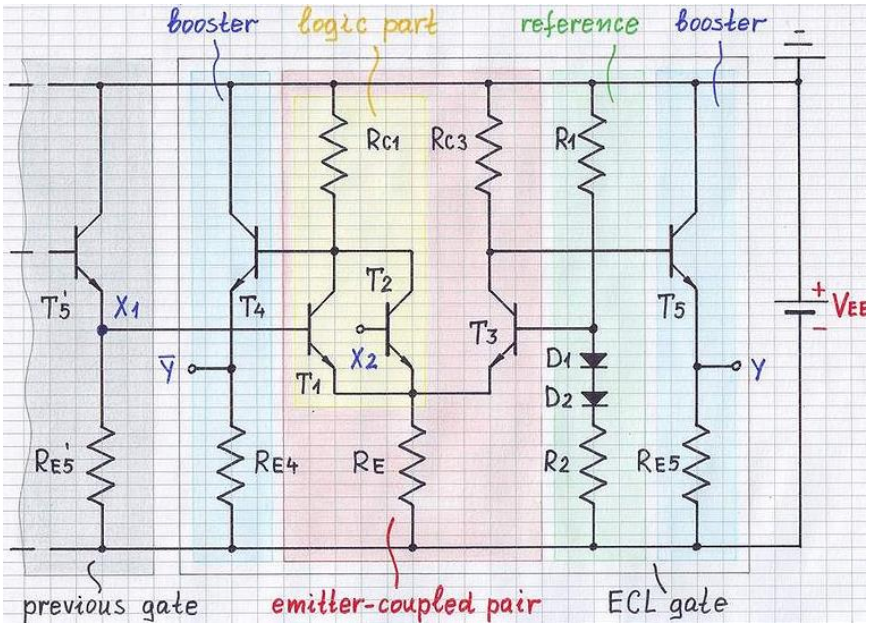


Fig.8.11 Emitter-coupled logic circuit

ECL OR GATE:

Emitter-coupled logic (ECL) is the fastest of all logic families and thus it is used in applications where very high speed is essential. High speeds have become possible in ECL because the transistors are used in difference amplifier configuration, in which they are never driven into saturation and thereby the storage time is eliminated. Here, rather than switching the transistors from ON to OFF and vice-versa, they are switched between cut-off and active regions. Propagation delays of less than 1 ns per gate have become possible in ECL.

Basically, ECL is realized using difference amplifier in which the emitters of the two transistors are connected and hence it referred to as emitter-coupled logic. A 3-input ECL gate is shown in Fig. (A) Which has three parts. The middle part is the difference amplifier which performs the logic operation.

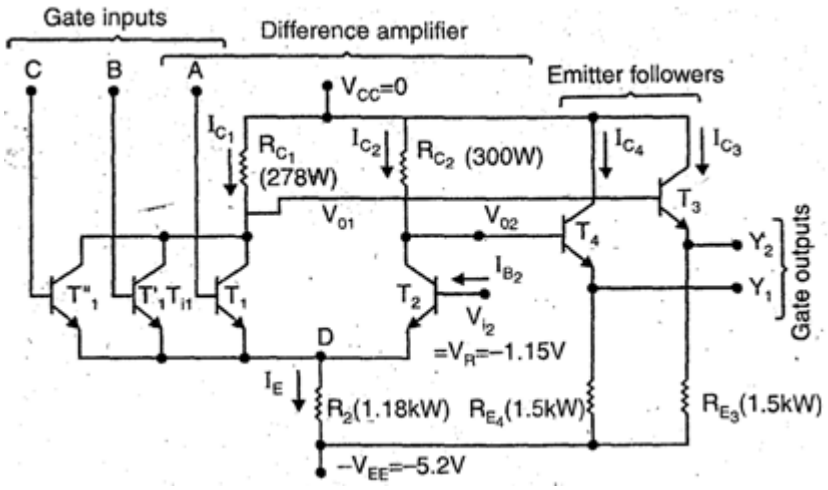


Fig 8.12 a 3 input ECL OR/NOR gate

Emitter followers are used for d.c level shifting of the outputs, so that V (0) and V (1) are same for the inputs and the outputs. Note that two outputs Y1 and Y2 are available in this circuit which is complementary. Y1. Corresponds to OR logic and Y2 to NOR logic and hence it is named as an OR/NOR gate.

Additional transistors are used in parallel to T1 to get the required fan-in. There is a fundamental difference between all other logic families (including MOS logic) and ECL as far as the supply voltage is concerned. In ECL, the positive end of the supply is connected to ground in contrast to other logic families in which negative end of the supply is grounded. This is done to minimize the effect of noise induced in the power supply and protection of the gate from an accidental short circuit developing between the output of a gate and ground. The voltage corresponding to V (0) and V (1) are both negative due to positive end of the supply being connected to ground. The symbol of an ECL OR/NOR gate is shown in Fig 8.13

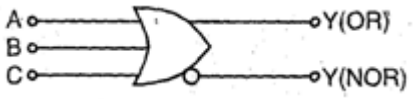


Fig 8.13 the symbol for a 3-input OR/NOR gate

8.6 CML Logic Families and its Comparison

8.6.1 Compare performance of ECL with TTL

ECL	TTL
1. Propagation delay in 500 Ps.	1. Propagation delay is 10 ns.
2. Noise margin is 150 mV.	2. Noise margin is 0.4 V.
3. Power dissipation is 5 mW.	3. Power dissipation is 10 mW.
4. Fanout is 25.	4. Fanout is 10.
5. 0.5 PJ is figure of merit.	5. Figure of merit is 100 PJ.

8.6.2 Compare performance of DTL and TTL

Parameter	DTL	TTL
1. Fan-out	8	10 to 20
2. Power Dissipation (mW)	8-12	10
3. Noise immunity	Good	Very good
4. Propagation Delay (sec)	30	10
5. Clock rate (MHz)	72	35

8.6.3 Comparison of TTL and ECL:

Parameter	TTL	ECL
Fan out	10	25
Propagation Delay	10ns	500 ps
Power Dissipation	10 mW	50 mW
Noise Margin	0.4 V	150 mV
Figure of merit (Or) Speed Power Product	100 PJ	0.5 pJ

8.6.4 Comparison of various logic families

	RTL	DTL	TTL					ECL	CMOS
			Standard	High power speed H	Low power low speed L	Schotlky low power LS	Schotlky standard S		
1. Fan out	5	8	10	10	20	20	10	25	>50
2. Power dissipation (mw) per gate	12	8-12	10	22	1	2	19	40-55	0.01 static; 1 at 1 MHz
3. Propagation delay per gate (nS)	12	30	10	6	33	9.5	3	2	70
4. Clock Rate (MHz) for FFs	8	72	35	50	3	45	125	>60	10

	Parameter	RTL	I^2L	DTL	HTL	TTL	ECL	MOS	CMOS
1.	Basic Gate	NOR	NOR	NAND	NAND	NAND	OR-NOR	NAND	NOR or NAND
2.	Fan-out	5	Depends on injector current	8	10	10 to 20	25	20	20 to 50
3.	Power dissip-ation in mW	12	6mm to 70 µM	8-12	55	10	40-55	0.2-10	0.0025
4.	Noise immunity	Nominal	Poor	Good	Excellent	Very Good	Poor	Good	Very Good
5.	Propagation delay (in sec.)	12	25-250	30	90	10	0.75	300	70.0
6.	Clock rate (MHZ)	8	–	72	4	35	>60	2	10
7.	Available functions	High	LSI only	Fairly high	Nominal	Very high	High	low	High

Code No: 44106 **Set No. 1**

II B.Tech II Semester Regular Examinations, Apr/May 2009
PULSE AND DIGITAL CIRCUITS
(Common to Electronics & Communication Engineering, Bio-Medical Engineering, Electronics & Control Engineering, Electronics & Telematics, Electronics & Computer Engineering and Instrumentation & Control Engineering)

Time: 3 hours Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Prove that for any periodic input wave form the average level of the steady state output signal forms Rc high pass circuit is always zero

(b) Explain how a low pass RC circuit acts as an integrator. [8+8]

2. (a) Design a clipping circuit with ideal components, which can give the waveform Shown in Fig.2a for a sinusoidal input.

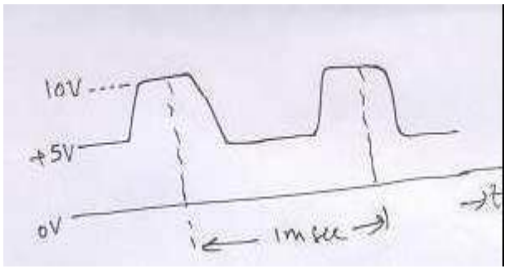


Fig. 2a

(b) State and prove clamping circuit theorem. [8+8]

3. (a) Explain how a transistor can be used as a switch.

(b) Explain the phenomenon of 'Latching" in a transistor switch [8+8]

4. Explain the method of unsymmetrical triggering of the binary with relevant circuit diagram. [16]

5. (a) If the amplifier gain is different from unity in a bootstrap circuit, what is the effect on the sweep voltage? What is the effect of amplifier bandwidth on the sweep output?

(b) In UJT sweep circuit VBB = 20 V, VY Y = 50V, R = 5k , RB1 = RB2 = 0 and C= 0.01 μF. the UJT fires when Vc = 10.6V and goes to OFF state when Vc = 2.8V. Find the

i. the amplitude of sweep signal

ii. the slope and displacement error

iii. the duration of the sweep, and

iv. the recovery time. [16]

6. (a) Explain the method of synchronization of a sinusoidal oscillator with pulses.

(b) Describe frequency division employing a transistor monostbale multivibrator. [8+8]

7. (a) Draw the circuit diagram of the unidirectional diode gate with more than two inputs and explain its operation.

(b) How do you overcome the loading effect of signal sources on control voltage?

(c) Draw the circuit diagram of a sampling gate with more than one control voltage and explain its working. [16]

8. (a) Define positive and negative logic system

(b) Define fan-In, fan-out

(c) Draw and explain the circuit diagram of a diode OR gate for positive logic.

[4+4+8]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: 44106 **Set No. 2**

II B.Tech II Semester Regular Examinations, Apr/May 2009
PULSE AND DIGITAL CIRCUITS
(Common to Electronics & Communication Engineering, Bio-Medical Engineering, Electronics & Control Engineering, Electronics & Telematics, Electronics & Computer Engineering and Instrumentation & Control Engineering)

Time: 3 hours Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Write a short notes on RC low pass circuit

(b) Draw the output response of RC low pass circuit for a step input signal and explain in detailed. [8+8]

2. (a) Draw the diode comparator circuit and explain the operation of it when ramp input signal is applied.

(b) Explain the operation of two level slicer. [10+6]

3. (a) Explain how a BJT can be used as a switch. Compare it performance as a switch with BBJT

(b) Describe the switching times of BJT by considering the charge distribution across the base region. Explain this for cut-off, active and saturation region. [8+8]

4. Draw and explain about the response of Schmitt circuit for the following.

(a) for loop gain _1

(b) loop gain >1. [16]

5. (a) What is a linear time base generator?

(b) Write the applications of time base generators.

(c) Define the sweep speed error, displacement error and transmission error of voltage time base waveform. [16]

6. (a) Explain the method of synchronization of a sinusoidal oscillator with pulses.

(b) Describe frequency division employing a transistor monostbale multivibrator. [8+8]

7. (a) Draw the circuit diagram of the unidirectional diode gate with more than two inputs and explain its operation.

(b) How do you overcome the loading effect of signal sources on control voltage?

(c) Draw the circuit diagram of a sampling gate with more than one control voltage

and explain its working. [16]

8. (a) What are the basic logic gates which perform all the operations in digital systems.

(b) Give some applications of logic gates.

(c) Define a positive and negative pulse logic systems.

(d) Draw a pulse train representing 1101011001. [16]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: 44106 **Set No. 3**

II B.Tech II Semester Regular Examinations, Apr/May 2009
PULSE AND DIGITAL CIRCUITS
(Common to Electronics & Communication Engineering, Bio-Medical Engineering, Electronics & Control Engineering, Electronics & Telematics, Electronics & Computer Engineering and Instrumentation & Control Engineering)

Time: 3 hours Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Explain about RLC Ringing Circuit

(b) Explain RC double differentiator circuit. [8+8]

2. (a) For the circuit shown in figure 2a , Vi is a sinusoidal voltage of peak 100 volts. Assume ideal diodes. Sketch one cycle of output voltage. Determine the maximum diode Current.

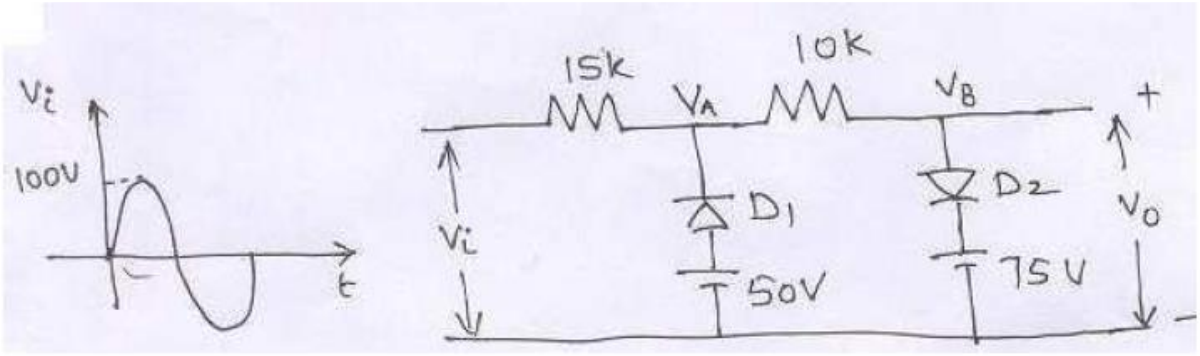


Figure 2a

(b) Explain positive peak clipping with reference voltage. [12+4]

3. (a) Describe the switching times of BJT by considoring charge distribution across the base region. Explain this far cut-off, active and saturation region.

(b) Give the expressions for rise time & fall time in terms of trunsistor parameters and operating corrents. [8+8]

4. Consider the Schmitt trigger of the following figure 4 with germanium transistors having hFE=40. The circuit parameters are VCC=55V, Rs=3.9K, Rc1=12K, Rc2=2K, R1=39K, R2=180K and Re=39K. Calculate [16]

(a) V1

(b) V2.

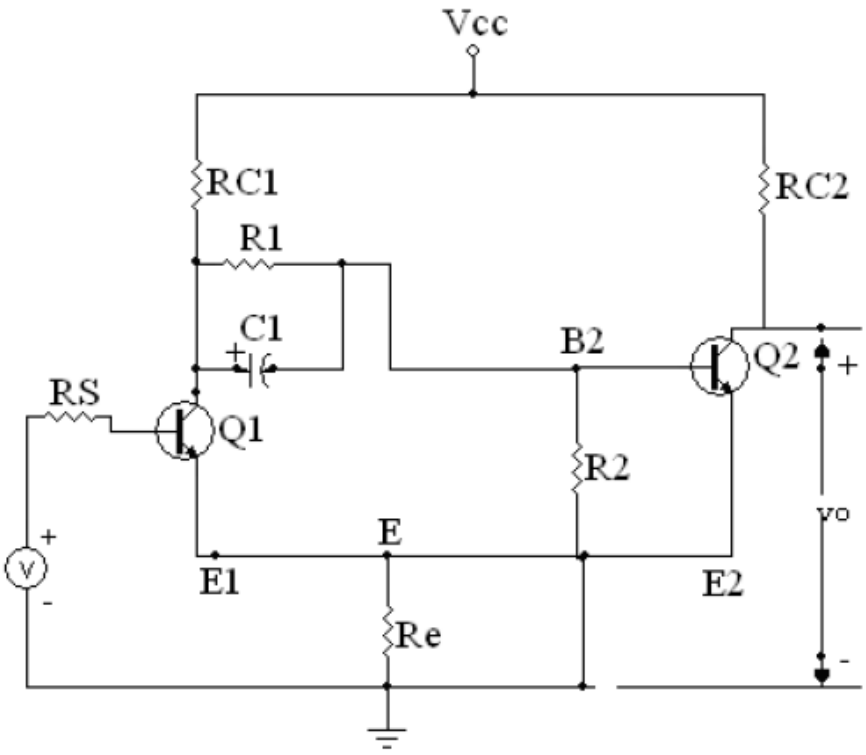


Figure 4

5. (a) Draw the circuit diagram of fixed amplitude sweep circuit and explain its operation.

(b) Draw the circuit diagram of transistor Miller time base generator and explain its working. [16]

6. (a) With the help of a circuit diagram and waveforms, explain frequency division of an astable multivibrator with pulse signals.

(b) The relaxation oscillator, when running freely, generates an output signal of peak - to - peak amplitude 100V and frequency 1 kHz. Synchronizing pulses are applied of such amplitude that at each pulse the breakdown voltage is lowered by 20V. Over what frequency range may the sync pulse frequency be varied if 1 : 1 synchronization is to result? If 5 : 1 synchronization is to be

obtained (fP /fS = 5), over what range of frequency may the pulse source be varied? [16]

7. (a) What is pedestal? How it effects the output of a sampling gate?

(b) What are the applications of sampling gates?

(c) Explain clearly the disadvantages of two diode bidirectional sampling gate compared to four divide gate. [6+4+6]

8. (a) Draw the circuit diagram of diode - resistor logic OR gate and explain its operation.

(b) The transistor inverter (NOT gate) circuit has a minimum value hfe = 30, VCC = 12V, RC = 2.2k, R1 = 15k and R2 =100k, VBB = 12V. Prove that circuit works as NOT gate. Assume typical junction voltages. The input is varying between 0 and 12V. [16]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: 44106 **Set No. 4**

II B.Tech II Semester Regular Examinations, Apr/May 2009
PULSE AND DIGITAL CIRCUITS
(Common to Electronics & Communication Engineering, Bio-Medical Engineering, Electronics & Control Engineering, Electronics & Telematics, Electronics & Computer Engineering and Instrumentation & Control Engineering)

Time: 3 hours Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks
⋆ ⋆ ⋆ ⋆ ⋆

1. (a) A symmetrical square wave whose peak-to-peak amptitude id 2V and whose average value is zero as applied to on Rc integrating circuit. The time constant

is equals to half -period of th esquare wave find the peak to peak value of the output amplitude

(b) Describe the relationship between rise time and RCtime constant of a low pass RC circuit. [8+8]

2. (a) Draw the basic circuit diagram of negative peak clamper circuit and explain its operation.

(b) What is meant by comparator and explain diode differentiator comparator operation with the help of ramp input signal is applied. [6+10]

3. (a) Define the following:

i. Storage time

ii. Delay time

iii. Rise time

iv. Fall time

(b) Explain how a BJT can be used as a switch. Compare its perfoemance as a switch with JFET. [8+8]

4. Write short notes on:

(a) Gate width of mono-stable multivibrator.

(b) Astable multivibrator as a voltage to frequency converter with circuit and waveform. [8+8]

5. (a) With the help of neat diagram explain the working of transistor Bootstrap time base generator.

(b) Draw a simple current sweep circuit and explain its working with the help of

diagrams. [16]

6. (a) Describe the sine wave frequency division with a sweep circuit.

(b) Compare sine wave synchronzation with pulse synchronization.

(c) What is Synchronization on one-to-one basis? [8+4+4]

7. (a) What is a sampling gate.

(b) Illustrate the principle of sampling gates with series and parallel switches and compare them.

(c) Draw the circuit diagram of unidirectional diode gate and explain its operation.[16]

8. (a) Draw the circuit diagram of diode - resistor logic OR gate and explain its operation.

(b) The transistor inverter (NOT gate) circuit has a minimum value hfe = 30, VCC = 12V, RC = 2.2k, R1 = 15k and R2 =100k, VBB = 12V. Prove that circuit works as NOT gate. Assume typical junction voltages. The input is varying between 0 and 12V. [16]

⋆ ⋆ ⋆ ⋆ ⋆

OBJECTIVE TYPE QUESTION BANK

---

1. When a square wave is given as input to a low pass RC circuit a reasonable reproduction of input is obtained if the rise time t_r is ---------- compared with pulse Width

a) Equal

b) Smaller

c) Not equal

d) Larger

2. The compensated attenuator will produce output signal which is ---------

a) Not same as input

b) Triple of input

c) Same as input

d) Double of input

3. The circuit which converts sinusoidal wave form into square under some special Condition is ----------

a) Dc restorer

b) Double ended clamper

c) Attenuator

d) Clamper

4. Under steady state the output is given by, when the circuit and input are as shown in the figure [c]

a) $V_o = V_i . V_m$

b) $V_o = V_i + V_m$

c) $V_o = V_i - V_m$

d) $V_o = V_i / V_m$

5. The reverse saturation current increases approximately for every ------- rise in Temperature

a) 30 c

b) 50 c

c) 70 c

d) 10 c

6) Zener diode has ---------- temperature coefficient

a) Sometimes positive and sometimes negative

b) Only NEGITIVE

c) Both positive and negative

d) Only positive

7. Turn off time of the transistor is =-------

a) $t_{off} = t_f + t_s$

b) $t_{off} = t_f + t_{on}$

c) $t_{off} = t_{fd} + t_s$

d) $t_{off} = t_{on} + t_s$

8. The V_{ce} of the n-p-n transistor is

a) -0.1v

b) 0.1v

c) 0.7 v

d) 0 v

9. The duration of quasi stable state of a Monoshot is-----

a) Fall gate

b) Gate time

c) Storage time

d) Recovery time

10. What is the name of the circuit which converts square wave in to spikes

a) Low pass RC

b) Bi stable multi

c) High pass RC

d) Monoshot

11. What is the response of step input to a high pass RC circuit

a) $V\ e^{-t/RC}$

b) $V\ (1- e^{t/RC})$

c) $V\ e^{t/RC}$

d) $V\ (1- e^{-t/RC})$

12. The response of the RC differentiator for the ramp input V_i=at is

a) RC

b) aC

c) aR

d) aRC

13. The semiconductor diode current equation is given by

a) $I=(1-e^{V/\ t}\ )$

b) $I=I_0\ (e^{1/nVt}\ -1)$

c) $I=I_0\ (e^{V/nVt}\ -1)$

d) $I=I_0\ (1-e^{1/nVt}\ )$

14. A comparator is a basic building block in a system used to analyze the --------

Distribution of noise generated in active device

a) Both frequency and phase

b) Amplitude

c) Phase

d) Frequency

15. The capacitance which appears across a reverse biased function of a diode is

called

a) Diffusion capacitance

b) Fixed capacitance

c) Transition capacitance

d) Valuable capacitance

16. Common base configurations is little used because

a) High voltage gain

b) High current gain

c) It has low input impedance

d) High input impedance

17. The V_{ce} (sat) of Si n-p-n transistor at 27 c is

a) 0.7 v

b) 0.3 v

c) 0.8 v

d) 0.1 v

18. The capacitor which assists the binary in making abrupt transition between states are called

a) delay

b) Storage

c) Commutating

d) Translation

19. Monostable vibrators generates

a) Pulse wave form

b) Ramp signal

c) Sine wave

d) Square wave

20. -------- Are basically regenerative circuits comprising of two cross coupled active devices

a)filters

b) Multivibrators

c) Attenuators

d) Clampers

21. The response of step input to a low pass RC circuit is

a)V $e^{-t/RC}$

b) V (1- $e^{t/RC}$)

c) V $e^{t/RC}$

d) V (1- $e^{-t/RC}$)

22. For DC input signal capacitor C acts as a

a) Open circuit

b) Short circuit

c) Both

d) None

23. Electron volt equivalent temp V_t =

a) T/1160

b) T/k

c) T/e

d) e/T

24. The breakdown occurring due to direct rupture of bonds because of existence of Strong electric field is

a)avalanche breakdown

b) Zener breakdown

c) Forward breakdown

d) None

25. Smallest times between two successive triggers is ----------

a) Restoring time

b) Storage time

c) Delay time

d) Rise time

26. If the transistor is indeed in saturation, the following condition must be satisfied

a) $i_C=i_B/h_{fe(min)}$

b) $i_B>i_C/h_{fe(min)}$

c) $i_B=i_C+Vce$

d) $i_B=i_C$

27. In a design of fixed bias binary $V_{CC}=V_{BB}=12v$,$h_{fe(min)}=20$, i_C sat=4 mA,assume n-p-n(Si) transistor then Rc is =

a) 2.925 kΩ

b) 200Ω

c) 0.5 kΩ

d) 100Ω

28. Expression of over shoot (d) of a Monoshot is

a) $d=Vcc-V_{BE(SAT)}$

b) $d=Vcc-I_B{}'R_{C1}-V_{CE(SAT)}$

c) $d=Vcc-I_B{}'R_{C1}$

d) $d=-Vcc+V_{BE(SAT)}$

29. No of quasi stable states of astable is

a) 1

b) 2

c) 3

d) 4

30. Schmitt trigger converts sine waves into

a) Square wave

b) Ramp

c) Cosine wave

d) Saw tooth

31. The percentage tilt in the response of a square wave input to a RC differentiator Circuit is given by

a) (T/2RC) X 100

b) (R/2TC) X 100

c) (RC/2T) X 100

d) (T/2TRC) X 100

32. The rise time of low pass RC circuit is given by

a) 2.2 RC

b) 30.2RC

c) 10 RC

d)20.2RC

33. Name the circuit which is used to convert analog into digital signal

a) Comparator

b) High pass filter

c) Low pass filter

d) Clamper

34. What is the current flowing through the capacitor when the voltage across the Capacitor is V

a) (1/C) dV/ dt

b) C (dV/dt)

c) (1/C) dI /dt

d) C (di/dt)

35. The following amplifier configuration yields the largest power gain

a) Emitter base

b) Common collector

c) Common base

d) Common emitter

36. The V_{BE}(Active) of n-p-n Si transistor at 25° c

a) 1 v

b) 2v

c) 0 v

d) 0.6v

37. The time required for the collector current to rise to 10 % of its maximum value in a transistor switch is called-------

a) Delay time

b) Fall time

c) Off time

d) On time

38. When the diode is forward biased it acts as

a) Inductor

b) Closed switch

c) Insulator

d) Open switch

39. The zener breakdown occurs at a electric field intensity of about

a)3×10^3 v/m

b)3×10^7 v/m

c)3×10^5 v/m

d)10×10^3 v/m

40. The V_{CE}(SAT) of n-p-n Ge transistor is

a) 0.7 v

b) 0 v

c) 0.1 v

d) -0.1 v

41. In the quasi stable state of Monoshot the transistor is

a) Q 1 OFF, Q2 ON

b) Q1 ON, Q2 ON

c) Q1 ON, Q2 OFF

d) Q1 OFF, Q2 OFF

42. The process of converting pulses into pips by means of a RC circuit is called

a) Peaking

b) Pulsing

c) Both

d) None

43. The output voltage V_o of RC differentiator for input V_i is

a) (RC) dVi/dt

b) (R) dVi/dt

c) (C) dVi/dt

d) RC

44. The clamping theorem is given by

a) $A_f/A_r=R_f/R$

b) $A_f/A_r=R_f/R_r$

c) $A_f/A_r=R_f$ x R

d) $A_f/A_r=1$

45. Usually the range of commutating capacitor is

a) 20 pf to 75 pf

b) 20 to 30 pf

c) 50 to 75 pf

d) 10 pf

46. Circuit which has only one permanently stable and one quasi stable state is called

a) Astable multi

b) Univibrator

c) Bistable multivibrator

d) Flip flop

47. The time period of a stable multi is T=

a) 1.3 RC

b) 1.38 RC

c) 1 RC

d) 2 RC

48. In RC integrator circuit the output is taken across

a) resistor

b) Transistor

c) Diode

d) Capacitor

49. The forward resistance of an ideal diode is

a) 10 MΩ

b) 0

c) 20 Ω

d) infinite

50. Thermal runaway in a transistor biased in the active region is due to

a) V_{CE}(SAT)

b) Output voltage

c) Input voltage

d) Change in reverse saturation current due to rise in temp

51. If the V_{CB} of n-p-n transistor of CE configuration is negative then the transistor is in

a) Cut off

b) Saturation

c) Inverted

d) active

52. One shot is also known as

a) Single cycle

b) Monostable multi

c) Univibrator

d) all of the above

53. The hysteresis in a Schmitt trigger circuit can be eliminated by making loop gain

a) =1

b) >1

c) <1

d) =0

54. The revere resistance of a ideal diode =

a) 10 Ω

b) 0

c) 20MΩ

d) infinite

55. The capacitance which appears across a reverse biased junction of a diode is called

a) Fixed capacitance

b) Variable capacitance

c) Diffusion capacitance

d) Transition capacitance

56. If the V_{CB} of n-p-n transistor in CE configuration is negative when the transistor is in

a) Active region

b) Cut off region

c) Saturation region

d) Inverted

57. The binary is sometimes referred to as

a) Norton's circuit

b) Eccless Jordon circuit

c) Thevinins circuit

d) Millimans circuit

58. At very high frequency the capacitor acts almost as a---------

a) Inductor

b) Short circuit

c) Resistor

d) Open circuit

59. The total charge in the body of a semiconductor

a) Both positive and negative

b) Positive

c) Negative

d) zero

60. The collector to emitter breakdown voltage with base not open circuit is BV_{CER} is given by

a) BV_{CBOnv} $(1-I_{CO}R_B/V?)$ b) BV_{CEOv} $(1-I_{CO}R_B/V?)$

c) BV_{CBOv} $(1-I_{CO}R_B/V?)$

d) BV_{CEOnv} $(1-I_{CO}R_B/V?)$

61. The circuit which is used to reduce amplitude of the signal is

a) Attenuator

b) Clamper

c) Clipper

d) Insulator

62. the negative clamper is also called

a) Positive peak clamper

b) Negative peak clamper

c) Positive peak clipper

d) Negative peak clipper

63. In the diode the time required for minority charge carriers to move into the other side of the PN junction and become majority charge carrier is called

a) Delay time

b) Transition time

c) Reverse recovery time

d) Storage time

64.Which of the following is linear circuit

a) FET

b) Resistor

c) Diode

d) Transistor

65. What is the value of damping factor k of RLC circuit for critical damping condition

a) k=10 b) k>10 c) k>20
d) k=1

66. A large signal approximation which often leads to a sufficient accurate solution is the ---------- representation

a) Ebers model

b) Hybrid model

c) Pi model

d) Piecewise linear

67. At small and moderate currents h_{FE} increases with

a) Decrease with temperature

b) Decrease of input voltage c) Increase of input voltage d) Increase of temperature

68. Find the value of collector resistor in a collector coupled stable multi for the following specifications f=10 KHZ ,Vcc=9 V, $i_{c(max)}$ =2 mA,h_{fe}=20

a) 1O

b) 4.35 KO

c) 3 KO d) 2KO

69. If the damping factor k of RLC circuit is less than unity then circuit is called ------ -----damping circuit

a) Under

b) Over

c) Critical

d) Under damped

70. The maximum reverse biasing voltage which may be applied before breakdown Between collector and base terminals is

a) BV_{CEO}

b) V_{CE}

c) V_{CB}

d) BV_{CBO}

71. Which of the following is the advantage of emitter coupled over collector coupled Multivibrator

a) Inherently self starting

b) Low power dissipation

c) Less noisy

d) Only one trigger signal is enough

72. No of triggers required for monostable multi to change from stable state to quasi Stable state and vice versa

a) 1

b) 2

c) 3

d) 4

73. The RLC circuit which gives nearly undamped oscillations is called --------- circuit

a) Clipping

b) Clamping

c) Coupling

d) Ringing

74. The disadvantage of shunt clipper

a) Round shaped edges of input waveform

b) No transmission of signal

c) Transmits same signal

d) Doubles amplitude of input waveform

75. Monostable multi vibrators generates

a) Square

b) Pulse

c) Sine

d) Ramp

76. The base width in a junction transistor is deliberately chosen small so that

a) The concentration of injected carrier is small

b) The majority carriers easily reaches the collector

c) The electric field s large

d) To reduce the recombination of injected minority carriers

77. A circuit which can indefinitely exist in either of two stable state and which can be Induced to make abrupt transition from one state to other by means of external Excitation

a) Monoshot

b) Oscillator

c) binary

d) Attenuator

78. The schmit trigger can be used as a

a) Filter

b) Attenuator

c) Comparator

d) Clamper

79. When does the transistor act as a closed switch

a) Both junctions are forward biased

b) Input junction is reverse biased and output junction is forward biased c) input junction is forward biased and output junction is reverse biased

d) Both junctions are reverse biased

80. When does the transistor act as open switch

a) Input junction is reverse biased and output junction is forward biased

b) Both junctions are forward biased

c) Both junctions are reverse biased

d) Input junction is forward biased and output junction is reverse biased

81. Transiton capacitance of diode is given as

a) $?^n/(VB)^3$

b) ?/(VB)^{n}

c) n)/VB n

d) (VB) /?

82. At constant base and collector current forward B-E voltage has typical Temperature sensitivity in the range of

a) -7.5 m V /c to -8.0 m V /c

b) -1.5 V /c to -2. m V /c

c) 1.5m V /c to -2 m V /c

d) -7.5 m V /c to 8.0 m V /c

83. Gain of integrator decreases with ---------- frequency

a) Increase

b) Constant

c) Low

d) Decreases

84. Time constant or RLciruit

a) R/L

b)R+L

c) RL

d) L/R

85. The application of voltage comparator

a) ohm meter

b) Voltmeter

c) Ammeter

d) Phase meter

86. For an ideal p-n junction diode the current $I=I_0 (e^{V/?Vt} -1)$ than what is the value ? for Ge

a)5

b) 15

c) 1

d) 10

87. A stable state of binary is one in which the current and voltages satisfy kirrchofs Laws and are constant and the condition satisfied that loop gain is

a) =1

b) <1

c) >>1

d) >1

88. In a transistor leakage current mainly depends on

a) temperature

b) minority carriers

c)concentration of majority carriers

d) none of the above

89. The commutating capacitor are also called

a) speed up capacitor

b) varicap

c) tuning capacitor

d) delay capacitor

90. If VTP=5.12 and LTP =3.312 then the value of hysterisis in schimmit trigger is

a) 1.81 V b) 5.4 V

c) 4.8 V d) 3.2V

91. The condition for perfect compensation of an attenuator

a) $R_1C_1=R_2C_2$

b) $R_1C_1=R_2$

c) $R_1=R_2$

d) none

92. Which of the following is the fastest switching device?

a) MOSFET

b) DIODE

c) JFET

d)BJT

93. The pulse width or gate width of Monoshot is

a) RC

b) 2 RC

c) 0.69 RC