Mrs.D.Sudha

Personal Information

Designation: Associate Professor
Qualification:M.tech.,(Ph.D).,
Experience: 8 years
Specialization: VLSI DESIGN
Date of Joining: 1-12-2018
Phone Number: +91 9885735866
E-mailId :sudha.phd2015@gmail.com

Achievements/Publications/workshops/Seminars/Guest Lectures

Publications:

1. cessing in Embedded Systems Using Multidimensional Retiming", International Journal of Advanced Engineering Technology / Vol.II / Issue II/April-June, 2011/239-244. 1. Sudha, D.; Ch.Santhirani , Sreenivasa Rao Ijjada,"High Performance and Low Leakage 3DSOI Fin-FET SRAM", **Scopus Indexed Journal** (**scince publications**) Sudha, D. *et al*. / American Journal of Engineering and Applied Sciences 2017, vol:10 (1),pages: 101.107 **DOI: 10.3844/ajeassp.2017.101.107**
2. Sudha D, Ch.Santhirani ," Design of low leakage power SRAM using Multithreshold technique", International Journal of Applied Engineering Research IJAER (**Scopus Indexed Journal**), Vol.10, Issue.23 year:August 2015, pages. 43549-43554, H index-9, SJR-0.13.
3. Sudha, D.; Ch.Santhirani , Sreenivasa Rao Ijjada,"Analysis of Sub-threshold Inverter and 6T SRAM Cell for Ultra-Low-Power Applications" © **Springer Nature Singapore Pte Ltd. 2018** R. Singh et al. (eds.), Intelligent Communication, Control and Devices, Advances in Intelligent Systems and Computing vol: 624, year -2008,pages:1401-1413. https://doi.org/10.1007/978-981-10-5903-2_147.
4. Sudha, D.; Ch.Santhirani , Sreenivasa Rao Ijjada," SOI Fin-FET 10T SRAM against Short Channel Effects",(**scince citation index**) polish academy of scinces institute of physics established in 1920 by polish physical scocity Poland,turcky.(**Accepted**)
5. Sudha, D.; Ch.Santhirani," ANALYSIS FOR LOW POWER 90NM NOVEL 10TSRAM**",** journal of advanced research in dynamical and control

systems**”(JARDCS)Elsevier Scopus- Indexed FREE Journal. Vol. 10, Special Issue-07, 2018 pages: 573-581.**

6. Sudha, D.; Ch.Santhirani,” Implementation of New Architecture for low leakage- low power-low area and robust SRAM cell design for computer and communication applications”, journal of advanced research in dynamical and control systems**” (JARDCS) Elsevier Scopus- Indexed FREE Journal . Vol. 10, Special Issue-07, 2018 pages: 563-571.**
7. D.Sudha, Ch.Santhirani.” High Speed Drain Gating Ground Bounce Technique for Arithmetic Circuits to reduce Leakage Power**”, (JARDCS)Elsevier Scopus- Indexed FREE Journal. Vol. 10, Special Issue-07, 2018 pages: 590-596.**
8. Sreenivas Rao ijjada, D.Sudha, Ch.SanthiRani “Effcient low Leakage Novel 10T SRAM Cell Architecture”vol.no.6, issue no 01,Januvary 2017. Pages:103-108.
9. D.Sduha ,2G.V.subbareddy, “CMOS Digital Based Technology for Static Power Reduction in Nanoscale Circuits”, International Journal of Research in Information Technology,(**IJRIT**) Volume 2, Issue 9, September 2014, Pg. 18-21.

Conferences:

1. Sudha, D.; Ch.Santhirani , Sreenivasa Rao Ijjada, “FinFET- One Scale up CMOS: Resolving Scaling Issues” 3rd International Conference on computing for sustainable global development (INDIAcom) Bharati Vidyapeeth's Institute of Computer Applications and Management (BVICAM), New Delhi (INDIA), year: 2016, pages 1183-11879. DOI:78-9-3805-4421-2/16/$31.00_c 2016 IEEE.
2. Sudha, D.; CH.SanthiRani, “SCPG:A new technique to redeuce leakage power in 16-bit binary multiplier”,Computational Intelligence and Computing Research (ICCIC), 2014 IEEE International Conference on Year: 2014 Pages: 1 - 7, DOI: 10.1109/ICCIC.2014.7238.

National Workshops:

1. Five Days National workshop on “VLSI & FPGA SIGNAL PROCESSING” organized by the dept.of electronics and communication engineering,. NIT-WARANGAL AND GITAM Deemed To Be University, AP,India. During 2nd - 7th , May 2018.

2. Five Days National workshop on “Low power system on chip design using XILINX FPGA Devices”. organized by the dept.of electronics and communication engineering,. NIT-WARANGAL, AP,India. During 3rd - 7th , October 2015.
3. One month online course IIT-BOMBAYX WHS791X Technical communication for Scientist and Engineers workshop, Course started oct-08 to Dec 5th at GRIET Hyd.

4. Two Day National Workshop Hands on Faculty Development Program me on software define radio”, organized during 16&17th December-2015 by the dept. of Electronics and communication Engineering, GRIET, Hyderabad..
5. WASA-2006(Workshop on Advances in sensors and Applications) GITAM college of Engineering, Visakhapatnam, AP, India- Dec 22nd &23rd 2011
6. Two day National Workshop on VLSI Embedded systems GRIET, HYD, , India - Feb 17th b&18th 2015.

Workshops/Short term courses organized

1. Two day national work shop on CADENCE tools ,GRIET.
2. Two day national work shop on “High speed VLSI circuit design”, GRIET, Feb 7th & 8th 2014.

Professional experience:

SKILLS

1. Knowledge of CADENCE,TCAD software

2. Knowledge of Simulation Softwares – Silvaco ATLAS, HSPICE, Modelsim, Xilinx, MATLAB, Simulink, dSPACE.

3. Knowledge of Hardware descriptive languages and kits – VHDL, Verilog HDL and FPGA and CPLD Kits.

4. Knowledge of programming Languages- ‘C’
5. Knowledge of Operating systems – Windows, Linux.