Mr. G. Rajesh Kumar

Personal Information

Designation: Assistant Professor

Qualification: M.Tech.

Experience: 4 years

Specialization: VLSI Design

Date of Joining: 19-09-2018

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Achievements/Publications/workshops/Seminars/Guest Lectures

Publications:

1. G. Rajesh Kumar and K. Babulu, "March Based Low Power MBIST Architecture for SRAM" International Journal of modern Electronics and Communication Engineering, Vol 6, Issue 4, 2018, pp. 49-53
2. G. Rajesh Kumar and K. Babulu, "Design and performance analysis of low power SRAM using modified MTCMOS" ARPN Journal of Engineering and Applied Sciences, Vol 13, Issue 14, 2018, pp. 4260-4265
3. G. Rajesh Kumar and K. Babulu, "Low Power March Memory Test Algorithm for Static Random Access Memories" *IJE Transactions B: Applications,* Vol. 31, Issue 2, 2018, 292-298
4. J. Ravi and G. Rajesh Kumar, "Image Fusion Algorithm Implementation Using Laplacian Pyramid" *International Journal of Scientific Progress and Research,* Vol 29, Issue 83, 2016, pp. 103-107
5. N. Veera Durga, G. Rajesh Kumar and PVS Muralidhar, Design and VLSI Implementation of Efficient Discrete Wavelet Transfer Scheme, "International Research Journal of Engineering and Technology", vol. 3, issue 8, 2016, pp. 109-116.
6. G. Rajesh Kumar and K. Babulu, "A Novel Architecture for Scan Cell in Low Power Test Circuitry", *Elsevier Procedia Materials Science* 10, 2015, pp. 403-408.
7. D. Viswabharathi, G. Rajesh Kumar, and K. Raghuram, "High Speed Test Architecture for SRAM using Modified March Algorithm", *International Journal of Engineering Research and Applications,* Vol. 2, Issue 6, 2012, pp. 1654-1659.

8. E. L. K. Priya, G. Rajesh Kumar and P. Lakshmi Sarojini, "Area Efficient Fixed Width Modified Booth Multiplier", *International Journal of Engineering Research & Technology* Vol. 1 Issue 8, 2012.
9. M. Radha Rani, G. Rajesh Kumar and A. Karna Rao, "Effective Estimation of Peak-Power for a Testable Digital Circuit", *International Journal of Advanced Research in Computer Engineering & Technology* Vol 1, Issue 7, 2012, pp. 125-129.
10. B. Sreenivasa Ganesh, G. Rajesh Kumar and J. E. N. Abhilash, "Design and Implementation of Floating Point Multiplier for Better Timing Performance" *International Journal of Advanced Research in Computer Engineering & Technology* Vol 1, Issue 7, 2012, pp. 130-136.

International and National Conferences

- Research paper titled, "VLSI Implementation of Second Generation Run Length Encoding Scheme for High Speed Data Transmission", presented in International Conference on Emerging Multidisciplinary Research and Computational Intelligence 2016 at SRKR Engineering College, Bhimavaram.
- Research paper titled, "March Algorithm Based MBIST Architecture for SRAM", presented in IETE national conference 2012 at NSTL, Vizag.

Faculty Development Programme, Workshop and seminars

- Participated one-week FDP on Recent Trends in VLSI Design and its Applications at SRKR engineering college, Bhimavaram, held from 20/11/2017 to 25/11/2017.
- Participated one-week FDP on Signal and Image processing with MatLab at SRKR engineering college, Bhimavaram, held from 03/07/2017 to 08/07/2017.
- Participated two-day national seminar on Assistive technology at Shri Vishnu Engineering College for Women, Bhimavaram, held from 23/07/2016 to 24/07/2016.
- Participated one-week FDP on Research Challenges in VLSI Design and Testing at Coimbatore Institute of Technology, Coimbatore, held from 08/12/2014 to 14/12/2014.
- Participated five-day FDP on VLSI Design Methodology using Mentor Graphics Tools at JNTUH, Hyderabad, held from 19/08/2010 to 23/08/2010.