CMR COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution)

ACADEMIC REGULATION R02
FOR CBCS BASED M. TECH. (REGULAR) DEGREE PROGRAMMES

(Applicable for the students of M. Tech. programme admitted into I year from Academic Year 2015-16 and onwards)

1.0 Eligibility for Admissions

Admission to the above program shall be made subject to eligibility, qualification and specialization as prescribed by Government of Telangana State from time to time.

Admission shall be made on the basis of merit/rank obtained by the candidates at the qualifying Entrance Test conducted by the Government of Telangana or on the basis of any other order of merit as approved by the University, subject to reservations as laid down by the Government from time to time.

2.0 Award of M. Tech. degree

2.1. A student shall be declared eligible for the award of the M. Tech. Degree, if he pursues a course of study in not less than two and not more than four academic years. However, he is permitted to write the examinations for two more years after four academic years of course work, failing which he shall forfeit his seat in M.Tech programme.

2.2. The M. Tech. degree of Jawaharlal Nehru Technological University Hyderabad shall be conferred on candidates who are admitted to the program and who fulfil all the requirements for the award of the degree.

2.3 The student shall register for all 88 credits and secure all the 88 credits.

2.4 The medium of instruction and examination shall be English.

3.0 A. Courses of Study

The following specializations are offered at present for the M. Tech. course of study.

1. Embedded Systems
2. Power Electronics
3. Structural Engineering
4. Computer Science & Engineering

and any other course as approved by the College/ University/AICTE from time to time.

B. Departments offering M.Tech. programmes with specializations mentioned below:

Sl. No.	Department	M.Tech Course
1	ECE	Embedded Systems
2	EEE	Power Electronics
3	Civil	Structural Engineering
4	CSE	Computer Science & Engineering

4.0. Course Registration

4.1. A 'Faculty Advisor or Counselor' shall be assigned to each student, who will advise him about the PG Programme, its Course Structure and Curriculum, Choice/Option for Courses, based on his

competence, progress, pre-requisites and interest.

4.2. Academic Section of the College invites 'Registration Forms' from students within 15 days from the commencement of class work through 'ON-LINE SUBMISSIONS', ensuring 'DATE and TIME Stamping'. The ON-LINE Registration Requests for any 'CURRENT SEMESTER' shall be completed BEFORE the commencement of SEEs (Semester End Examinations) of the 'PRECEDING SEMESTER'.

4.3. A Student can apply for ON-LINE Registration, ONLY AFTER obtaining the 'WRITTEN APPROVAL' from his Faculty Advisor, which should be submitted to the College Academic Section through the Head of Department (a copy of the same being retained with Head of Department, Faculty Advisor and the Student).

4.4. If the Student submits ambiguous choices or multiple options or erroneous entries - during ON-LINE Registration for the Course(s) under a given/ specified Course Group/ Category as listed in the Course Structure, thereby causing discrepancy, the decision of Head of the Department shall be final.

4.5. Course Options exercised through ON-LINE Registration are final and **cannot** be changed /inter-changed; further, alternate choices will also not be considered. However, if the Course that has already been listed for Registration (by the Head of Department) in a Semester could not be offered due to any unforeseen or unexpected reasons, then the Student shall be allowed to have alternate choice - either for a new Course (subject to offering of such a Course), or for another existing Course (subject to availability of seats), which may be considered. Such alternate arrangements will be made by the Head of Department, with due notification and time-framed schedule, within the **first week** from the commencement of Class-work for that Semester.

5.0. Attendance

The programs are offered on a unit basis with each course t being considered a unit.

5.1 The minimum instruction period for each semester shall be 90 clear instruction days.

5.2. A student shall be eligible to write semester end examinations **of a course** if he acquires a minimum of 75% of attendance **in that course.**

5.3. Condonation of shortage of attendance in each Course up to 10% (65% and above and below 75%) in each semester may be granted by the Institute Academic Committee on valid medical reasons.

5.4. Shortage of attendance below 65% shall not be condoned.

5.5. Students whose shortage of attendance is not condoned in any semester **for a course(s)** are not eligible to write their end semester examination of **those** courses and their registration **for these courses** shall stand cancelled. **They have to register for these courses later when offered.**

5.6. A fee as prescribed by the Institute Academic Committee shall be payable towards condonation of shortage of attendance.

5.7. A candidate shall put in a minimum required attendance, in at least 3 theory Courses in I semester for promoting to II semester.

5.8. In order to qualify for the award of the M. Tech. Degree, the candidate shall complete all the academic requirements of the courses, as per the course structure.

5.9. A student shall not be promoted to the next semester unless he satisfies the attendance requirement of the present semester as applicable. They may re-register for the semester when offered next. If a candidate fulfils the attendance requirement in the present semester, he shall not be eligible for re-registration into the same class.

6. Evaluation

6.1. The performance of the candidate in each semester shall be evaluated Course-wise, with a maximum of 100 marks for theory and 100 marks for practicals, on the basis of Internal Evaluation and Semester End Examination.

6.2. For the theory courses 70 marks shall be awarded based on the performance in the Semester End Examination and 30 marks shall be awarded based on the Internal Evaluation. For internal evaluation there shall be the two internal examinations conducted-one in the middle of the semester and the other immediately after the completion of instruction period. Each internal examination shall be conducted for a total duration of 120 minutes. The final marks secured by the student in 'internal evaluation' for the semester are arrived at by giving a weightage of 70% to the best secured 'internal examination' and 30% weightage to the least secured 'internal examination'. A student who is absent for any internal examination for any reason what so ever shall be deemed to have secured 'zero' marks in the test/ examination and no make-up test/ examination shall be conducted.

6.3. Question paper pattern for evaluation

Internal Examination

Part A (10 Marks)

5 questions of 2 marks each (All questions are compulsory).

Part B (20 Marks)

4 questions to be answered out of 6 questions, each question carries 5 marks.

External Examination

Part A (20 Marks)

5 questions (1 question from each unit) of 4 marks each (Compulsory questions)

Part B (50 Marks)

5 questions (1 question from each unit with internal choice) each question carries 10 marks.

6.4. For practical courses, 70 marks shall be awarded based on the performance in the End Semester Examinations. 30 marks shall be awarded for day to day performance in the practicals as internal marks.

6.5. Laboratory end examination for M. Tech. courses for 70 marks must be conducted with two Examiners, one of them being the Laboratory Course Teacher and the second examiner shall be external examiner. External Examiner shall be appointed by the Controller of Examinations from other institutions or industry.

6.6. There shall be seminar presentation during I semester as well as II semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Departmental Academic Committee consisting of Head of the Department, Supervisor and two other senior faculty members of the department. For each Seminar there will only be internal evaluation for 50 marks. A candidate has to secure for each seminar a minimum of 50% of maximum marks to be declared successful. If he fails to secure minimum marks, he has to re-appear during the supplementary examinations.

6.8. There shall be a Comprehensive Viva-Voce in III Semester. The Comprehensive Viva-Voce is intended to assess the student's understanding of various Courses during the M.Tech course of study. The Viva-Voce will be conducted by a Committee consisting of Head of the Department, two Senior Faculty members of the Department. The Comprehensive Viva-Voce is evaluated for 100 marks by the Committee. There are no internal marks for the Comprehensive Viva-Voce. A candidate has to secure a minimum of 50% of marks to be declared successful.

6.9. A candidate shall be deemed to have secured the minimum academic requirement in a course if he secures a minimum of 40% marks in the End semester Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

6.10. In case the candidate does not secure the minimum academic requirement in any course (as specified in 6.9) he has to reappear for the Semester End Examination in that course.

6.11. A candidate shall be given one chance to re-register for the Courses if the internal marks secured by a candidate are less than 50% and has failed in the end examination. In such a case, the candidate must re-register for the Course(s) and secure the required minimum attendance. The candidate's attendance in the re-registered Course(s) shall be calculated separately to decide upon his eligibility for writing the end examination in those Courses(s). In the event of the student taking another chance, his internal marks and end examination marks obtained in the previous attempt stand cancelled.

6.12. In case the candidate secures less than the required attendance in any course, he shall not be permitted to write the End Examination in that course. He shall re-register the course when next offered.

7. Examinations and Assessment – The Grading System

7.1 Marks will be awarded to indicate the performance of each student in each Theory Course or Lab/Practical, or Seminar, or Project, et., based on the % marks obtained in CIE + SEE (Continuous Internal Evaluation + Semester End Examination, both taken together) as specified in item 6 above, and a corresponding Letter Grade shall be given.

7.2 As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades (UGC Guidelines) and corresponding range of percentage of marks shall be followed:

% of Marks Secured (class intervals)	Letter Grade (UGC Guidelines)	Grade Points
80% and above ($\geq 80\%, \leq 100\%$)	**O (Outstanding)**	**10**
Below 80% but not less than 70% ($\geq 70\%, <80\%$)	**A^+ (Excellent)**	**9**
Below 70% but not less than 60% ($\geq 60\%, <70\%$)	**A (Very Good)**	**8**
Below 60% but not less than 55% ($\geq 55\%, <60\%$)	**B^+ (Good)**	**7**
Below 55% but not less than 50% ($\geq 50\%, < 55\%$)	**B (above Average)**	**6**
Below 50% ($< 50\%$)	**F (FAIL)**	**0**
Absent	**AB**	**0**

7.3 A student obtaining 'F' Grade in any Course shall be considered ' failed ' and is required to reappear as 'Supplementary Candidate' in the Semester End Examination (SEE), as and when offered. In such cases, his Internal Marks (CIE Marks) in those Courses will remain the same as those he obtained earlier.

7.4 A student not appeared for examination the 'AB' Grade will be allocated in any Course shall be considered 'failed' and will be required to reappear as 'Supplementary Candidate' in the Semester End Examination (SEE), as and when offered.

7.5 A Letter Grade does not imply any specific Marks percentage and it will be the range of marks percentage.

7.6 In general, a student shall not be permitted to repeat any Course (s) only for the sake of 'Grade Improvement' or 'SGPA/CGPA Improvement'

7.7 A student earns Grade Point (GP) in each Course, on the basis of the Letter Grade obtained by him in that Course. The corresponding 'Credit Points '(CP) are computed by multiplying, the Grade Point with Credits for that particular Courses.
Credit Points (CP) = Grade Point (GP) x Credit … For a Course.

7.8 The Student passes the Course only when he **gets GP ≥ 6 (B Grade or above)**

7.9 The Semester Grade Point Average (SGPA) is calculated by dividing the Sum of Credit Points (∑CP) secured from All Courses registered in a Semester, by the Total Number of Credits registered during that Semester. SGPA is rounded off to TWO Decimal Places, SGPA is thus computed as.

SGPA = $\{ \sum^{N}_{i=1} C_i G_j \} / \{ \sum^{N}_{i=1} C_i \}$ ….For each Semester.

Where 'i' is the Course indicator index (takes into account all Courses in a Semester), 'N' is the no. of Courses 'REGISTERED' for the Semester (as specifically required and listed under the Course Structure of the parent Department), C_i is the no. of Credits allotted to the i^{th} Course, and G_i represent the Grade Points (GP) corresponding to the Letter Grade awarded for that i^{th} Course.

7.10. The Cumulative Grade Point Average (CGPA) is measure of the overall cumulative performance of a student over all Semesters considered for registration. The CGPA is the ratio of the Total Credit Points secured by a student in All registered Courses in All Semesters, and the Total Number of Credits registered in All the Semesters. CGPA is rounded off to TWO Decimal Places. CGPA is thus computed from the I Year Second Semester onwards, as the end of each Semester, as per the formula.

CGPA = $\{\sum^{M}_{j=1} C_j G_j \} / \{\sum^{M}_{j=1} C_j\}$ } …. For all S Semester registered
{ it., upto and inclusive of S Semester, S ≥2).

Where 'M' is the TOTAL no. of Subject (as specifically required and listed under the Course Structured of the parent Department) the Student has 'REGISTERED' from the 1st Semester onwards upto and inclusive of the Semester S (Obviously M > N), 'j ' is the Subject indicator index (takes into account all Courses from 1 to S Semesters),C_j is the no. of Credits allotted to the j^{th} Courses from G_j represent the Grade Points (GP) corresponding to the Letter Grade awarded for the j^{th} Course. After registration and completion of II Semester however, the SGPA of that Semester itself may be taken as the CGPA, as there are no cumulative effects.

7.11. For Calculations listed in item 7.6 – 7.10, performance in failed Courses (securing F Grade) will also be take into account, and the credits of such Courses will also be included in the multiplications and summations.

7.12. For Calculations listed in item 7.6 – 7.10, performance in failed Courses (Securing F Grade) will also be taken into account, and the Credits of such Courses will also be included in the multiplication and summations.

8 .**Evaluation of Project/Dissertation Work**

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

8.1 A Project Review Committee (PRC) shall be constituted with Head of the Department as Chairperson, Project Supervisor and one senior faculty member of the Department offering the M.Tech programme as members.

8.2 Registration of Project Work: A Candidate is permitted to register for the project work after satisfying the attendance requirement of all the courses, both theory and practical of I year.

8.3 After satisfying 8.2, a candidate has to submit, in consultation with his project Supervisor, the title, objective and plan of action of his project work to the PRC for approval. Only after obtaining the approval of the PRC the student can initiate the Project work.

8.4 If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the PRC. However, the PRC shall examine whether or not the changes of topic/supervisor leads to a major changes of his initial plans of project proposal. If yes his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

8.5 A candidate shall submit his project status report in two stages at least with a gap of 3 months between them.

8.6 The work on the project shall be initiated at the beginning of the III semester and the duration of the project is two semesters. A candidate is permitted to submit Project Thesis only after successful completion of all theory and practical courses with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Head of the Department and make an oral presentation before the PRC.

8.7 After approval from the PRC, the soft copy of the thesis should be submitted to the College for ANTI-PLAGIARISM check and the plagiarism report should be included in the final thesis. If the result of above check is less than 24%, then only thesis will be accepted for submission.

8.8. Three copies of the Project Thesis certified by the supervisor shall be submitted to the College.

8.9 For Project Work Review-I will be conducted in III Semester and carries a maximum internal marks of 50. The evaluation should be done by the PRC for 25 marks and Project Supervisor for 25 marks. The Supervisor and PRC will examine the Literature Survey in the same domain, Problem Definition, Objective, Scope of Work**.** A candidate has to secure a minimum of 50% of marks to be declared successful in Project Work Review I. If he fails to secure minimum required marks he has to reappear during the supplementary examination.

8.10. Project Work Review II in IV Semester carries 50 internal marks. The evaluation should be done by the PRC for 25 marks and the Project Supervisor for 25 marks. The PRC will examine the overall progress of the Project Work and decide the eligibility of the Project for final submission. A candidate has to secure a minimum of 50% of marks to be declared successful in Project Work Review II. If he fails to fulfill minimum marks, he has to reappear for Review-II during the supplementary examination.

8.11 The thesis shall be adjudicated by the committee consisting of one senior faculty selected by the Head of the Department, the guide concerned, Head of the Department and external examiner.

8.12 If the report of the committee is not favourable, the candidate shall revise and resubmit the Thesis. If the report of the committee is unfavourable again, the thesis shall be summarily rejected.

8.13. For Project Work Evaluation (Viva Voice) will be conducted on acceptance of the Thesis in IV Semester. This is an external evaluation for 150 marks and will be evaluated by the committee. The External Examiner for the committee shall be appointed by the Controller of Examinations. The candidate has to secure minimum of 50% marks in Project Evaluation (Viva Voice) examination for its successful completion.

8.14. If he fails to secure minimum marks as specified in 8.13, he will reappear for the Viva Voice examination only after three months. In the reappeared examination also if the candidate fails to secure minimum prescribed marks the registration for the programme stands cancelled and he will not be eligible for the award of the degree.

8.15. The Head of the Department shall coordinate and make arrangements for the conduct of Project Viva Voice examination.

9. Award of Degree and Class

9.1 A Student who registers for all the specified Courses as listed in the Course Structure, satisfies all the Course Requirements, and passes the examinations prescribed in the entire PG Programme (PGP), and secured the required number of **88** Credits (with CGPA $\geq$ 6.0), shall be declared to have 'QUALIFIED' for the award of the M.Tech. Degree in the chosen Branch of Engineering and Technology, with the specialization for which he took admission.

9.2 Award of Class

After a student has satisfied the requirements prescribed for the completion of the programme, becomes eligible for the award of M.Tech. Degree, he shall be placed in one of the following three classes based on the CGPA.

Class Awarded	CGPA
First Class and Distinction	$\geq$ 7.75
First Class	6.75 $\leq$ CGPA > 7.75
Second Class	6.00 $\leq$ CGPA < 6.75

9.3 A student with final CGPA (at the end of the PGP) < 6.00 will not be eligible for the Award of Degree.

10. Withholding of Results

If the student has not paid the dues, if any, to the institution or if any case of indiscipline is pending against him, the result of the student will be withheld and he will not be allowed into the next semester.

11. General

11.1. Wherever the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”, “hers”.

11.2. The academic regulation should be read as a whole for the purpose of any interpretation.

11.3. In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Academic Council is final.

11.4. The college may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the college.

MALPRACTICES RULES
DISCIPLINARY ACTION FOR
IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/ Improper conduct	**Punishment**
1.(a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other Courses the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the Courses of that Semester/year. The Hall Ticket of the candidate is to be cancelled.
3.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the Courses of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the Remaining Courses of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all end semester examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4.	Smuggles the answer book or	Expulsion from the examination hall

	additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination	and cancellation of performance in that subject and all the other Courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the Courses of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all end semester Examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks	Cancellation of the performance in that subject
6.	Refuses to obey the orders of the Chief Superintendent/Assistant– Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the college or organizes a walk out or instigates others **to** examination hall walk out, or threatens the officer- in-charge or any person on duty in or outside the examination hall of any injury**,** to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer- in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other Courses the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the Courses of that semester/year. The candidates are also debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other Courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the

		Courses of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other Courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the Courses of that semester/year. The candidate is also debarred and forfeits the seat.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	If the student belongs to the college, expulsion from the examination hall an cancellation of performance in that subject and all other Courses hall and all other Courses that candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the Courses of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other Courses the candidate has already appeared including practical examinations and project work and shall not be permitted for other remaining examinations of the Courses of that semester/year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other Courses the candidate has appeared including practical examinations and project work of that semester/year.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the College Academic Committee for further action to award suitable punishment.	

Malpractices identified by squad or special invigilators

Punishments to the candidates as per the above guidelines.

Malpractice identified at Spot center during valuation

The following procedure is to be followed in case of malpractice cases detected during valuation, scrutiny etc. at spot center.

1) Malpractice is detected at the spot valuation. The case is to be referred to the malpractice committee. Malpractice committee will meet and discuss/question the candidate and based on the evidences, the committee will recommend suitable action on the candidate.

2) A notice is to be served to the candidate(s) involved through the Principal to his address and to the candidate(s) permanent address regarding the malpractice and seek explanations.
3) The involvement of staff who are in charge of conducting examinations, invigilators valuing examination papers and preparing / keeping records of documents relating to the examinations in such acts (inclusive of providing incorrect or misleading information) that infringe upon the course of natural justice to one and all concerned at the examinations shall be viewed seriously and recommended for award of appropriate punishment after thorough enquiry.
4) Based on the explanation and recommendation of the committee, action may be initiated.
5) **Malpractice committee:**

i.	Controller of Examinations	Chairman
ii.	Assistant controller of Evaluation	Member
iii.	Chief Examiner of the subject/ subject expert	Member
iv.	Concerned Head of the Department	Member
v.	Concerned Invigilator	Member

CMR COLLEGE OF ENGINEERING & TECHNOLOGY

(AUTONOMOUS)
DEPARTMENT OF ECE

EFFECTIVE FROM ACEDEMIC YEAR 2015-16
R02 COURSE STRUCTURE AND SYLLABUS FOR M.Tech (EMBEDDED SYSTEMS)

I Semester			Title	L	P	C
CODE		Group				
1	B2201	CC	Microcontrollers for Embedded System Design	4	--	4
2	B2202	CC	Embedded Real Time Operating Systems	4	--	4
3	B2203	CC	Embedded C	4	--	4
4		PE	Professional Elective –I	4	--	4
5		PE	Professional Elective –II	4	--	4
6		OE	Open Elective -I	4	--	4
7	B2204	CC	Embedded C Laboratory	--	4	2
8	B2205	PW	Seminar	--	4	2
Total				24	8	**28**

II Semester			Title	L	P	C
CODE		Group				
1	B2206	CC	Hardware Software Co-Design	4	--	4
2	B2207	CC	Embedded System Design	4	--	4
3	B2208	CC	Embedded Networking	4	--	4
4		PE	Professional Elective -III	4	--	4
5		PE	Professional Elective -IV	4	--	4
6		OE	Open Elective -II	4	--	4
7	B2209	CC	Embedded Systems Laboratory	--	4	2
8	B2210	PW	Seminar	--	4	2
Total				24	8	**28**

II Year

III Semester				L	P	C
1	B2211	PW	Comprehensive Viva-Voce	--	--	4
2	B2212A	PW	Project Work (Review-I)	--	24	12
Total				**--**	**--**	**16**

IV Semester				L	P	C
1	B2212B	PW	Project Work (Review-II)	--	--	4
2	B2212C	PW	Project Work (Viva-Voce)		16	12
Total				**--**	**--**	**16**

Electives

S. No	Code	Name of Subject
Professional Elective –I		
1	B2229	Advanced Digital Signal Processing

2	B2220	VLSI Technology and Design
3	B2221	Embedded Computing
Professional Elective –II		
1	B2222	Digital System Design
2	B2223	Soft Computing Techniques
3	B2230	Image & Video Processing
Professional Elective –III		
1	B2224	Sensors and Actuators
2	B2225	Wireless Communications and Networks
3	B2504	Advanced Operating Systems
Professional Elective –IV		
1	B2226	Multimedia and Signal Coding
2	B2227	System On Chip Architecture
3	B2228	Wireless LANs and PANs
Open Elective –I		
1	B2240	Robotics
2	B2241	Digital Signal Processors & Architecture
3	B2314	Digital Control Systems
4	B2315	Reliability Engineering
5	B2522	Parallel and Distributed Algorithms
6	B2507	Software Architecture Design Patterns
Open Elective –II		
1	B2242	CPLD & FPGA Architecture & Applications
2	B2243	Low Power VLSI Design
3	B2319	Renewable Energy Systems
4	B2533	Cloud Computing
5	B2515	Web Services & Service Oriented Architecture
6	B2601	Operations Research

S. No	Category
CC	Core Course
PE	Professional Elective
OE	Open Elective
PW	Project Work, Seminar

DETAILED SYLLABUS
M.TECH(EMBEDDED SYSTEMS) R-02 REGULATION

I SEMESTER

(B2201) MICRO CONTROLLERS FOR EMBEDDED SYSTEMS DESIGN

M.Tech(ES) I Semester

L	T	P	C
4	0	0	4

UNIT –I:

ARM Architecture:

ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

UNIT –II:

ARM Programming Model – I:

Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT –III:

ARM Programming Model – II:

Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single- Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

UNIT –IV:

ARM Programming:

Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT –V:

Memory Management:

Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.

Text Books

1. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.

Reference books

1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.

(B2202) EMBEDDED REAL TIME OPERATING SYSTEMS

M.Tech(ES) I Semester

L	T	P	C
4	0	0	4

UNIT-I

Introduction

Introduction to UNIX/LINUX, Overview of Commands, File I/O (open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT - II:

Real Time Operating Systems

Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency.

Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT - III:

Objects, Services and I/O

Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O

Concepts, I/O Subsystem

UNIT - IV:

Exceptions, Interrupts and Timers

Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT - V:

Case Studies of RTOS

RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, Tiny OS, and Basic Concepts of Android OS.

Text book

1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011

Reference books

1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh

(B2203) EMBEDDED C

M.Tech(ES) I Semester

L	T	P	C
4	0	0	4

UNIT – I:

Programming Embedded Systems in C

Introduction ,What is an embedded system, Which processor should you use, Which programming language should you use, Which operating system should you use, How do you develop embedded software, Conclusions

Introducing the 8051 Microcontroller Family

Introduction, What's in a name, The external interface of the Standard 8051, Reset requirements ,Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption ,Conclusions

UNIT-II: Reading Switches

Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code), Example: Counting goats, Conclusions

UNIT – III:

Adding Structure to the Code

Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example, Example: Restructuring the goat-counting example, Further examples, Conclusions

UNIT – IV:

Meeting Real-Time Constraints

Introduction, Creating 'hardware delays' using Timer 0 and Timer 1, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2?, The need for 'timeout' mechanisms, Creating loop timeouts, Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions

UNIT – V:

Case Study: Intruder Alarm System

Introduction, The software architecture, Key software components used in this example, running the program, the software, Conclusions

Text books

1. Embedded C - Michael J. Pont, 2nd Ed., Pearson Education, 2008

Reference books

1. PIC micro MCU C-An introduction to programming, The Microchip PIC in CCS C - Nigel Gardner

(B2229) ADVANCED DIGITAL SIGNAL PROCESSING

(Professional Elective -I)

M.Tech(ES) I Semester

L	T	P	C
4	0	0	4

UNIT I

Review of DFI', FFT, IIR Filters, FIR Filters, Multirate Signal Processing: Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor lID, Multistage Implementation of Sampling Rate Conversion, Filter design & Implementation for sampling rate conversion, Applications of Multi rate Signal Processing

UNIT II

Non-Parametric methods of Power Spectral Estimation: Estimation of spectra from finite duration observation of signals, Non-parametric Methods: Bartlett, Welch & Blackman & Tukey methods, Comparison of all Non-Parametric methods

UNIT III

Parametric Methods of Power Spectrum Estimation: Autocorrelation & Its Properties, Relation between auto correlation & model parameters, AR Models - Yule-Waker & Burg Methods, MA & ARMA models for power spectrum estimation.

UNIT -IV

Linear Prediction: Forward and Backward Linear Prediction - Forward Linear Prediction, Backward Linear Prediction, Optimum reflection coefficients for the Lattice Forward and Backward Predictors. Solution of the Normal Equations: Levinson Durbin Algorithm, Schur Algorithm. Properties of Linear Prediction Filters

UNIT V

Finite Word Length Effects: Analysis of finite word length effects in Fixed-point DSP systems – Fixed , Floating Point Arithmetic - ADC quantization noise & signal quality - Finite word length effect in IIR digital Filters - Finite word-length effects in FFI' algorithms.

Text books

1. Digital Signal Processing: Principles, Algorithms & Applications - J .G.Proakis & D.G.Manolokis, 4th ed., PHI.
2. Discrete Time signal processing - Alan V Oppenheim & Ronald W Schaffer, PI-II.
3. DSP - A Practical Approach - Emmanuel C.Ifeacher, Barrie. W. Jervis, 2 ed., Pearson Education.

Reference books

1. Modern spectral Estimation: Theory & Application - S. M .Kay, 1988, PI-IT.
2. Multirate Systems and Filter Banks - P.P. Vaidyanathan - Pearson Education
3. Digital Signal Processing - S. Salivahanan, A. Vallavaraj, C. Gnanapriya, 2000,TMH

(B2220) VLSI TECHNOLOGY & DESIGN

(Professional Elective-I)

M.Tech(ES) I Semester

L	T	P	C
4	0	0	4

UNIT –I:

Review of Microelectronics and Introduction to MOS Technologies: MOS, CMOS, BiCMOS Technology.

Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: $I_{ds} - V_{ds}$ relationships, Threshold Voltage V_T, G_m, G_{ds} and ω_o, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Z_{pu}/Z_{pd}, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT –II:

Layout Design and Tools:

Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

Logic Gates & Layouts:

Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT –III:

Combinational Logic Networks:

Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT-IV: Sequential Systems

Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT –V: Floor Planning

Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

Text books

1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A. Pucknell, 2005, PHI.
2. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.

Reference books

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
   Principals of CMOS VLSI Design – N.H.E Weste, K. Eshraghian, 2nd Ed., Addison Wesley.

(B1206) EMBEDDED COMPUTING

(Professional Elective I)

M.Tech(ES) I Semester

L	T	P	C
4	0	0	4

UNIT –I:

Programming on Linux Platform:

System Calls, Scheduling, Memory Allocation, Timers, Embedded Linux, Root File System, Busy Box.

Operating System Overview: Processes, Tasks, Threads, Multi-Threading, Semaphore, Message Queue.

UNIT –II:

Introduction to Software Development Tools:

GNU GCC, make, gdb, static and dynamic linking, C libraries, compiler options, code optimization switches, lint, code profiling tools,.

UNIT-III: Interface Modules

Sensor and actuator interface, data transfer and control, GPS, GSM module interfacing with data processing and display, OpenCV for machine vision, Audio signal processing.

UNIT-IV: Networking Basics

Sockets, ports, UDP, TCP/IP, client server model, socket programming, 802.11, Bluetooth, ZigBee, SSH, firewalls, network security.

UNIT –V:

IA32 Instruction Set: application binary interface, exception and interrupt handling, interrupt latency, assemblers, assembler directives, macros, simulation and debugging tools.

Text books

1. Modern Embedded Computing - Peter Barry and Patrick Crowley, 1st Ed., Elsevier/Morgan Kaufmann, 2012.
2. Linux Application Development - Michael K. Johnson, Erik W. Troan, Adission Wesley, 1998.
3. Assembly Language for x86 Processors by Kip R. Irvine
4. Intel® 64 and IA-32 Architectures Software Developer Manuals

Reference books

1. Operating System Concepts by Abraham Silberschatz, Peter B. Galvin and Greg Gagne.
2. The Design of the UNIX Operating System by Maurice J. Bach Prentice-Hall
3. UNIX Network Programming by W. Richard Stevens

(B2221)DIGITAL SYSTEM DESIGN

(Professional Elective - II)

M.Tech(ES) I Semester

L	T	P	C
4	0	0	4

UNIT -I:

Minimization and Transformation of Sequential Machines:

The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines.

Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

UNIT-II: Digital Design

Digital Design Using ROMs, PALs and PLAs , BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

UNIT -III:

SM Charts:

State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

UNIT -IV:

Fault Modeling & Test Pattern Generation:

Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location – Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model.

Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

UNIT -V:

Fault Diagnosis in Sequential Circuits:

Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment

Text books

1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.
3. Logic Design Theory – N. N. Biswas, PHI

Reference books

1. Switching and Finite Automata Theory – Z. Kohavi , 2nd Ed., 2001, TMH
2. Digital Design – Morris Mano, M.D.Ciletti, 4th Edition, PHI.

3. Digital Circuits and Logic Design – Samuel C. Lee , PHI

(B2223)SOFT COMPUTING TECHNIQUES

(Professional Elective -II)

M.Tech(ES) I Semester

L	T	P	C
4	0	0	4

UNIT-I: Introduction

Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rule-based systems, the AI approach, Knowledge representation - Expert systems.

UNIT –II:

Artificial Neural Networks:

Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron, Learning and Training the neural network, Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations, Hopfield network, Self-organizing network and Recurrent network, Neural Network based controller.

UNIT –III:

Fuzzy Logic System:

Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning, Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification, Fuzzy knowledge and rule bases, Fuzzy modeling and control schemes for nonlinear systems, Self-organizing fuzzy logic control, Fuzzy logic control for nonlinear time delay system.

UNIT –IV:

Genetic Algorithm:

Basic concept of Genetic algorithm and detail algorithmic steps, Adjustment of free parameters, Solution of typical control problems using genetic algorithm, Concept on some other search techniques like Tabu search and Ant-colony search techniques for solving optimization problems.

UNIT-V: Applications

GA application to power system optimisation problem, Case studies: Identification and control of linear and nonlinear dynamic systems using MATLAB-Neural Network toolbox, Stability analysis of Neural-Network interconnection systems, Implementation of fuzzy logic controller using MATLAB fuzzy-logic toolbox, Stability analysis of fuzzy control systems.

Text books

1. Introduction to Artificial Neural Systems - Jacek.M.Zurada, Jaico Publishing House, 1999.
2. Neural Networks and Fuzzy Systems - Kosko, B., Prentice-Hall of India Pvt. Ltd., 1994.

Reference books

1. Fuzzy Sets, Uncertainty and Information - Klir G.J. & Folger T.A., Prentice-Hall of India Pvt. Ltd., 1993.
2. Fuzzy Set Theory and Its Applications - Zimmerman H.J. Kluwer Academic Publishers, 1994.

3. Introduction to Fuzzy Control - Driankov, Hellendroon, Narosa Publishers.
4. Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi.
5. Elements of Artificial Neural Networks - Kishan Mehrotra, Chelkuri K. Mohan, Sanjay Ranka, Penram International.
6. Artificial Neural Network –Simon Haykin, 2nd Ed., Pearson Education.
7. Introduction Neural Networks Using MATLAB 6.0 - S.N. Shivanandam, S. Sumati, S. N. Deepa,1/e, TMH, New Delhi.

(B2230) IMAGE & VIDEO PROCESSING

(Professional Elective -II)

M.Tech(ES) I Semester

L	T	P	C
4	0	0	4

UNIT I : Fundamentals of Image Processing and Image Transforms
Basic steps of Image Processing System Sampling and Quantization of an image - Basic relationship between pixels
Image Transforms: 2 D- Discrete Fourier Transform, Discrete Cosine Transform (DCT), Wavelet Transforms: Continuous Wavelet Transform, Discrete Wavelet Transforms.

UNIT II: Image Processing Techniques
Image Enhancement Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters. Frequency domain methods: Basics of filtering in frequency domain, image smoothing, image sharpening, Selective filtering.

Image Segmentation: Segmentation concepts, Point, Line and Edge Detection, Thresholding, Region Based segmentation.

UNIT III: Image Compression
Image compression fundamentals - Coding Redundancy, Spatial and Temporal redundancy, Compression models: Lossy & Lossless, Huffman coding, Arithmetic coding, LZW coding, Run length coding, Bit plane coding, Transform coding, Predictive coding, Wavelet coding, JPEG Standards.

UNIT IV: **Basic steps of Video Processing**
Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, Filtering operations.

UNIT V: **2-D Motion Estimation**
Optical flow, General Methodologies, Pixel Based Motion Estimation, Block- Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

Text books
1. Digital Image Processing - Gonzaleze and Woods, 3rd ed., Pearson.
2. Video processing and communication - Yao Wang, J oem Ostermann and Ya-quin Zhang. I SI Ed., PII Int.

Reference Book
1. Digital Video Processing - M. Tekalp, Prentice Hall International

(B2240) ROBOTICS

(Open Elective – I)

M.Tech(ES) I Semester

L	T	P	C
4	0	0	4

Unit - I: Introduction & Basic Definitions

Introduction, Control Programs for Robots, Industry Applications of Robots, Pick and Place, Gantry and Arm type Robots in typical set-ups like Automobile Industry Coordinate Systems: Cartesian, Cylindrical, Polar, and Revolute systems: Robot Positioning: Robot Arms; Axes, their ranges, offset and In-line Wrist: Roll, Pitch and Yaw, their meaning in Robotics

Unit-II: Mechanical Aspects

Kinematics, Inverse Kinematics, Motion planning and Mobile Mechanisms

Unit-Ill: Sensors and Applications

Range and Use of Sensors, Micro switches, Resistance Transducers, Piezo-electric, Infrared and Lasers. Applications of Sensors: Reed Switches, Ultrasonic, Barcode Readers and RFlD

Unit-TV Robot Systems

Hydraulic and Electrical Systems including pumps, valves, solenoids, cylinders, stepper motors, Encoders and *i\C* Motors

Unit- V Programming of Robots

Programming of Robots such as Lego Robots, Programming environment, Example Applications, Safety considerations

Text books:

1. Introduction to Robotics - PJ .Mckerrow, ISBN: 0201182408
2. Introduction to Robotics - S. Nikv, 200 I, Prentice Hall,
3. Mechatronics and Robotics: Design & Applications - A. Mutanbara, I 999, CRC Press.

Reference book

1. Robotics - K. S. Fu, RC. Gonzalez and C.S.G. Lee, 2008, TMH.

(B2241) DIGITAL SIGNAL PROCESSORS & ARCHITECTURES

(Open Elective – I)

M.Tech(ES) I Semester

L	T	P	C
4	0	0	4

UNIT –I:

Introduction to Digital Signal Processing:

Introduction, a Digital signal-processing system, The sampling process, discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation.

Computational Accuracy in DSP Implementations:

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT –II:

Architectures for Programmable DSP Devices:

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT -III:

Programmable Digital Signal Processors:

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT –IV:

Analog Devices Family of DSP Devices:

Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor.

Introduction to Black fin Processor - The Black fin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

UNIT –V:

Interfacing Memory and I/O Peripherals to Programmable DSP Devices:

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

Text books

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. A Practical Approach To Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, New Age International, 2006/2009
3. Embedded Signal Processing with the Micro Signal Architecture: Woon-Seng Gan, Sen M. Kuo, Wiley-IEEE Press, 2007

Reference books

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkataramani and M. Bhaskar, 2002, TMH.
2. Digital Signal Processing – Jonatham Stein, 2005, John Wiley.
3. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. 2000, S. Chand & Co.
4. Digital Signal Processing Applications Using the ADSP-2100 Family by The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI
5. The Scientist and Engineer's Guide to Digital Signal Processing by Steven W. Smith, Ph.D., California Technical Publishing, ISBN 0-9660176-3-3, 1997
6. Embedded Media Processing by David J. Katz and Rick Gentile of Analog Devices, Newnes , ISBN 0750679123, 2005

(B2314) DIGITAL CONTROL SYSTEMS

(Open Elective – I, Offered By EEE Dept)

M. Tech(ES) – I Semester

L	T	P	C
4	0	0	4

UNIT – I: Introduction

Block Diagram of typical control system- advantages of sampling in control systems – examples of discrete data and digital systems – data conversion and quantization – sample and hold devices – D/A and A/D conversion – sampling theorem – reconstruction of sampled signals –ZOH.

Z-transform: Definition and evaluation of Z-transforms – mapping between s-plane and z-plane – inverse z-plane transform – theorems of the Z-transforms –limitations of z-transforms –pulse transfer function –pulse transfer function of ZOH –relation between G(s) and G(z) – signal flow graph method applied to digital systems.

UNIT- II: State Space Analysis

State space modeling of digital systems with sample and hold – state transition equation of digital time in variant systems – solution of time in variant discrete state equations by the Z-Transformation – transfer function from the state model – Eigen values – Eigen vector and diagonalisation of the A-matrix – Jordan canonical form. Computation of state transition matrix-Transformation to phase to variable canonical form-The state diagram – decomposition of digital system – Response of sample data system between sampling instants using state approach.

Stability: Definition of stability – stability tests – The second method of Liapunov.

UNIT- III: Time Domain Analysis

Comparison of time response of continuous data and digital control systems-correlation between time response and root locus j the s-plane and z-plane – effect of pole-zero configuration in the z-plane upon the maximum overshoot and peak time of transient response – Root loci for digital control systems – steady state error analysis of digital control systems – Nyquits plot – Bode plot-G.M and P.M.

UNIT- IV: Digital Control Design

The digital control design with digital controller with bilinear transformation – Digital PID controller-Design with deadbeat response-Pole placement through state feedback-Design of full order state observer-Discrete Euler Lagrance Equation – Discrete maximum principle.

UNIT-V: Digital State Observer

Design of - Full order and reduced order observers. Design by max. principle: Discrete Euler language equation-discrete maximum principle.

Text Books

1. Discrete-Time Control systems - K. Ogata, Pearson Education/PHI, 2nd Edition.
2. Digital Control and State Variable Methods by M.Gopal, TMH.

Reference Books

1. Digital Control Systems, Kuo, Oxford University Press, 2nd Edition, 2003.
2. Digital Control Engineering, M.Gopal

(B2315) RELIABILITY ENGINEERING

(Open Elective – I, Offered By EEE Dept)

M. Tech(ES) – I Semester

L	T	P	C
4	0	0	4

UNIT – I: Basics of Probability Theory & Distribution

Basic probability theory – rules for combining probabilities of events – Bernoulli's trials – probabilities density and distribution functions – binomial distribution – expected value and standard deviation of binomial distribution.

UNIT – II: Network Modelling and Reliability Analysis

Analysis of Series, Parallel, Series-Parallel networks – complex networks – decomposition method.

UNIT – III: Reliability Functions

Reliability functions f(t), F(t),R(t),h(t) and their relationships – exponential distribution – Expected value and standard deviation of exponential distribution – Bath tub curve – reliability analysis of series parallel networks using exponential distribution – reliability measures MTTF, MTTR, MTBF.

UNIT – IV: Markov Modelling

Markov chains – concept of stochastic transitional probability Matrix, Evaluation of limiting state Probabilities. – Markov processes one component repairable system – time dependent probability evaluation using Laplace transform approach – evaluation of limiting state probabilities using STPM – two component repairable models.

UNIT – V: Frequency & Duration Techniques

Frequency and duration concept – Evaluation of frequency of encountering state, mean cycle time, for one , two component repairable models – evaluation of cumulative probability and cumulative frequency of encountering of merged states.

Text Books

1. Reliability Evaluation of Engg. System – R. Billinton, R.N.Allan, Plenum Press, New York, reprinted in India by B.S.Publications, 2007.
2. Reliability Evaluation of Power systems – R. Billinton, R.N.Allan, Pitman Advance Publishing Program, New York reprinted in India by B.S.Publications, 2007.

(B2522)PARALLEL AND DISTRIBUED ALGORITHMS

(Open Elective – 1 offered by CSE Dept.)

M.Tech(ES) I Semester

L	T	P	C
4	0	0	4

Objectives

- To learn parallel and distributed algorithms development techniques for shared memory and message passing models.
- To study the main classes of parallel algorithms.
- To study the complexity and correctness models for parallel algorithms.

Unit-I

Basic Techniques, Parallel Computers for increase Computation speed, Parallel & Cluster Computing.

Unit-II

Message Passing Technique- Evaluating Parallel programs and debugging, Portioning and Divide and conquer strategies examples.

Unit-III

Pipelining- Techniques computing platform, pipeline programs examples

Unit-IV

Synchronous Computations, load balancing, distributed termination examples, programming with shared memory, shared memory multiprocessor constructs for specifying parallel list sharing data parallel programming languages and constructs, open MP

Unit-V

Distributed shared memory systems and programming achieving constant memory distributed
shared memory programming primitives, algorithms – sorting and numerical algorithms.

Text Book

1. Parallel Programming, Barry Wilkinson, Michael Allen, Pearson Education, 2nd Edition.

Reference Book

1. Introduction to Parallel algorithms by Jaja from Pearson, 1992.

(B2507) SOFTWARE ARCHITECTURE DESIGN PATTERNS

(Open Elective – 1 offered by CSE Dept.)

M.Tech(ES) I Semester

L	T	P	C
4	0	0	4

Objectives:

- After completing this course, the student should be able to:
- To understand the concept of patterns and the Catalog.
- To discuss the Presentation tier design patterns and their affect on: sessions, client access, validation and consistency.
- To understand the variety of implemented bad practices related to the Business and Integration tiers.
- To highlight the evolution of patterns.
- To how to add functionality to designs while minimizing complexity
- To understand what design patterns really are, and are not
- To learn about specific design patterns.
- To learn how to use design patterns to keep code quality high without overdesign.

UNIT I

Envisioning Architecture The Architecture Business Cycle, What is Software Architecture, Architectural patterns, reference models, reference architectures, architectural structures and views.

Creating an Architecture Quality Attributes, Achieving qualities, Architectural styles and patterns, designing the Architecture, Documenting software architectures, Reconstructing Software Architecture.

UNIT II

Analyzing Architectures Architecture Evaluation, Architecture design decision making, ATAM, CBAM.

Moving from one system to many Software Product Lines, Building systems from off the shelf components, Software architecture in future.

UNIT III

Patterns Pattern Description, Organizing catalogs, role in solving design problems, Selection and usage.

Creational and Structural patterns Abstract factory, builder, factory method, prototype, singleton, adapter, bridge, composite, façade, flyweight.

UNIT IV

Behavioral patterns Chain of responsibility, command, Interpreter, iterator, mediator, memento, observer, state, strategy, template method, visitor.

UNIT V

Case Studies A-7E – A case study in utilizing architectural structures, The World Wide Web - a case study in interoperability, Air Traffic Control – a case study in designing for high availability, Celsius Tech – a case study in product line development,

Text Books

1. Software Architecture in Practice, second edition, Len Bass, Paul Clements & Rick Kazman, Pearson Education, 2003.

2. Design Patterns, Erich Gamma, Pearson Education, 1995.

Reference Books

1. Beyond Software architecture, Luke Hohmann, Addison wesley, 2003.
2. Software architecture, David M. Dikel, David Kane and James R. Wilson, Prentice Hall PTR, 2001
3. Software Design, David Budgen, second edition, Pearson education, 2003
4. Head First Design patterns, Eric Freeman & Elisabeth Freeman, O'REILLY, 2007.
5. Design Patterns in Java, Steven John Metsker & William C. Wake, Pearson education, 2006
6. J2EE Patterns, Deepak Alur, John Crupi & Dan Malks, Pearson education, 2003.
7. Design Patterns in C#, Steven John metsker, Pearson education, 2004.
8. Pattern Oriented Software Architecture, F.Buschmann & others, John Wiley & Sons.

(B2205) EMBEDDED C LABORATORY

M.Tech(ES) I Semester

L	T	P	C
0	0	4	2

Note:

Minimum of 10 experiments have to be conducted.

The following programs have to be tested on 89C51 Development board/equivalent using Embedded C Language on Keil IDE or Equivalent.

1. Program to toggle all the bits of Port P1 continuously with 250 mS delay.
2. Program to toggle only the bit P1.5 continuously with some delay. Use Timer 0, mode 1 to create delay.
3. Program to interface a switch and a buzzer to two different pins of a Port such that the buzzer should sound as long as the switch is pressed.
4. Program to interface LCD data pins to port P1 and display a message on it.
5. Program to interface keypad. Whenever a key is pressed, it should be displayed on LCD.
6. Program to interface seven segment display unit.
7. Program to transmit a message from Microcontroller to PC serially using RS232.
8. Program to receive a message from PC serially using RS232.
9. Program to get analog input from Temperature sensor and display the temperature value on PC Monitor.
10. Program to interface Stepper Motor to rotate the motor in clockwise and anticlockwise directions
11. Program to Sort RTOS on to 89C51 development board.
12. Program to interface Elevator.

II SEMESTER

(B2206) HARDWARE - SOFTWARE CO-DESIGN

M.Tech(ES) II Semester

L	T	P	C
4	0	0	4

UNIT –I:

Co- Design Issues:

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms:

Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT –II:

Prototyping and Emulation:

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures:

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III:

Compilation Techniques and Tools for Embedded Processor Architectures:

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV:

Design Specification and Verification:

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V:

Languages for System – Level Specification and Design-I:

System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II:

Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

Text Books

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers

Reference Books

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer

(B2207) EMBEDDED SYSTEMS DESIGN

M.Tech(ES) II Semester

L	T	P	C
4	0	0	4

UNIT -I:

Introduction to Embedded Systems

Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT -II:

Typical Embedded System:

Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT -III:

Embedded Firmware:

Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT -IV:

RTOS Based Embedded System Design:

Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT -V:

Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

Text books

1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.

Reference books

1. Embedded Systems - Raj Kamal, TMH.
2. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.
3. Embedded Systems – Lyla, Pearson, 2013
4. An Embedded Software Primer - David E. Simon, Pearson Education.

(B2208) EMBEDDED NETWORKING

M.Tech(ES) II Semester

L	T	P	C
4	0	0	4

UNIT –I:

Embedded Communication Protocols:

Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire.

UNIT –II:

USB and CAN Bus:

USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.

UNIT-III: Ethernet Basics

Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.

UNIT

UNIT-IV: Embedded Ethernet

Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT –V:

Wireless Embedded Networking:

Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.

Text books

1. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, Tony Givargis, John & Wiley Publications, 2002
2. Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port - Jan Axelson, Penram Publications, 1996.

Reference books

1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series - Dogan Ibrahim, Elsevier 2008.
2. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003.
3. Networking Wireless Sensors - Bhaskar Krishnamachari , Cambridge press 2005.

(B2224) SENSORS AND ACTUATORS

(Professional Elective –III)

M.Tech(ES) II Semester

L	T	P	C
4	0	0	4

UNIT -I:

Sensors / Transducers: Principles – Classification – Parameters – Characteristics - Environmental Parameters (EP) – Characterization

Mechanical and Electromechanical Sensors: Introduction – Resistive Potentiometer – Strain Gauge – Resistance Strain Gauge – Semiconductor Strain Gauges -Inductive Sensors: Sensitivity and Linearity of the Sensor –Types-Capacitive Sensors:– Electrostatic Transducer– Force/Stress Sensors Using Quartz Resonators – Ultrasonic Sensors

UNIT –II:

Thermal Sensors: Introduction – Gas thermometric Sensors – Thermal Expansion Type Thermometric Sensors – Acoustic Temperature Sensor – Dielectric Constant and Refractive Index thermosensors – Helium Low Temperature Thermometer – Nuclear Thermometer – Magnetic Thermometer – Resistance Change Type Thermometric Sensors –Thermoemf Sensors– Junction Semiconductor Types– Thermal Radiation Sensors –Quartz Crystal Thermoelectric Sensors – NQR Thermometry – Spectroscopic Thermometry – Noise Thermometry – Heat Flux Sensors

Magnetic sensors: Introduction – Sensors and the Principles Behind – Magneto-resistive Sensors – Anisotropic Magnetoresistive Sensing – Semiconductor Magnetoresistors– Hall Effect and Sensors – Inductance and Eddy Current Sensors– Angular/Rotary Movement Transducers – Synchros – Synchro-resolvers - Eddy Current Sensors – Electromagnetic Flowmeter – Switching Magnetic Sensors SQUID Sensors

UNIT -III:

Radiation Sensors: Introduction – Basic Characteristics – Types of Photosensistors/Photo detectors– X-ray and Nuclear Radiation Sensors– Fiber Optic Sensors

Electro analytical Sensors: Introduction – The Electrochemical Cell – The Cell Potential - Standard Hydrogen Electrode (SHE) – Liquid Junction and Other Potentials – Polarization – Concentration Polarization-– Reference Electrodes - Sensor Electrodes – Electro ceramics in Gas Media .

UNIT -IV:

Smart Sensors: Introduction – Primary Sensors – Excitation – Amplification – Filters – Converters – Compensation– Information Coding/Processing - Data Communication – Standards for Smart Sensor Interface – The Automation

Sensors –Applications: Introduction – On-board Automobile Sensors (Automotive Sensors)– Home Appliance Sensors – Aerospace Sensors –– Sensors for Manufacturing – Sensors for environmental Monitoring

UNIT -V:

Actuators: Pneumatic and Hydraulic Actuation Systems- Actuation systems – Pneumatic and hydraulic systems - Directional Control valves – Pressure control valves – Cylinders - Servo and proportional control valves – Process control valves – Rotary actuators

Mechanical Actuation Systems- Types of motion – Kinematic chains – Cams – Gears – Ratchet and pawl – Belt and chain drives – Bearings – Mechanical aspects of motor selection

Electrical Actuation Systems-Electrical systems -Mechanical switches – Solid-state switches Solenoids – D.C. Motors – A.C. motors – Stepper motors

Text Books

1. D. Patranabis – "Sensors and Transducers" –PHI Learning Private Limited.
2. W. Bolton – "Mechatronics" –Pearson Education Limited.

Reference Books

1. Sensors and Actuators – D. Patranabis – 2nd Ed., PHI, 2013.

(B2225) WIRELESS COMMUNICATIONS AND NETWORKS

(Professional Elective –III)

M.Tech(ES) II Semester

L	T	P	C
4	0	0	4

UNIT -I

The Cellular Concept-System Design Fundamentals: Introduction, Frequency Reuse, Channel Assignment Strategies, Handoff Strategies- Prioritizing Handoffs, Practical Handoff Considerations, Interference and system capacity – Co channel Interference and system capacity, Channel planning for Wireless Systems, Adjacent Channel interference , Power Control for Reducing interference, Trunking and Grade of Service, Improving Coverage & Capacity in Cellular Systems- Cell Splitting, Sectoring .

UNIT –II

Mobile Radio Propagation: Large-Scale Path Loss: Introduction to Radio Wave Propagation, Free Space Propagation Model, Relating Power to Electric Field, The Three Basic Propagation Mechanisms, Reflection-Reflection from Dielectrics, Brewster Angle, Reflection from prefect conductors, Ground Reflection (Two-Ray) Model, Diffraction-Fresnel Zone Geometry, Knife-edge Diffraction Model, Multiple knife-edge Diffraction, Scattering, Outdoor Propagation Models- Longley-Ryce Model, Okumura Model, Hata Model, PCS Extension to Hata Model, Walfisch and Bertoni Model, Wideband PCS Microcell Model, Indoor Propagation Models-Partition losses (Same Floor), Partition losses between Floors, Log-distance path loss model, Ericsson Multiple Breakpoint Model, Attenuation Factor Model, Signal penetration into buildings, Ray Tracing and Site Specific Modeling.

UNIT –III

Mobile Radio Propagation: Small –Scale Fading and Multipath: Small Scale Multipath propagation-Factors influencing small scale fading, Doppler shift, Impulse Response Model of a multipath channel- Relationship between Bandwidth and Received power, Small-Scale Multipath Measurements-Direct RF Pulse System, Spread Spectrum Sliding Correlator Channel Sounding, Frequency Domain Channels Sounding, Parameters of Mobile Multipath Channels-Time Dispersion Parameters, Coherence Bandwidth, Doppler Spread and Coherence Time, Types of Small-Scale Fading-Fading effects Due to Multipath Time Delay Spread, Flat fading, Frequency selective fading, Fading effects Due to Doppler Spread-Fast fading, slow fading, Statistical Models for multipath Fading Channels-Clarke's model for flat fading, spectral shape due to Doppler spread in Clarke's model, Simulation of Clarke and Gans Fading Model, Level crossing and fading statistics, Two-ray Rayleigh Fading Model.

UNIT -IV

Equalization and Diversity: Introduction, Fundamentals of Equalization, Training A Generic Adaptive Equalizer, Equalizers in a communication Receiver, Linear Equalizers, Non linear Equalization-Decision Feedback Equalization (DFE), Maximum Likelihood Sequence Estimation (MLSE) Equalizer, Algorithms for adaptive equalization-Zero Forcing Algorithm, Least Mean Square Algorithm, Recursive least squares algorithm. Diversity Techniques-Derivation of selection Diversity improvement, Derivation of Maximal Ratio Combining improvement, Practical Space Diversity Consideration-Selection Diversity, Feedback or Scanning Diversity, Maximal Ratio Combining, Equal Gain Combining, Polarization Diversity, Frequency Diversity, Time Diversity, RAKE Receiver.

UNIT -V

Wireless Networks: Introduction to wireless Networks, Advantages and disadvantages of Wireless Local Area Networks, WLAN Topologies, WLAN Standard IEEE 802.11,IEEE 802.11 Medium Access Control, Comparision of IEEE 802.11 a,b,g and n standards, IEEE 802.16 and its enhancements, Wireless PANs, Hiper Lan, WLL.

Text Books

1. Wireless Communications, Principles, Practice – Theodore, S. Rappaport, 2nd Ed., 2002, PHI.
2. Wireless Communications-Andrea Goldsmith, 2005 Cambridge University Press.
3. Mobile Cellular Communication – Gottapu Sasibhushana Rao, Pearson Education, 2012.

Reference Books

1. Principles of Wireless Networks – Kaveh Pah Laven and P. Krishna Murthy, 2002, PE
2. Wireless Digital Communications – Kamilo Feher, 1999, PHI.
3. Wireless Communication and Networking – William Stallings, 2003, PHI.
4. Wireless Communication – Upen Dalal, Oxford Univ. Press
5. Wireless Communications and Networking – Vijay K. Gary, Elsevier.

(B2504) ADVANCED OPERATING SYSTEMS

(Professional Elective -III)

M.Tech(ES) II Semester

L	T	P	C
4	0	0	4

UNIT –I:

Introduction to Operating Systems

Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluation of operating System

UNIT –II:

Introduction to UNIX and LINUX

Basic commands & command arguments, Standard input, output, Input / output redirection, filters and editors, Shells and operations

UNIT-III: System Calls

System calls and related file structures, Input / Output, Process creation & termination.

Inter Process Communication

Introduction, file and record locking, Client – Server example, pipes, FIFOs, Streams & Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

UNIT –IV:

Introduction to Distributed Systems

Goals of distributed system, Hardware and software concepts, Design issues.

Communication in Distributed Systems:

Layered protocols, ATM networks, Client - Server model, Remote procedure call and Group communication.

UNIT –V:

Synchronization in Distributed Systems

Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions

Deadlocks:

Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.

Text books

1. The design of the UNIX Operating Systems – Maurice J. Bach, 1986, PHI.
2. Distributed Operating System - Andrew. S. Tanenbaum, 1994, PHI.
3. The Complete reference LINUX – Richard Peterson, 4th Ed., McGraw – Hill.

Reference books

1. Operating Systems: Internal and Design Principles - Stallings, 6th Ed., PE.
2. Modern Operating Systems, Andrew S Tanenbaum, 3rd Ed., PE.
3. Operating System Principles- Abraham Silberchatz, Peter B. Galvin, Greg Gagne, 7th Ed., John Wiley
4. UNIX User Guide – Ritchie & Yates.
5. UNIX Network Programming - W.Richard Stevens, 1998, PHI.

(B2226) MULTI MEDIA AND SIGNAL CODING

(Professional Elective -IV)

M.Tech(ES) II Semester

L	T	P	C
4	0	0	4

UNIT -I:

Introduction to Multimedia: Multimedia, World Wide Web, Overview of Multimedia Tools, Multimedia Authoring, Graphics/ Image Data Types, and File Formats.

Color in Image and Video: Color Science – Image Formation, Camera Systems, Gamma Correction, Color Matching Functions, CIE Chromaticity Diagram, Color Monitor Specifications, Out-of-Gamut Colors, White Point Correction, XYZ to RGB Transform, Transform with Gamma Correction, L*A*B* Color Model. Color Models in Images – RGB Color Model for CRT Displays, Subtractive Color: CMY Color Model, Transformation from RGB to CMY, Under Color Removal: CMYK System, Printer Gamuts, Color Models in Video – Video Color Transforms, YUV Color Model, YIQ Color Model, Ycbcr Color Model.

UNIT -II:

Video Concepts: Types of Video Signals, Analog Video, Digital Video.

Audio Concepts: Digitization of Sound, Quantization and Transmission of Audio.

UNIT -III:

Compression Algorithms:

Lossless Compression Algorithms: Run Length Coding, Variable Length Coding, Arithmetic Coding, Lossless JPEG, Image Compression.

Lossy Image Compression Algorithms: Transform Coding: KLT And DCT Coding, Wavelet Based Coding.

Image Compression Standards: JPEG and JPEG2000.

UNIT -IV:

Video Compression Techniques: Introduction to Video Compression, Video Compression Based on Motion Compensation, Search for Motion Vectors, H.261- Intra-Frame and Inter-Frame Coding, Quantization, Encoder and Decoder, Overview of MPEG1 and MPEG2.

UNIT -V:

Audio Compression Techniques: ADPCM in Speech Coding, G.726 ADPCM, Vocoders – Phase Insensitivity, Channel Vocoder, Formant Vocoder, Linear Predictive Coding, CELP, Hybrid Excitation Vocoders, MPEG Audio – MPEG Layers, MPEG Audio Strategy, MPEG Audio Compression Algorithms, MPEG-2 AAC, MPEG-4 Audio.

Text Books

1. Fundamentals of Multimedia – Ze- Nian Li, Mark S. Drew, PHI, 2010.
2. Multimedia Signals & Systems – Mrinal Kr. Mandal Springer International Edition 1st Edition, 2009

Reference Books

1. Multimedia Communication Systems – Techniques, Stds& Netwroks K.R. Rao, Zorans. Bojkoric, Dragorad A.Milovanovic, 1st Edition, 2002.
2. Fundamentals of Multimedia Ze- Nian Li, Mark S.Drew, Pearson Education (LPE), 1st Edition, 2009.
3. Multimedia Systems John F. Koegel Bufond Pearson Education (LPE), 1st Edition, 2003.

4. Digital Video Processing – A. Murat Tekalp, PHI, 1996.
5. Video Processing and Communications – Yaowang, Jorn Ostermann, Ya-QinZhang, Pearson, 2002

(B2227) SYSTEM ON CHIP ARCHITECTURE

(Professional Elective-IV)

M.Tech(ES) II Semester

L	T	P	C
4	0	0	4

UNIT –I:

Introduction to the System Approach

System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT-II

UNIT-II: Processors

Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT –III:

Memory Design for SOC

Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT -IV

Interconnect Customization and Configuration:

Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT –V

Application Studies / Case Studies:

SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

Text Books

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.

Reference Books

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

(B2228) WIRELESS LANS AND PANS

(Professional Elective - IV)

M.Tech(ES) II Semester

L	T	P	C
4	0	0	4

UNIT –I:

Wireless System & Random Access Protocols:

Introduction, First and Second Generation Cellular Systems, Cellular Communications from 1G to 3G, Wireless 4G systems, The Wireless Spectrum; Random Access Methods: Pure ALOHA, Slotted ALOHA, Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA).

UNIT-II: Wireless LANs

Introduction, importance of Wireless LANs, WLAN Topologies, Transmission Techniques: Wired Networks, Wireless Networks, comparison of wired and Wireless LANs; WLAN Technologies: Infrared technology, UHF narrowband technology, Spread Spectrum technology

UNIT –III:

The IEEE 802.11 Standard for Wireless LANs:

Network Architecture, Physical layer, The Medium Access Control Layer; MAC Layer issues: Hidden Terminal Problem, Reliability, Collision avoidance, Congestion avoidance, Congestion control, Security, The IEEE 802.11e MAC protocol

UNIT-IV: Wireless PANs

Introduction, importance of Wireless PANs, The Bluetooth technology: history and applications, technical overview, the Bluetooth specifications, piconet synchronization and Bluetooth clocks, Master-Slave Switch; Bluetooth security; Enhancements to Bluetooth: Bluetooth interference issues, Intra and Inter Piconet scheduling, Bridge selection, Traffic Engineering, QoS and Dynamics Slot Assignment, Scatternet formation.

UNIT –V:

The IEEE 802.15 working Group for WPANs:

The IEEE 802.15.3, The IEEE 802.15.4, ZigBee Technology, ZigBee components and network topologies, The IEEE 802.15.4 LR-WPAN Device architecture: Physical Layer, Data Link Layer, The Network Layer, Applications; IEEE 802.15.3a Ultra wideband.

Text Books

1. Ad Hoc and Sensor Networks - Carlos de Morais Cordeiro and Dharma Prakash Agrawal, World Scientific, 2011.
2. Wireless Communications and Networking - Vijay K.Garg, Morgan Kaufmann Publishers, 2009.

Reference Books

1. Wireless Networks - Kaveh Pahlaram, Prashant Krishnamurthy, PHI, 2002.
2. Wireless Communication- Marks Ciampor, Jeorge Olenewa, Cengage Learning, 2007.

(B2242) CPLD AND FPGA ARCHITECTURES AND APPLICATIONS

(Open Elective – II)

M.Tech(ES) II Semester

L	T	P	C
4	0	0	4

UNIT-I:

Introduction to Programmable Logic Devices

Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II:

Field Programmable Gate Arrays

Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT -III:

SRAM Programmable FPGAs

Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT -IV:

Anti-Fuse Programmed FPGAs

Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT -V:

Design Applications

General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

Text Books

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

Reference Books

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

(B2243) LOW POWER VLSI DESIGN

(Open Elective – II)

M.Tech(ES) II Semester

L	T	P	C
4	0	0	4

UNIT I

Low Power Design - An over View: Introduction to low ..• voltage low power design, limitations, Silicon-on-Insulator.

MOS/BiCMOS Processes: Bi CMOS processes, Integration and Isolation considerations, Integrated Analog/ Digital CMOS Process.

UNIT II

Low- Voltage/Low Power CMOS/ BiCMOS Processes: Deep submicron processes, SOl CMOS, lateral BIT on SOl, future trends and directions of CMOS/BiCMOS processes.

UNIT III

Device Behaviour and Modelling: Advanced MOSFET models, limitations of MOSFET models, bipolar models. Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid- mode environment

UNIT IV

CMOS and Bi-CMOS Logic Gates: Conventional CMOS and BiCMOS logic gates/Performance evaluation. Low- Voltage Low Power Logic Circuits Comparison of advanced BiCMOS Digital circuits. ESD-free Hi CMOS, Digital circuit operation and comparative Evaluation.

UNIT V

Low Power Latches And Flip Flops: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

Text books

1. CMOS/BiCMOS ULSI low voltage, low power by Yeo Rofaill Gohl(3 Authors)-Pearson Education Asia 1st Indian reprint,2002

Reference books

1. Digital Integrated circuits - J .M. Rabaey, PH. N.J 1996
2. CMOS Digital Integrated Circuits Analysis & Design - Sung-Mo Kang, Yusuf Lleblebici 3rd ed., 2003, TMH2003
3. VLSI DSP Systems - K.K. Parhi, 999, John Wiley & Sons.
4. IEEE Trans Electron Devices, IEEE J, Solid State Circuits, and other National and International Conferences and Symposia.

(B2319) RENEWABLE ENERGY SYSTEMS

(Open Elective – II, Offered by EEE Dept)

M.Tech(ES) II Semester

L	T	P	C
4	0	0	4

UNIT-I:

Photo voltaic power generation ,spectral distribution of energy in solar radiation, solar cell configurations, voltage developed by solar cell, photo current and load current, practical solar cell performance, commercial photo voltaic systems, test specifications for PV systems, applications of super conducting materials in electrical equipment systems.

UNIT-II:

Principles of MHD power generation, ideal MHD generator performance, practical MHD generator, MHD technology.

Wind Energy conversion: Power from wind, properties of air and wind, types of wind Turbines, operating characteristics.

UNIT-III:

Tides and tidal power stations, modes of operation, tidal project examples, turbines and generators for tidal power generation.

Wave energy conversion: properties of waves and power content, vertex motion of Waves, device applications. Types of ocean thermal energy conversion systems Application of OTEC systems examples,

UNIT-IV:

Miscellaneous energy conversion systems: coal gasification and liquefaction, biomass conversion, geothermal energy, thermo electric energy conversion, principles of EMF generation, description of fuel cells, Co-generation and energy storage, combined cycle co-generation, energy storage.

Global energy position and environmental effects: energy units, global energy position.

UNIT-V:

Types of fuel cells, H_2-O_2 Fuel cells, Application of fuel cells – Batteries, Description of batteries, Battery application for large power. Environmental effects of energy conversion systems, pollution from coal and preventive measures steam stations and pollution, pollution free energy systems.

Text Books

1. "Energy conversion systems" by Rakosh das Begamudre, New age International publishers, New Delhi - 2000.
2. "Renewable Energy Resources" by John Twidell and Tony Weir, 2nd Edition, Fspon &Co

(B2533) CLOUD COMPUTING

(Open Elective – II, offered by CSE Dept.)

M.Tech(ES) II Semester

L	T	P	C
4	0	0	4

Course Objectives:

- To learn the new computing model which enables shared resources on demand over the network.
- To learn about the pay-per-use scenarios.
- To learn about the new kind of service models and deployment models.
- To learn about the virtualization technology.
- To learn the python programming or various services and models.
- To develop cloud applications in Python

UNIT-I

Principles of Parallel and Distributed Computing, Introduction to cloud computing, Cloud computing Architecture, cloud concepts and technologies, cloud services and platforms, Cloud models, cloud as a service, cloud solutions, cloud offerings, introduction to Hadoop and Mapreduce.

UNIT –II

Cloud Platforms for Industry, Healthcare and education, Cloud Platforms in the Industry, cloud applications. Virtualization, cloud virtualization technology, deep dive: cloud virtualization, Migrating in to cloud computing, Virtual Machines Provisioning and Virtual Machine Migration Services, On the Management of Virtual Machines for cloud Infrastructure, Comet cloud, T- Systems,

UNIT-III

Cloud computing Applications: Industry, Health, Education, Scientific Applications, Business and Consumer Applications, Understanding Scientific Applications for Cloud Environments, Impact of Cloud computing on the role of corporate IT. Enterprise cloud computing Paradigm, Federated cloud computing Architecture, SLA Management in Cloud Computing, Developing the cloud: cloud application Design.

UNIT-IV

Python Basics, Python for cloud, cloud application development in python, Cloud Application Development in Python.

Programming Google App Engine with Python: A first real cloud Application, Managing Data in the cloud, Google app engine Services for Login Authentication, Optimizing UI and Logic, Making the UI Pretty: Templates and CSS, Getting Interactive. Map Reduce Programming Model and Implementations.

UNIT-V

Cloud management, Organizational Readiness and change management in the cloud age ,Cloud Security ,Data security in the cloud, Legal Issues in the Cloud , Achieving Production Readiness for the cloud Services

Text Books

1. Cloud Computing : Raj Kumar Buyya , James Broberg, andrzej Goscinski, 2013 Wiley

2. Mastering Cloud Computing: Raj Kumar buyya, Christian Vecchiola,selvi-2013.
3. Cloud Computing: Arshdeep Bahga, Vijay Madisetti, 2014, University Press.
4. Cloud computing: Dr Kumar Saurab Wiley India 2011.

Reference Books

1. Code in the Cloud: Mark C.Chu-Carroll 2011, SPD.(Second part of IV UNIT)
2. Essentials of cloud computing : K Chandrasekharan CRC Press.
3. Cloud Computing: John W. Rittinghouse, James Ransome, CRC Press.
4. Virtualization Security: Dave shackleford 2013. SYBEX a wiley Brand.
5. Cloud computing and Software Services: Ahson , Ilyas.2011.
6. Cloud Computing Bible: Sosinsky 2012. Wiley India .
7. Cloud Computing: Dan C. Marinescu-2013, Morgan Kaufmann.
8. Distributed and Cloud Computing, Kai Hwang, Geoffery C.Fox, Jack J.Dongarra, Elsevier, 2012

(B2515) WEB SERVICES AND SERVICE ORIENTED ARCHITECTURE

(Open Elective – II, offered by CSE Dept.)

M.Tech(ES) II Semester

L	T	P	C
4	0	0	4

Course Objectives

- To give the student an understanding of the strengths and weaknesses of a service based architecture, informed by an ability to implement and deploy simple web services using a suitable development platform.
- To define and design applications as combinations of services, and be able to discuss the emergent properties of those compositions;
- To understand the research context and potential future directions for these technologies.

Course Outcomes:

On successful completion of this course, the student should be able to:

- Gain a comprehensive understanding of software oriented architectures and web services.
- Analyse and manage a modern medium scale software development project using SOA principles.
- Formulate functional testing, compliance testing and load testing of Web
- Services to Identify bug-finding ideas in testing Web Services.
- Synthesize a service oriented application that meets the business needs.

UNIT I

Evolution and Emergence of Web Services – Evolution of distributed computing. Core distributed computing technologies – client/server, CORBA, JAVA RMI, Micro Soft DCOM, MOM, Challenges in Distributed Computing, role of J2EE and XML in distributed computing, emergence of Web Services and Service Oriented Architecture (SOA). Introduction to Web Services – The definition of web services, basic operational

model of web services, tools and technologies enabling web services, benefits and challenges of using web services.

UNIT II

Web Service Architecture – Web services Architecture and its characteristics, core building blocks of web services, standards and technologies available for implementing web services, web services communication, basic steps of implementing web services. Describing Web Services – WSDL introduction, non functional service description, WSDL1.1 Vs WSDL 2.0, WSDL document, WSDL elements, WSDL binding, WSDL tools, WSDL port type, limitations of WSDL.

UNIT III

Brief Over View of XML – XML Document structure, XML namespaces, Defining structure in XML documents, Reuse of XML schemes, Document navigation and transformation. SOAP : Simple Object Access Protocol, Inter-application communication and wire protocols, SOAP as a messaging protocol, Structure of a SOAP message, SOAP envelope, Encoding, Service Oriented Architectures, SOA revisited, Service roles in a SOA, Reliable messaging, The enterprise Service Bus, SOA Development Lifecycle, SOAP HTTP binding, SOAP communication model, Error handling in SOAP.

UNIT IV

Registering and Discovering Services : The role of service registries, Service discovery, Universal Description, Discovery, and Integration, UDDI Architecture, UDDI Data Model, Interfaces, UDDI Implementation, UDDI with WSDL, UDDI specification, Service Addressing and Notification, Referencing and addressing Web Services, Web Services Notification.

UNIT V

SOA and web services security considerations, Network-level security mechanisms, Application-level security topologies, XML security standards, Semantics and Web Services, The semantic interoperability problem, The role of metadata, Service metadata, Overview of .NET and J2EE, SOA and Web Service Management, Managing Distributed System, Enterprise management Framework, Standard distributed management frameworks, Web service management, Richer schema languages, WS- Metadata Exchange.

Text Books

1. Web Services & SOA Principles and Technology, Second Edition, Michael P.Papazoglou.
2. Developing Java Web Services, R. Nagappan, R. Skoczylas, R.P. Sriganesh, Wiley India.
3. Developing Enterprise Web Services, S. Chatterjee, J. Webber, Pearson Education.

Reference Books

1. XML, Web Services, and the Data Revolution, F.P.Coyle, Pearson Education.
2. Building web Services with Java, 2nd Edition, S. Graham and others, Pearson Education.
3. Java Web Services, D.A. Chappell & T. Jewell, O'Reilly, SPD.
4. McGovern, et al., "Java web Services Architecture", Morgan Kaufmann Publishers, 2005. J2EE Wer Services, Richard Monson-Haefel, Pearson Education

(B2601) OPERATIONS RESEARCH

(Open Elective – II offered by ME Dept.)

M.Tech(ES) II Semester

L	T	P	C
4	0	0	4

UNIT – I

Development – Definition– Characteristics and Phases – Types of models – Operations Research models – applications.

Allocation: Linear Programming Problem - Formulation – Graphical solution – Simplex method – Artificial variables techniques: Two–phase method, Big-M method; Duality Principle.

UNIT – II

Transportation Problem – Formulation – Optimal solution, unbalanced transportation problem – Degeneracy

Assignment problem – Formulation – Optimal solution - Variants of Assignment Problem; Traveling Salesman problem.

UNIT – III

Sequencing – Introduction – Flow **–**Shop sequencing – n jobs through two machines – n jobs through three machines – Job shop sequencing – two jobs through 'm' machines

Replacement: Introduction – Replacement of items that deteriorate with time – when money value is not counted and counted – Replacement of items that fail completely- Group Replacement.

UNIT – IV

Theory of Games: Introduction –Terminology– Solution of games with saddle points and without saddle points- 2 x 2 games –m x 2 & 2 x n games - graphical method – m x n games - dominance principle.

Inventory: Introduction – Single item, Deterministic models – Types - Purchase inventory models with one price break and multiple price breaks –Stochastic models – demand discrete variable or continuous variable – Single Period model with no setup cost.

UNIT – V

Dynamic Programming

Introduction – Terminology- Bellman's Principle of Optimality – Applications of dynamic programming- shortest path problem – linear programming problem.

Simulation

Introduction – Types of Simulation- Event Type Simulation - Monte Carlo Technique - Applications.

Text Books

1. Operation Research /J. K. Sharma /McMilan.
2. Introduction to O.R /Taha /PHI

Reference Books

1. Operations Research: Methods and Problems / Maurice Saseini, Arhur Yaspan and Lawrence Friedman

2. Operations Research /A. M. Natarajan, P. Balasubramaniam, A. Tamilarasi/Pearson Education.
3. Operations Research / Wagner/ PHI Publications.
4. Introduction to O.R/Hillier & Libermann (TMH).

(B1219) EMBEDDED SYSTEMS LABORATORY

M.Tech(ES) II Semester

L	T	P	C
0	0	4	2

Note:

A. The following programs are to be implemented on ARM based Processors/Equivalent.
B. Minimum of 10 programs from Part –I and 6 programs from Part -II are to be conducted.

PART- I:

The following Programs are to be implemented on ARM Processor

1. Simple Assembly Program for
    a. Addition | Subtraction | Multiplication | Division
    b. Operating Modes, System Calls and Interrupts
    c. Loops, Branches
2. Write an Assembly programs to configure and control General Purpose Input/Output (GPIO) port pins.
3. Write an Assembly programs to read digital values from external peripherals and execute them with the Target board.
4. Program for reading and writing of a file
5. Program to demonstrate Time delay program using built in Timer / Counter feature on IDE environment
6. Program to demonstrates a simple interrupt handler and setting up a timer
7. Program demonstrates setting up interrupt handlers. Press button to generate an interrupt and trace the program flow with debug terminal.
8. Program to Interface 8 Bit LED and Switch Interface
9. Program to implement Buzzer Interface on IDE environment
10. Program to Displaying a message in a 2 line x 16 Characters LCD display and verify the result in debug terminal.
11. Program to demonstrate I2C Interface on IDE environment
12. Program to demonstrate I2C Interface – Serial EEPROM
13. Demonstration of Serial communication. Transmission from Kit and reception from PC using Serial Port on IDE environment use debug terminal to trace the program.
14. Generation of PWM Signal
15. Program to demonstrate SD-MMC Card Interface.

PART- II:

Write the following programs to understand the use of RTOS with ARM Processor on IDE Environment using ARM Tool chain and Library:

1. Create an application that creates two tasks that wait on a timer whilst the main task loops.
2. Write an application that creates a task which is scheduled when a button is pressed, which illustrates the use of an event set between an ISR and a task
3. Write an application that Demonstrates the interruptible ISRs(Requires timer to have higher priority than external interrupt button)
4. a).Write an application to Test message queues and memory blocks. b).Write an application to Test byte queues

5. Write an application that creates two tasks of the same priority and sets the time slice period to illustrate time slicing.

Interfacing Programs:

6. Write an application that creates a two task to Blinking two different LEDs at different timings
7. Write an application that creates a two task displaying two different messages in LCD display in two lines.
8. Sending messages to mailbox by one task and reading the message from mailbox by another task.
9. Sending message to PC through serial port by three different tasks on priority Basis.
10. Basic Audio Processing on IDE environment