

H.T No:

**R18**

Course Code: B30206



**CMR COLLEGE OF ENGINEERING & TECHNOLOGY**  
(UGC AUTONOMOUS)

M.Tech II Semester Supplementary Examinations March/April-2023

Course Name: **EMBEDDED REAL TIME OPERATING SYSTEM**

(Embedded Systems)

Date: 24.03.2023 FN

Time: 3 hours

Max.Marks: 70

(Note: Assume suitable data if necessary)

**PART-A**

Answer all FIVE questions (Compulsory)

Each question carries FOUR marks.

5x4=20M

1. What is fork and v fork and write commands? 4M
2. List out the differences between OS and RTOS. 4M
3. Explain about the Recursive locking. 4M
4. Explain the real time clocks with examples. 4M
5. Explain the important features of Vx Works for a sophisticated RTOS. 4M

**PART-B**

Answer the following. Each question carries TEN Marks.

5x10=50M

6. A). Explain: i) open, ii) Lseek, iii) exit, iv) wait and v) waitpid. 10M
- OR**
6. B). What are OS services? Explain the structures of user and supervisory mode. 10M
7. A). What are the different types of scheduling strategies used in RTOS? Explain briefly? 10M
- OR**
7. B). i) Explain the communication and concurrency with examples. 5M  
ii) Explain the synchronization and task operation with examples. 5M
8. A). Explain the creation and activation of a task by task spawn function in VxWorks. For task priority function, Define 3 options on spawning. 10M
- OR**
8. B). i) Explain the basics I/O concepts with examples. 5M  
ii) Differentiate process and thread and define task and explain with diagram all the five states of task. 5M
9. A). i) Explain the Interrupt service routines in an RTOS. 5M  
ii) Explain the interrupts, spurious interrupts with examples. 5M
- OR**
9. B). Demonstrate about weighted round-robin approach for scheduling real-time systems with an example. 10M
10. A). Explain the block diagram of Automatic Chocolate Vending Machine System (ACVM). 10M
- OR**
10. B). Write and elaborate the coding for sending application layer byte stream on a TCP/IP network using RTOS Vx works. 10M

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H.T No:

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**R18**

Course Code: B30221



**CMR COLLEGE OF ENGINEERING & TECHNOLOGY**  
(UGC AUTONOMOUS)

**M.Tech II Semester Supplementary Examinations March/April-2023**

**Course Name: DIGITAL SYSTEM DESIGN**

**(Embedded Systems)**

**Date: 28.03.2023 FN**

**Time: 3 hours**

**Max.Marks: 70**

**(Note: Assume suitable data if necessary)**

**PART-A**

**Answer all FIVE questions (Compulsory)**

**Each question carries FOUR marks.**

**5x4=20M**

1. What are the limitations and capabilities of FSM? 4M
2. What are differences between PLA and PAL? 4M
3. What are the principal components of State machine chart? 4M
4. Explain bridging fault model. 4M
5. What is meant by Circuit test approach? 4M

**PART-B**

**Answer the following. Each question carries TEN Marks.**

**5x10=50M**

6. A). Find the equivalence partition and a corresponding reduced machine in a standard form for the machine shown below. 10M

PS	NS,Z	
	X=0	X=1
A	F,0	B,1
B	G,0	A,1
C	B,0	C,1
D	C,0	B,1
E	D,0	A,1
F	E,1	F,1
G	E,1	G,1

**OR**

6. B). A fundamental mode sequential machine has two inputs,  $x_1$  and  $x_2$ , and one output,  $z_1$ .  $z_1$  becomes 1 if and only if the input state is  $x_1=x_2=1$  and the preceding input combination is  $x_1=0$  and  $x_2=1$ . Derive a minimum-row state table. 10M

7. A). Implement a BCD to Gray code converter on a PLA. 10M

**OR**

7. B). Design a 32-bit Adder. 10M

8. A). Realize the state machine chart for dice controller. 10M

**OR**

8. B). With an example, explain the use of ASM charts in the design of digital circuits. 10M

**(P.T.O.)**

9. A). i) Explain the Stuck at faults with an example. 5M  
ii) Draw the circuit which realizes the logic function  $z = x_1 x_2 + x_3 x_4$  using AND and OR gates. For the circuits realized above, determine a test vector which denotes SA0 fault on the line 'x2'. 5M

**OR**

9. B). i) What is the significance of Kohavi algorithm? Explain how it is useful in the detection of faults in digital circuits. 5M  
ii) Apply Kohavi's algorithm to the given POS function  $f = (A + \bar{B})(C + BD)$ . 5M

10. A). Explain about fault detection experiment. 10M

**OR**

10. B). Explain about transition test approach with an example. 10M

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