H.T No: | | | | | | | | | | | **R22** **Course Code: B455303**

CMR COLLEGE OF ENGINEERING & TECHNOLOGY

(UGC AUTONOMOUS)

M.Tech II Semester Regular Examinations September-2023

Course Name: ARM MICROCONTROLLERS

(Embedded Systems)

Date: 04.09.2023 FN **Time: 3 hours** **Max.Marks: 60**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions (Compulsory)

Each question carries ONE mark. **10x1=10M**

1. Write Embedded system hardware and software. 1 M
2. Write about ARM -APSR instructions. 1 M
3. What is Thumb state? 1 M
4. Write a short note on long multiplication. 1 M
5. Distinguish between Cross Compiler and Cross Assembler. 1 M
6. Explain the segment memory management scheme. 1 M
7. What are the instruction dependencies in ARM? Explain each briefly. 1 M
8. Write a short note on UAL. 1 M
9. Write a short note on Cortex –M4 FPU. 1 M
10. Explain FMUL and FMULP instructions. 1 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A). Discuss in detail the hardware fundamentals of the actual ARM processor. 10M

OR

11. B). Explain the 3-stage pipeline ARM organization. 10M

12. A). Explain the Interrupt service routines (ISRs). What are the advantages of ISR? 10M

OR

12. B). Explain ARM design methodology requirements analysis. 10M

13. A). Briefly explain the data processing instructions for ARM processor 10M

OR

13. B). Describe in detail the following Thumb instructions: i) Register usage instructions and ii) Single-register load-store instructions 10M

14. A). What is context switching? With figure and assembly code explain two stages of the context switch. 10M

OR

14. B). Comparison of the instruction set in ARM Cortex-M Processors. 10M

15. A). Mention useful techniques for optimizing ARM assembly, and briefly explain them. 10M

OR

15. B). Discuss the role of LI and L2 cache memories in ARM processor. 10M

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H.T No: | | | | | | | | | | | **R22** **Course Code: B455304**

CMR COLLEGE OF ENGINEERING & TECHNOLOGY

(UGC AUTONOMOUS)

M.Tech II Semester Regular Examinations September-2023

Course Name: DIGITAL CONTROL SYSTEMS

(Embedded Systems)

Date: 06.09.2023 FN **Time: 3 hours** **Max.Marks: 60**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions (Compulsory)

Each question carries ONE mark. **10x1=10M**

1. Show the relation between s-place and z-plane. 1 M
2. What are the shortcomings of ZOH? 1 M
3. Outline the properties State Transition matrix. 1 M
4. Define controllability and observability. 1 M
5. Identify the methods of testing the stability of digital control system? 1 M
6. Interpret Zero-input stability. 1 M
7. Illustrate the equation describing the idealized non-interacting PID controller. 1 M
8. What is the only design parameter in deadbeat control? 1 M
9. Define the types of state observers. 1 M
10. Write the Ackerman's formula. 1 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A). The input output of a sampled data system is described by the difference equation $y(k+2)+2y(k+1)+4y(k)=r(k)$ determine the pulse transfer function. 10M

OR

11. B). What is meant by zero order hold? Derive the transfer function of zero order hold device. 10M

12. A). Discuss the duality between controllability and observability. 10M

OR

12. B). Examine whether the discrete data system given below is 10M

$$X(k+1) = \begin{bmatrix} 0 & 1 \\ -2 & -2 \end{bmatrix} X(k) + \begin{bmatrix} 1 \\ -1 \end{bmatrix} u(k) \; ; y(k) = [1 \quad 0] X(k)$$

(i) State controllable (ii) Output controllable (iii) Observable

13. A). Using bilinear transformation, explain the design procedure of lag and lead Compensators. 10M

OR

13. B). Using Jury stability criterion, find if all the poles of the following transfer function lie inside the unit circle on the z-plane. 10M

$$G(z) = \frac{3z^4+2z^3-z^2+4z+5}{z^4+0.5z^3-0.2z^2+z+0.4}$$

(P.T.O..)

14. A). Consider the system $X(k+1) = \begin{bmatrix} 0 & 1 \\ -0.16 & -1 \end{bmatrix} X(k) + \begin{bmatrix} 0 \\ 1 \end{bmatrix} u(k)$; 10M

$y(k) = [1 \quad 1] X(k)$

Design a current observer for the system. It is desired that the response to the initial observer error be deadbeat.

OR

14. B). Explain the design procedure of digital PID controllers. 10M

15. A). Illustrate any two methods of pole-placement for design of digital controller. 10M

OR

15. B). Discuss the necessary conditions for design of state feedback controller through pole placement. 10M

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H.T No: | | | | | | | | | | | R22 | Course Code: B455408

CMR COLLEGE OF ENGINEERING & TECHNOLOGY

(UGC AUTONOMOUS)

M.Tech II Semester Regular Examinations September-2023

Course Name: DESIGN FOR TESTABILITY

(Embedded Systems)

Date: 08.09.2023 FN **Time: 3 hours** **Max.Marks: 60**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions (Compulsory)

Each question carries ONE mark. **10x1=10M**

1. Define the role of testing and role of diagnosis in VLSI. 1 M
2. Define the terms defect and fault. 1 M
3. What is the application of logic level modeling and simulation? 1 M
4. What are the signal values used at circuit level modeling and simulation? 1 M
5. What is 0-controllability(C0)? 1 M
6. Define the length of a sequential path. 1 M
7. Define degree of parallelism. 1 M
8. Define fault coverage. 1 M
9. List boundary scan registers. 1 M
10. Define noninvasive mode of boundary scan. 1 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A). How do you address bridging and delay faults? 10M

OR

11. B). Explain Single stuck – Fault model with an example. 10M

12. A). Explain concurrent Fault Simulation and deductive fault simulation procedures. 10M

OR

12. B). Explain what action an event-driven true-value simulator will take when it evaluates a zero-delay gate. 10M

13. A). i) Explain generic scan-based designs. 5M
ii) Explain the level sensitive scan design rules 5M

OR

13. B). i) What is Transition-count compression? Elaborate. 5M
ii) Write a brief note on BILBO architecture. 5M

14. A). Write a short notes on generic off line BIST Architectures 10M

OR

14. B). Discuss on A concurrent BIST Architecture with neat sketch. 10M

15. A). Draw and explain TAP controller state diagram and timing diagram 10M

OR

15. B). i) Explain control-and -observe scan cell method. 5M
ii) Discuss BSDL pin descriptions. 5M

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H.T No: | | | | | | | | | | | R22 | Course Code: B455410

CMR COLLEGE OF ENGINEERING & TECHNOLOGY

(UGC AUTONOMOUS)

M.Tech II Semester Regular Examinations September-2023

Course Name: HARDWARE & SOFTWARE CO-DESIGN

(Embedded Systems)

Date: 11.09.2023 FN | Time: 3 hours | Max.Marks: 60

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions (Compulsory)

Each question carries ONE mark. 10x1=10M

1. List the types of Architectures. 1 M
2. Explain the need of co-synthesis. 1 M
3. Draw the Architecture of VLIW. 1 M
4. Explain data flow graph. 1 M
5. Define compiler. 1 M
6. Define ASIC. 1 M
7. What is Emulation? 1 M
8. Draw the Architecture of FPGA based emulation. 1 M
9. Define co-design. 1 M
10. Define scheduling. 1 M

PART-B

Answer the following. Each question carries TEN Marks. 5x10=50M

11.A). Explain Data path Architecture and its working principle. 10M

OR

11. B). Draw the flow graph of Cosyma and explain the working of each block. 10M

12. A). Draw and explain the block diagram of prototyping and emulation techniques. 10M

OR

12. B). Explain Aptix prototyping systems with neat diagrams 10M

13. A). Draw the architecture of CISC and explain. 10M

OR

13. B). Explain the architecture of parallel processor. 10M

14. A). Explain system specialization techniques. 10M

OR

14. B). Explain design and co-design computation models. 10M

15. A). Explain Target Architectures and application system classes. 10M

OR

15. B). Draw the flow graph of Cosyma and explain the working of each block. 10M

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