H.T No: | | | | | | | | | | | **R18** | Course Code: A30506

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(UGC AUTONOMOUS)
B.Tech III Semester Supplementary Examinations February-2024
Course Name: DISCRETE MATHEMATICS
(Common for CSE, IT, CSC, CSM, CSD, AID & AIM)

Date: 05.02.2024 AN **Time: 3 hours** **Max.Marks: 70**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions (Compulsory)

Each question carries TWO marks. **10x2=20M**

1. Draw the hasse diagram for the poset (P(x), ≤) where x={1,2,3,4} and ≤ ={(x,y)/ x is subset to y} 2 M
2. How do you prove Schroeder Bernstein Theorem? 2 M
3. State the pigeonhole principle. 2 M
4. Given the polynomial $p(x) = x^2 + x + 5$ and $g(x) = x + 2$. Find the value of q(x) and r(x). 2 M
5. Show that $p \rightarrow q \equiv \sim p \vee q$ using truth table. 2 M
6. Write the existential quantifier in terms of universal quantifier. 2 M
7. What is permutation group? Give an example. 2 M
8. Differentiate disjunctive and conjunctive Normal forms. 2 M
9. What is Hamiltonian Graph? 2 M
10. What is meant by articulation point? 2 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A). Define an equivalence relation and show that the relation R defined as aRb iff 4 divides (a-b) over set of integers is an equivalence relation. 10M

OR

11. B). Show that (D_{30}, R), where a R b If and only if a divides b, is a complemented lattice. D_{30} is set of positive divisors of 30. 10M

12. A). Explain the Euclidian algorithm with an example. 10M

OR

12. B). Suppose that the license plates of certain state require 3 English letters followed by 4 digits: 10M
   a) How many different plates can be manufactured if repetition of letters and digits allowed.
   b) How many plates are possible if only letters can be repeated.
   c) How many are possible if no repetitions are allowed at all.

13. A). By using logic equivalence prove or disprove $(\sim p(p \vee q)) \rightarrow q \equiv T$. 10M

OR

13. B). Obtain the principal disjunctive normal form of $(P \wedge Q) \vee (\sim P \wedge R) \vee (Q \wedge R)$. 10M

(P.T.O..)

14. A). What is a group show that addition modulo 5 is a group? 10M

OR

14. B). List out the identities of Boolean algebra. 10M

15. A). Show that K_5 is non-planar. 10M

OR

15. B). Define isomorphism of graph. Justify that the graph $K_{2,3}$ Is a planar graph. 10M

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H.T No: | | | | | | | | | | | R18 | Course Code: A30461

CMR COLLEGE OF ENGINEERING & TECHNOLOGY

(UGC AUTONOMOUS)

B.Tech III Semester Supplementary Examinations February-2024

Course Name: ANALOG & DIGITAL ELECTRONICS

(Common for CSE & IT)

Date: 07.02.2024 AN | Time: 3 hours | Max.Marks: 70

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions (Compulsory)

Each question carries TWO marks. 10x2=20M

1. List the differences between ideal diode and practical diode. 2 M
2. Define transition capacitance. 2 M
3. Draw the symbols of NPN and PNP transistor. 2 M
4. Explain about the various regions in a transistor. 2 M
5. How a FET can be used as a voltage variable Resistance (VVR)? 2 M
6. Discuss octal number system. 2 M
7. Show both NAND and NOR gates are called Universal gates. 2 M
8. Analyze the steps for simplification of POS expression. 2 M
9. Illustrate applications of shift registers. 2 M
10. Define race around condition? How it can be avoided. 2 M

PART-B

Answer the following. Each question carries TEN Marks. 5x10=50M

11.A). Explain the V-I characteristics of Zener diode and distinguish between Avalanche and Zener Break downs. 10M

OR

11. B). Draw the circuit of bridge rectifier and explain its operation with the help of input and output waveforms. 10M

12. A). Explain the constructional details of Bipolar Junction Transistor. 10M

OR

12. B). Discuss the construction, principle of operation, characteristics and applications of UJT. 10M

13. A). Explain the operation of FET with its characteristics and explain the Different regions in transfer characteristics. 10M

OR

13. B). i) Solve the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend: 6M

(a) 100 – 110000 (b) 11010 - 1101

ii) Construct a table for 4 -3 -2 -1 weighted code and write 9154 using this code. 4M

(P.T.O..)

14. A). Simplify the following Boolean expressions using K-map and implement them using NOR gates: 10M

F (W, X, Y, Z) = W'X'Y'Z' + WXY'Z' + W'X'YZ + WXYZ.

OR

14. B). i) Construct the logic diagram of a full subtractor using only 2-Input NAND gates. 8M

ii) Explain the properties of EX-OR gate. 2M

15. A). Design a 4-bit BCD Ripple Counter by using T-FF. 10M

OR

15. B). Explain the state reduction and state assignment in designing Sequential circuit. Consider one example in the above process. 10M

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H.T No: | | | | | | | | | | | **R18** | Course Code: A30513

CMR COLLEGE OF ENGINEERING & TECHNOLOGY

(UGC AUTONOMOUS)

B.Tech III Semester Supplementary Examinations February-2024

Course Name: COMPUTER ORGANIZATION & ARCHITECTURE

(Common for CSE, IT, CSC, CSM, AID & AIM)

Date: 09.02.2024 AN **Time: 3 hours** **Max.Marks: 70**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions (Compulsory)

Each question carries TWO marks. **10x2=20M**

1. Define computer organization of a digital computer. 2 M
2. Write Basic symbols for register transfer. 2 M
3. Differentiate between restoring and non-restoring division algorithm. 2 M
4. Represent the number $(+37.8)_{10}$ as a floating point binary number with normalized fraction mantissa 16 bits and exponent 8 bits. 2 M
5. What is the need of I/O interface? 2 M
6. Why does DMA have priority over the CPU when both request a memory transfer? 2 M
7. Define pipelining. 2 M
8. List the pipeline hazards. 2 M
9. What is cache memory? 2 M
10. What is meant by memory interleaving? 2 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A). i) Explain about Bus and Memory Transfer. 5M

ii) Explain about Computer instructions. 5M

OR

11. B). i) Describe Instruction cycle in computer system. 5M

ii) A Computer uses a memory unit with 256 K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address 5M

part.

(a) How many bits are there in the operation code, the

register code part, and the address part?

(b) Draw the instruction word format and indicate the

number of bits in each part.

(c) How many bits are there in the data and address inputs of the memory?

12. A). i) Explain the process of floating point number multiplication with flow chart. 5M

ii) Show the hardware for a 2 bit-by-2 bit array multiplier and explain its working. 5M

OR

12. B). i) Using booth's multiplication algorithm, multiply the 3 X -4, show all the steps. 7M

ii) What is the principle of carry look-ahead adder? 3M

(P.T.O..)

13. A). With a neat block diagram, explain the architecture of 8086 Microprocessor. 10M

OR

13. B). i) What is interrupt? Why priority of interrupt is required? How it is restored? 5M

ii) Give the comparison between programmed I/O and interrupt driven I/O. 5M

14. A). Name the two pipeline organizations. Explain about the arithmetic pipeline with the help of an example. 10M

OR

14. B). Explain instruction pipeline with neat timing diagram. 10M

15. A). Draw and explain fully associative cache organization. 10M

OR

15. B). Explain various page replacement algorithms. 10M

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H.T No: | | | | | | | | | | | **R18** | Course Code: A30507

CMR COLLEGE OF ENGINEERING & TECHNOLOGY

(UGC AUTONOMOUS)

B.Tech III Semester Supplementary Examinations February-2024

Course Name: OBJECT ORIENTED PROGRAMMING

(Common for CSE & IT)

Date: 12.02.2024 AN | **Time: 3 hours** | **Max.Marks: 70**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions (Compulsory)

Each question carries TWO marks. **10x2=20M**

1.	Define Object Oriented Programming.	2 M
2.	What is Package. List out the predefined packages.	2 M
3.	Define Exception. List out the types of exceptions	2 M
4.	What is static inner class.	2 M
5.	Define Thread. List out the states of Thread.	2 M
6.	Define File.	2 M
7.	Differentiate between Array and List.	2 M
8.	Define String Tokenizer.	2 M
9.	What is an Event? Represent the relationship between event Source and event Listener.	2 M
10.	Define Adapter Class.	2 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A).	Explain multilevel inheritance with an example.	10M
	OR	
11. B).	Explain overloading and overriding with an example.	10M
12. A).	Explain different types of inner classes with example.	10M
	OR	
12. B).	Explain the classification of exceptions with example.	10M
13. A).	Distinguish between multiple process and multiple threads.	10M
	OR	
13. B).	Describe inter thread communication.	10M
14. A).	Write a note on java collection framework.	10M
	OR	
14. B).	What is enumeration and iterator explain with example.	10M
15. A).	Describe hierarchy of Swing and Scala components.	10M
	OR	
15. B).	Write a java program to implement Mouse Events	10M

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H.T No: | | | | | | | | | | | **R18** | **Course Code: A30509**

CMR COLLEGE OF ENGINEERING & TECHNOLOGY

(UGC AUTONOMOUS)

B.Tech III Semester Supplementary Examinations February-2024

Course Name: DATABASE MANAGEMENT SYSTEMS

(Common for CSE, IT, CSC, CSD & AID)

Date: 14.02.2024 AN **Time: 3 hours** **Max.Marks: 70**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions (Compulsory)

Each question carries TWO marks. **10x2=20M**

1.	What is DBMS? What are the advantages of DBMS.	2 M
2.	How to represent the strong entity set and weak entity set in ER-Model?	2 M
3.	Define the terms: Relational Databases, Tables.	2 M
4.	Define the form of basic SQL query.	2 M
5.	List the primitive operators in Relational algebra.	2 M
6.	What is schema refinement.	2 M
7.	Define Serializability.	2 M
8.	What is the motivation for concurrent execution?	2 M
9.	What is an index? Give an example.	2 M
10.	Define un clustered index.	2 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A).	Explain conceptual design with E-R model and Draw an E-R Diagram that illustrates the Banking System.	10M
	OR	
11. B).	Explain the architecture of DBMS with a neat diagram and note its scope.	10M
12. A).	What is a relation? Differentiate between a relation schema and relation instance? What are domain constraints, Discuss.	10M
	OR	
12. B).	Illustrate the Set comparison operators and Aggregation operators with example.	10M
13. A).	i) Discuss in detail about the operations of relation algebra with example. ii) Compare Super key, Candidate key, Primary Key for a relation with example.	5M 5M
	OR	
13. B).	What is redundancy? Explain the problems caused by redundancy with suitable example.	10M
14. A).	i)What is Transaction? Explain the properties of Transaction. ii) Give an overview of Validation Based Protocol.	5M 5M
	OR	
14. B).	Explain the concept of Serializability and Recoverability with example.	10M
15. A).	State and explain various file organization methods. Give suitable examples to each of them.	10M
	OR	
15. B).	Explain about indexed sequential access methods in detail.	10M

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