H.T No: | | | | | | | | | | | R22 | Course Code: A405308

CMR COLLEGE OF ENGINEERING & TECHNOLOGY

(UGC AUTONOMOUS)

B.Tech III Semester Regular Examinations February-2024

Course Name: SOFTWARE ENGINEERING

(Common for CSE, CSM & AIM)

Date: 05.02.2024 AN | Time: 3 hours | Max.Marks: 60

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions (Compulsory)

Each question carries ONE mark. 10x1=10M

1.	What is Software Engineering?	1 M
2.	List the types of software models.	1 M
3.	What are kinds of non-functional requirements?	1 M
4.	What is feasibility study?	1 M
5.	Write about class diagram with an example.	1 M
6.	List the design concepts.	1 M
7.	Define Alpha testing.	1 M
8.	List the metrics for the design model.	1 M
9.	Write about software risks.	1 M
10.	What is software reliability?	1 M

PART-B

Answer the following. Each question carries TEN Marks. 5x10=50M

11.A).	Explain in detail the capability Maturity Model Integration (CMMI)?	10M
	OR	
11. B).	i) Discuss in brief about the waterfall model.	5M
	ii) Explain the Spiral model in detail with a neat sketch.	5M
12. A).	i) Describe five desirable characteristics of a good software requirement specification document.	5M
	ii) What are the types of requirement validation?	5M
	OR	
12. B).	i) Compare functional requirements with nonfunctional requirements.	5M
	ii) Explain about requirements management phases of requirement engineering process.	5M
13. A).	What are the design principles of a good software design? Explain.	10M
	OR	
13. B).	i) Explain the architectural patterns.	5M
	ii) Explain the guidelines of component level design.	5M
14. A).	i) What is testing? How is it different from debugging?	2M
	ii) What is integration testing? Explain in detail about types of integration testing.	8M

(P.T.O..)

OR

14. B). i) Differentiate between black box and white box testing? 5M
ii) Discuss about metrics for testing in detail. 5M

15. A). i) List and explain the various software quality factors. 5M
ii) Reactive vs proactive risk strategies. 5M

OR

15. B). i) Illustrate in detail ISO 9000 quality standards. 5M
ii) Discuss about RMMM Plan. 5M

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H.T No: | | | | | | | | | | | R22 | Course Code: A404204

CMR COLLEGE OF ENGINEERING & TECHNOLOGY

(UGC AUTONOMOUS)

B.Tech III Semester Regular Examinations February-2024

Course Name: DIGITAL ELECTRONICS

(Common for CSE, CSC & IT)

Date: 07.02.2024 AN **Time: 3 hours** **Max.Marks: 60**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions (Compulsory)

Each question carries ONE mark. **10x1=10M**

1.	Convert (46AD)16 to octal number system.	1 M
2.	Draw the symbol of universal gates.	1 M
3.	Draw AND gate using universal NAND gate.	1 M
4.	What are don't cares? What is the use of these?	1 M
5.	What is the use of HDL?	1 M
6.	What is multiplexers?	1 M
7.	Compare latch and flip-flops.	1 M
8.	What are the advantages of sequential circuits?	1 M
9.	What is ROM?	1 M
10.	What is the use of reduction state?	1 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A). Translate the following numbers as indicated: 10M
i) (4350)5 = ( )2
ii) (11010011)2 = ( )16
iii) (552)6 = ( )8
iv) (1001001.011)2 = ( )10
v) (2AC5.D)16 = ( )10

OR

11. B). Use Boolean theorems and properties to reduce the following Boolean expression: 10M
i) (A+B+C) (B'+C) + (A+D)(A'+C).
ii) (A+B)(A+B')(A'+B).

12. A). Simplify the following expressions using K-Map and realize with NAND and NOR gates. 10M
F = πM (1, 2, 3, 8, 9, 10, 11, 14). πd (7,15)

OR

12. B). Minimize the following Boolean functions using K-map and draw the logic diagram using NAND gates. 10M
F (A,B,C,D) =Σ*m* (1,3,5,8,9,11,15) +d (2,13)

13. A). Draw the combinational circuit for half subtractor and full subtractor. 10M

OR

13. B). Design Four-bit magnitude comparator gate level circuit. 10M

(P.T.O..)

14. A). Explain the JK flip-flop and D flip flop with the help of circuit diagram, graphic symbol and characteristic table. 10M

OR

14. B). Explain in detail about registers and counters with an example. 10M

15. A). Construct the PLA for the following Boolean function: 10M
(i) F1= $\Sigma m(0,1,3,4)$ (ii) F2 = $\Sigma m(0,1,2,3,4,5)$.

OR

15. B). Design a gated latch circuit with 2 inputs G and D, one output Q. The gated latch is a memory element that accepts the value of D when G=1 and retains this value after G goes to 0. One G=0 a change in D doesn't change the value of output Q. 10M

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H.T No: | | | | | | | | | | | R22 | Course Code: A404203

CMR COLLEGE OF ENGINEERING & TECHNOLOGY

(UGC AUTONOMOUS)

B.Tech III Semester Regular Examinations February-2024

Course Name: ELECTRONICS DEVICES AND CIRCUITS

(Common for CSE, IT, CSC, CSM, CSD & AID)

Date: 09.02.2024 AN **Time: 3 hours** **Max.Marks: 60**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions (Compulsory)

Each question carries ONE mark. **10x1=10M**

1. Show the circuit diagram of the PN junction diode under the forward biased condition. 1 M
2. Recall the PN junction diode current equation. 1 M
3. List the two applications of rectifiers. 1 M
4. Show the circuit diagram of the bridge rectifier. 1 M
5. What is the relationship between α and β of a transistor? 1 M
6. Show the circuit diagram of a transistor when it is in the active region. 1 M
7. What is the Shockley equation of a junction field effect transistor? 1 M
8. Define the pinch-off voltage of a JFET. 1 M
9. Show the circuit diagram of a Zener diode as a voltage regulator. 1 M
10. Show the symbol of a UJT. 1 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A). Explain the operation of a PN junction diode under forward and reverse biased conditions with the help of suitable diagrams. 10M

OR

11. B). Illustrate the forward and reverse characteristics of a PN junction diode and also write the equations for static and dynamic resistances. 10M

12. A). Explain the operation of a full-wave rectifier with a suitable diagram and also derive the expressions for the average DC load current and the RMS value of the load current. 10M

OR

12. B). Determine the power delivered to the load, the percentage of regulation at full load, the rectification efficiency, and the secondary's TUF when a transformer with a center-tapped secondary winding feeds a full wave rectifier circuit. From either end of the secondary to the center tap, the rms voltage is 25V.Given a load of 2kΩ and a diode with a forward resistance of 4Ω and a secondary resistance of 10Ω. 10M

13. A). Explain the input and output characteristics of a common-emitter configuration with a suitable diagram. 10M

OR

13. B). Determine the current will flow in the collector circuit of this transistor when connected in CE configuration with a base current of 30μA when a transistor operating in CB configuration has $I_C = 2.98mA$, $I_E = 3mA$ and $I_{CO} = 0.01mA$. 10M

(P.T.O.)

14. A). Construct an n-channel JFET and explain its operation in detail with a suitable diagram. 10M

OR

14. B). Choose a datasheet of a JFET gives the following information: I_{DSS} = 4mA, $V_{GS\,(off)}$ = -9V and $g_{m(max)}$ = 4000μs. Determine the transconductance for V_{GS} = -3V and find drain current I_D at this point. 10M

15. A). Construct and explain the workings of LEDs in detail with a suitable diagram. 10M

OR

15. B). Construct and explain the workings of a tunnel diode in detail with a suitable diagram. 10M

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H.T No: | | | | | | | | | | | R22 | Course Code: A405303

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(UGC AUTONOMOUS)

B.Tech III Semester Regular Examinations February-2024

Course Name: OBJECT ORIENTED PROGRAMMING THROUGH JAVA

(Common for CSE, CSC & CSD)

Date: 12.02.2024 AN | **Time: 3 hours** | **Max.Marks: 60**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions (Compulsory)

Each question carries ONE mark. **10x1=10M**

1. What is meant by JVM. 1 M
2. Define constructor. 1 M
3. What is substitutability? 1 M
4. Define interface. 1 M
5. What is meant by Exception. 1 M
6. Define Daemon thread. 1 M
7. How to create check box? 1 M
8. Define frame. 1 M
9. What is meant by application. 1 M
10. Define JDBC. 1 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A). List and explain Java Buzz words. 10M

OR

11. B). i) Write a java program to count the number of digits present in a string. 5M
ii) Write a java program to print prime numbers of a given number. 5M

12. A). List out forms of inheritance? Explain construction form of inheritance with an example program 10M

OR

12. B). Solve the issue of multiple inheritances with the help of interface. 10M

13. A). Write a program to implement exception handling using try with three catch blocks and one finally block. 10M

OR

13. B). Solve the given problem using synchronization of threads: Thread A should write the contents into a file. Thread B should read the contents from the file. The content written by Thread A and the content read by Thread B should be displayed on the screen. 10M

14. A). What is the significance of Layout Managers? Discuss any two Layout Managers with an example program. 10M

OR

14. B). i) Write a program to accept two numbers in text fields and print result in third textfield when add button is clicked using AWT. 5M
ii) Explain about Tabbed Panes with an example. 5M

(P.T.O...)

15. A). Write a java program to illustrate key events. 10M

OR

15. B). Write a Java program to demonstrate the Life Cycle of an applet. 10M

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H.T No: | | | | | | | | | | | R22 | Course Code: A405304

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CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(UGC AUTONOMOUS)

B.Tech III Semester Regular Examinations February-2024

Course Name: DATABASE MANAGEMENT SYSTEMS

(Common for CSE, CSC & CSD)

Date: 14.02.2024 AN | **Time: 3 hours** | **Max.Marks: 60**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions (Compulsory)

Each question carries ONE mark. **10x1=10M**

1. Differentiate between schema and data model. 1 M
2. Give an example for total participation and partial participation. 1 M
3. List the types of Data Integrity. 1 M
4. What is Domain Relational calculus? 1 M
5. Differentiate between Trigger and view. 1 M
6. Define Functional Dependency. 1 M
7. Define Transaction 1 M
8. What is multiple granularity locking? 1 M
9. What is hashing? Give an Example. 1 M
10. What are the advantages of using tree structured indexes? 1 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A). What is data independence? Explain the different types of data independence. 10M

OR

11. B). State and explain additional features of E-R models. 10M

12. A). What is the purpose of integrity constraints? Discuss integrity constraints briefly. 10M

OR

12. B). Write short notes on difference, union, rename and cartesian product operations in relational algebra. 10M

13. A). Consider following schema and write SQL for given statements. 10M

Student (Rollno, Name, Age, Sex, City)

Student_marks (Rollno, Sub1, Sub2, Sub3, Total, Average)

Write query to

i). Calculate and store total and average marks from Sub1, Sub2 & Sub3.

ii). Display name of students who got more than 60 marks in subject Sub1.

iii). Display name of students with their total and average marks.

iv). Display name of students who got equal marks in subject Sub2.

OR

13. B). Compare the following normal forms with examples. 10M

i). 3NF and BCNF

ii). 4NF and 5NF.

(P.T.O..)

14. A). Discuss about Conflict serializability and view serializability. 10M

OR

14. B). Demonstrate the concepts of Log Based Recovery and Recovery with Concurrent Transactions. 10M

15. A). What are the indexed data structures? Describe them briefly. 10M

OR

15. B). What is the limitation of index-sequential file? Explain with example how B+ tree overcomes it. 10M

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