CMR COLLEGE OF ENGINEERING &TECHNOLOGY

(UGC Autonomous)

Kandlakoya, Medchal Road, Hyderabad – 501401

ACADEMIC REGULATIONS - R 22

Academic Regulations of M. Tech (Regular/Full Time) Programmes, 2022-23 (R22) CBCS)

(Effective for the students admitted into I Year from the Academic Year 2022-23)

1.0 Post-Graduate Degree Programmes in Engineering & Technology (PGP in E & T)

CMR College of Engineering & Technology (CMRCET) offers **Two** Years (**Four** Semesters) full-time Master of Technology (M.Tech.) Degree Programmes, under Choice Based Credit System (CBCS) in different branches of Engineering and Technology with different specializations.

2.0 Eligibility for Admissions

2.1 Admission to the PGPs shall be made subject to eligibility, qualification and specializations prescribed by the University from time to time, for each specialization under each M.Tech programme.

2.2 Admission to the post graduate programme shall be made on the basis of either the merit rank or Percentile obtained by the qualified student in the relevant qualifying GATE Examination/ the merit rank obtained by the qualified student in an entrance test conducted by Telangana State Government (PGECET) for M. Tech. programmes / an entrance test conducted by JNTUH/ on the basis of any other exams approved by the University, subject to reservations as laid down by the Govt. from time to time.

2.3 The medium of instructions for all PG Programmes will be **ENGLISH** only.

3.0 M. Tech. Programme (PGP in E & T) Structure

3.1 The M. Tech. Programs in E & T of CMRCET are of Semester pattern, with **Four** Semesters consisting of **Two** academic years, each academic year having **Two** Semesters (First/Odd and Second/Even Semesters). Each Semester shall be of 22 weeks duration (inclusive of Examinations), with a minimum of 90 instructional days per Semester.

3.2 The two-year M. Tech. program consists of **68** credits and the student has to register for all **68** credits and earn all **68** credits for the award of M. Tech. degree. There is **NO** exemption of credits in any case.

3.3 The student shall not take more than four academic years to fulfill all the academic requirements for the award of M. Tech. degree from the date of commencement of first year first semester, failing which the student shall forfeit the seat in M. Tech. programme.

3.4 UGC/AICTE specified definitions/descriptions are adopted appropriately for various terms and abbreviations used in these PG academic regulations, as listed below:

3.4.1 Semester Scheme

Each Semester shall have 'Continuous Internal Evaluation (CIE)' and 'Semester End Examination (SEE)'. Choice Based Credit System (CBCS) and Credit Based Semester System (CBSS) are taken as 'references' for the present set of Regulations. The terms 'SUBJECT' and 'COURSE' imply thesame meaning here and refer to 'Theory Subject', or

'Lab Course', or 'Design/Drawing Subject', or 'Mini Project with Seminar', or 'Dissertation', as the case may be.

3.4.2 Credit Courses

All subjects/courses are to be registered by the student in a semester to earn credits which shall be assigned to each subject/course in an L: T: P: C (Lecture Periods: Tutorial Periods: Practical Periods: Credits) structure based on the following general pattern:

- One credit for one hour/week/semester for theory/lecture (L) courses
- One credit for two hours/ week/semester for laboratory/ practical (P) courses or tutorials (T)

Other student activities like study tour, guest lecture, conference/workshop participations, technical paper presentations and mandatory courses (Non-credit Audit Courses) will not carry any credits.

3.4.3 Subject Course Classification

All subjects/courses offered for the Post-Graduate Programme in E & T (M.Tech. Degree Programme) are broadly classified as follows. The University has followed in general the guidelines issued by AICTE/UGC.

S. No.	Broad Course Classification	Course Group/ Category	Course Description
1	Core Courses (CoC)	PCC- Professional Core Course	Includes subjects related to the parent discipline/department/ branch of Engineering
		Dissertation	M. Tech. Project or PG Project or Major Project
		Mini Project with Seminar	Seminar based on core contents related to ParentDiscipline/ Department/ Branch of Engineering
2	Elective Courses (EE)	PEC - Professional Electives Course	Includes elective subjects related to the parentdiscipline/department/branch of Engineering
		OEC - Open Electives Course	Elective subjects which include inter-disciplinary subjects or subjects in an area outside the parent discipline/department/ branch of Engineering
3	***Mandatory Courses***	--	***Non-Credit Audit Courses***

4.0 Course Registration

4.1 A 'Faculty Advisor or Counselor' shall be assigned to each specialization, who will advise on the Post Graduate Programme (PGP), its Course Structure and Curriculum, Choice/Option for Subjects/ Courses, based on his competence, progress, pre-requisites and interest.

4.2 The Academic Section of the College invites 'Registration Forms' from students within 15 days from the commencement of class work. The Registration Requests for any 'CURRENT SEMESTER' shall be completed BEFORE the commencement of SEEs

(Semester End Examinations) of the 'PRECEDING SEMESTER'.

4.3 A Student can apply for Registration, ONLY AFTER obtaining the 'WRITTEN APPROVAL' from his Faculty Advisor, which should be submitted to the College Academic Section through the Head of Department (a copy of it being retained with Head of Department, Faculty Advisor and the Student).

4.4 Subject/ Course Options through Registration are final and CANNOT be changed, nor can they be inter-changed; further, alternate choices also will not be considered. However, if the Subject/ Course that has already been listed for Registration by the College in a Semester could not be offered due to unforeseen or unexpected reasons, then the Student will be allowed to have alternate choice either for a new Subject, if it is offered, or for another existing Subject (subject to availability of seats). Such alternate arrangements will be made by the Head of Department, with due notification and time-framed schedule, within the FIRST WEEK from the commencement of Class-work for that Semester.

5.0 Attendance Requirements

The programmes are offered based on a unit system with each subject being considered a unit. Attendance is calculated separately for each subject.

5.1 Attendance in all classes (Lectures/Laboratories) is compulsory. The minimum required attendance ineach theory subject (***also mandatory Audit Courses***) including the attendance of mid-term examination /Laboratory etc. is 75%. Two periods of attendance for each theory subject shall be considered, if the student appears for the mid-term examination of that subject. ***The attendance of mandatory Audit Courses should be maintained separately by the College.*** A student shall not be permitted to appear for the Semester End Examinations (SEE), if his attendance is less than 75%.

5.2 A student's Seminar report and presentation on Mini Project shall be eligible for evaluation, only if he ensures a minimum of 75% of his attendance in Seminar presentation classes on Mini Project duringthat Semester.

5.3 **Condoning of shortage of attendance** (between 65% and 75%) up to a maximum of 10% (considering the days of attendance in sports, games, NCC, NSS activities and Medical grounds) in each subject (Theory/Lab/Mini Project with Seminar) of a semester shall be granted by the College Academic Committee on genuine reasons.

5.4 A prescribed fee per subject shall be payable for condoning shortage of attendance after getting the approval of College Academic Committee for the same. The College Academic Committee shall maintain relevant documents along with the request from the student.

5.5 Shortage of Attendance below 65% in any subject shall in **no case be condoned.**

5.6 A Student, whose shortage of attendance is not condoned in any Subject(s) (Theory/Lab/Mini Project with Seminar) in any Semester, is considered as 'Detained in that Subject(s), and is not eligible to write Semester End Examination(s) of such Subject(s), (in case of Mini Project with Seminar, his/her Mini Project with Seminar

Report or Presentation are not eligible for evaluation) in that Semester; and he/she has to seek re-registration for those Subject(s) in subsequent Semesters, and attend the same as and when offered.

5.7 A student fulfills the attendance requirement in the present semester, shall not be eligible for readmission into the same class.

5.8 a) A student shall put in a minimum required attendance in at least **three theory subjects (excluding *mandatory (non-credit audit)* course)** in first Year I semester for promotion to first Year II Semester.

b) A student shall put in a minimum required attendance in at least **three theory subjects (excluding *mandatory (non-credit audit)* course)** in first Year II semester for promotion to second Year I Semester.

6.0 Academic Requirements

The following academic requirements must be satisfied, in addition to the attendance requirements mentioned in item no. 5. The performance of the candidate in each semester shall be evaluated subject- wise, with a maximum of 100 marks per subject / course (theory / practical), based on Internal Evaluation and Semester End Examination.

6.1 A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/course, if he secures not less than:

- 40% of Marks (24 out of 60 marks) in the Semester End Examination;
- 40% of Marks in the internal examinations (16 out of 40 marks allotted for CIE); and
- A minimum of 50% of marks in the sum total of CIE (Continuous Internal Evaluation) and SEE(Semester End Examination) taken together; in terms of Letter Grades this implies securing **'B'** Grade or above in a subject.

6.2 A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to Mini Project with seminar, if student secures not less than 50% marks (i.e. 50 out of 100 allotted marks). The student would be treated as failed, if student (i) does not submit a seminar report on Mini Project or does not make a presentation of the same before the evaluation committee as per schedule or (ii) secures less than 50% marks in Mini Project with seminar evaluation. The failed student shall reappear for the above evaluation when the notification for supplementary examination is issued.

6.3 A student shall register for all subjects for total of **68** credits as specified and listed in the course structure for the chosen specialization, put in the required attendance and fulfill the academic requirements for securing **68** credits obtaining a minimum of **'B'**

Grade or above in each subject, and all **68** credits securing Semester Grade Point Average **(SGPA) ≥ 6.0** (in each semester) and final Cumulative Grade Point Average **(CGPA)** (i.e., CGPA at the end of PGP**) ≥ 6.0**, and shall ***pass all the mandatory Audit Courses*** to complete the PGP successfully.

Note: (1) The SGPA will be computed and printed on the marks memo only if the candidate

passes inall the subjects offered and gets minimum B grade in all the subjects.

(2) CGPA is calculated only when the candidate passes in all the subjects offered in all thesemesters

6.4 Marks and Letter Grades obtained in all those subjects covering the above specified **68** credits alone shall be considered for the calculation of final CGPA, which will be indicated in the Grade Card /Marks Memo of second year second semester.

6.5 If a student registers for extra subject(s) (in the parent department or other departments/ branches of Engineering) other than those listed subjects totaling to **68** credits as specified in the course structure, the performance in extra subject(s) (although evaluated and graded using the same procedure as that of the required **68** credits) will not be considered while calculating the SGPA and CGPA. For suchextra subject(s) registered, percentage of marks and Letter Grade alone will be indicated in the Grade Card/Marks Memo, as a performance measure, subject to completion of the attendance and academic requirements as stated in items 5 and 6.1 - 6.3.

6.6 When a student is detained due to shortage of attendance in any subject(s) in any semester, no Grade allotment will be made for such subject(s). However, he is eligible for re-registration of such subject(s) in the subsequent semester(s), as and when next offered, with the academic regulations of the batch into which he is re-registered, by paying the prescribed fees per subject. In all these re-registration cases, the student shall have to secure a fresh set of internal marks and Semester End Examination marks for performance evaluation in such subject(s), and SGPA/CGPA calculations.

6.7 A student eligible to appear for the Semester End Examination in any subject, but absent from it or failed (failing to secure 'B' Grade or above), may reappear for that subject at the supplementary examination as and when conducted. In such cases, his Internal Marks assessed earlier for that subject will be carried over, and added to the marks secured in the supplementary examination, for the purpose of evaluating his performance in that subject.

6.8 A Student who fails to earn 68 credits as per the specified course structure, and as indicated above, within four academic years from the date of commencement of his first year first semester, shall forfeit his seat in M. Tech. programme and his admission shall stand cancelled.

7.0 Evaluation - Distribution and Weightage of Marks

The performance of a student in each semester shall be evaluated subject- wise (irrespective of credits assigned) for a maximum of 100 marks.

7.1 The performance of a student in every subject/course (including practicals and Project) will be evaluated for 100 marks each, with 40 marks allotted for CIE (Continuous Internal Evaluation) and 60 marks for SEE (Semester End-Examination). The Continuous Internal Evaluation shall be made based on the average of the marks secured in the two Mid-Term Examinations conducted, first Mid-Term examinations in the middle of the Semester and second Mid-Term examinations during the last weekof instruction.

7.2 In CIE, for theory subjects, during a semester, there shall be two mid-term examinations. Each Mid- Term examination consists of two parts i) **Part – A** for 10 marks, ii) **Part – B** for 20 marks with a total duration of 2 hours as follows:

1. Mid-Term Examination for 30 marks:
   a. Part - A: Objective/quiz paper for 10 marks.
   b. Part – B: Descriptive paper for 20 marks.

The objective/quiz paper is set with multiple choice, fill-in the blanks and match the following type of questions for a total of 10 marks. The descriptive paper shall contain 6 full questions out of which, the student has to answer 4 questions, each carrying 5 marks. The average of the two Mid Term Examinations shall be taken as the final marks for Mid Term Examination (for 30 marks).

The remaining 10 marks of Continuous Internal Assessment (out of 40) are distributed as:

2. Assignment for 5 marks. (Average of 2 Assignments each for 5 marks)
3. Subject Viva-Voce/PPT/Poster Presentation/ Case Study on a topic in the concerned subject for 5 marks.

While the first mid-term examination shall be conducted on 50% of the syllabus, the second mid-term examination shall be conducted on the remaining 50% of the syllabus.

Five (5) marks are allocated for assignments (as specified by the subject teacher concerned). The first assignment should be submitted before the conduct of the first mid-term examination, and the second assignment should be submitted before the conduct of the second mid-term examination. The average of the two assignments shall be taken as the final marks for assignment (for 5 marks).

Subject Viva-Voce/PPT/Poster Presentation/ Case Study on a topic in the concerned subject for 5 marks before II Mid-Term Examination.

- The Student, in each subject, shall have to earn 40% of marks (i.e. 16 marks out of 40 marks) in CIE, 40% of marks (i.e. 24 marks out of 60) in SEE and Overall 50% of marks (i.e. 50 marks out of 100 marks) both CIE and SEE marks taking together.

The student is eligible to write Semester End Examination of the concerned subject, if the student scores ≥ 40% (16 marks) of 40 Continuous Internal Examination (CIE) marks.

In case, the student appears for Semester End Examination (SEE) of the concerned subject but not scored minimum 40% of CIE marks (16 marks out of 40 internal marks), his performance in that subject in SEE shall stand cancelled inspite of appearing the SEE.

The details of the end semester question paper pattern are as follows:

7.3 The Semester End Examinations (SEE), for theory subjects, will be conducted for 60 marks consistingof two parts viz. i) **Part- A** for 10 marks, ii) **Part - B** for 50 marks.

- Part-A is a compulsory question which consists of ten sub-questions from all units carrying equalmarks.
- Part-B consists of five questions (numbered from 2 to 6) carrying 10 marks each. Each of these questions is from each unit and may contain sub-questions. For each question there will be an "either" "or" choice, which means that there will be two questions from each unit and the studentshould answer either of the two questions.
- The duration of Semester End Examination is 3 hours.

7.4 For practical subjects there shall be a Continuous Internal Evaluation (CIE) during the semester for 40 marks and 60 marks for semester end examination. Out of the 40 marks for internal evaluation:

1. A write-up on day-to-day experiment in the laboratory (in terms of aim, components/procedure, expected outcome) which shall be evaluated for 10 marks
2. 10 marks for viva-voce (or) tutorial (or) case study (or) application (or) poster presentation of thecourse concerned.
3. Internal practical examination conducted by the laboratory teacher concerned shall be evaluatedfor 10 marks.
4. The remaining 10 marks are for Laboratory Project, which consists of the Design (or) Software / Hardware Model Presentation (or) App Development (or) Prototype Presentation submission which shall be evaluated after completion of laboratory course and before semester end practical examination.

The Semester End Examination shall be conducted with an external examiner and the laboratory teacher. The external examiner shall be appointed from the cluster / other colleges which will be decided by the examination branch of the University.

In the Semester End Examination, held for 3 hours, total 60 marks are divided and allocated as shownbelow:

1. 10 marks for write-up
2. 15 for experiment/program
3. 15 for evaluation of results
4. 10 marks for presentation on another experiment/program in the same laboratory course and

5. 10 marks for viva-voce on concerned laboratory course.

- The Student, in each subject, shall have to earn 40% of marks (i.e. 16 marks out of 40 marks) in CIE, 40% of marks (i.e. 24 marks out of 60) in SEE and Overall 50% of marks (i.e. 50 marks out of 100 marks) both CIE and SEE marks taking together.

The student is eligible to write Semester End Examination of the concerned subject, if the student scores ≥ 40% (16 marks) of 40 Continuous Internal Examination (CIE) marks.

In case, the student appears for Semester End Examination (SEE) of the concerned subject but not scored minimum 40% of CIE marks (16 marks out of 40 internal marks), his performance in that subject in SEE shall stand cancelled inspite of appearing the SEE.

7.5 For conducting laboratory end examinations of all PG Programmes, one internal examiner and one external examiner are to be appointed by the Principal/Controller of Examinations. The external examiner should be selected from outside the College concerned but within the cluster.

7.6 There shall be Mini Project with Seminar during I year II semester for internal evaluation of 100 marks. The Departmental Academic Committee (DAC) will review the progress of the mini project during the seminar presentations and evaluate the same for 50 marks. Mini Project Viva Voce will be evaluated by the DAC for another 50 marks before the semester end examinations. Student shall carryout the mini project in consultation with the mini project supervisor which may include critically reviewing the literature, project implementation and submit it to the department in the form of a report and shall make an oral presentation before the DAC consisting of Head of the Department, Mini Project supervisor and two other senior faculty members of the department. The student has to secure a minimum of 50% of marks in i) seminar presentation and ii) mini project viva voce, to be declared successful. If he fails to obtain the minimum marks, he has to reappear for the same as and when scheduled.

7.7 Every candidate shall be required to submit a dissertation on a topic approved by the Dissertation Review Committee.

7.8 A Dissertation Review Committee (DRC) shall be constituted with the Head of the Department as Chairperson, Dissertation Supervisor and one senior faculty member of the Department offering the M.Tech. programme.

7.9 Registration of Dissertation Work: A candidate is permitted to register for the Dissertation Work after satisfying the attendance requirement in all the subjects, both theory and laboratory.

7.10 After satisfying 7.9, a candidate must present in ***Dissertation Work Review - I***, in consultation with his Dissertation Supervisor, the title, objective and plan of action of his Dissertation work to the Dissertation Review Committee (DRC) for approval ***within***

four weeks from the commencement of **Second year First Semester**. Only after obtaining the approval of the DRC can the student initiate the Dissertation work.

7.11 If a candidate wishes to change his supervisor or topic of the Dissertation, he can do so with the approval of the DRC. However, the DRC shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of Dissertation proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

7.12 A candidate shall submit his Dissertation progress report in two stages at least with a gap of **three** months between them.

7.13 The work on the Dissertation shall be initiated at the beginning of the II year and the duration of the Dissertation is two semesters. A candidate is permitted to submit Dissertation Thesis only after successful completion of all theory and practical courses with the approval of DRC ***not earlier than 40 weeks*** from the date of approval of the Dissertation work. For the approval of DRC, the candidate shall submit the draft copy of thesis to the Head of the Department and make an oral presentation before the DRC.

7.14 ***The Dissertation Work Review - II*** in II Year I Semester carries 100 internal marks. Evaluation should be done by the DRC for 50 marks and the Supervisor will evaluate the work for the other 50 marks. The Supervisor and DRC will examine the Problem Definition, Objectives, Scope of Work, Literature Survey in the same domain and progress of the Dissertation Work. A candidate has to secure a minimum of 50% of marks to be declared successful in Dissertation Work Review - II. If he fails to obtain the minimum required marks, he has to reappear for Dissertation Work Review - II as and when conducted.

7.15 ***The Dissertation Work Review - III*** in II Year II Sem. carries 100 internal marks. Evaluation should be done by the DRC for 50 marks and the Supervisor will evaluate it for the other 50 marks. The DRC will examine the overall progress of the Dissertation Work and decide whether or not the Dissertation is eligible for final submission. A candidate has to secure a minimum of 50% of marks to be declared successful in Dissertation Work Review - III. If he fails to obtain the required minimum marks, he has to reappear for Dissertation Work Review - III as and when conducted. For Dissertation Evaluation (Viva Voce) in II Year II Semester there are external marks of 100 and it is evaluated by the external examiner. The candidate has to secure a minimum of 50% marks in Dissertation Evaluation (Viva- Voce) examination.

7.16 Dissertation Work Reviews - II and III shall be conducted in phase I (Regular) and Phase II (Supplementary). Phase II will be conducted only for unsuccessful students in Phase I. The unsuccessful students in Dissertation Work Review - II (Phase II) shall reappear for it at the time of Dissertation Work Review - III (Phase I). These students shall reappear for Dissertation Work Review- III in the next academic year at the time of Dissertation Work Review - II only after completion of Dissertation Work Review - II, and then Dissertation Work Review - III follows. The unsuccessful students in

Dissertation Work Review - III (Phase II) shall reappear for Dissertation Work Review - III in the next academic year only at the time of Dissertation Work Review - II (Phase I).

7.17 After approval from the DRC, a soft copy of the thesis should be submitted for ANTI-PLAGIARISM check and the plagiarism report should be submitted to the Examination branch and be included in the final thesis. The Thesis will be accepted for submission, if the similarity index is less than **30%**. If the similarity index has more than the required percentage, the student is advised to modify accordingly and re- submit the soft copy of the thesis after one month. The maximum number of re-submissions of thesis after plagiarism check is limited to ***TWO***. The candidate has to register for the Dissertation work and work for two semesters. After three attempts, the admission is liable to be cancelled. The college authorities are advised to make plagiarism check of every soft copy of theses before submissions.

7.18 Three copies of the Dissertation Thesis certified by the supervisor shall be submitted to the College, after submission of a research paper related to the Dissertation work in a UGC approved journal. A copy of the submitted research paper shall be attached to thesis.

7.19 The thesis shall be adjudicated by an external examiner selected by the Principal/Controller of Examinations. For this, the Head of the department shall submit a panel of **three** examiners from among the list of experts in the relevant specialization as submitted by the supervisor concerned.

7.20 If the report of the external examiner is unsatisfactory, the candidate shall revise and resubmit the Thesis. If the report of the examiner is unsatisfactory again, the thesis shall be summarily rejected. Subsequent actions for such dissertations may be considered, only on the specific recommendations of the external examiner and /or Dissertation Review Committee. No further correspondence in this matter will be entertained, if there is no specific recommendation for resubmission.

7.21 If the report of the examiner is satisfactory, the Head of the Department shall coordinate and decide for the conduct of Dissertation Viva-Voce examination. The Dissertation Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner who adjudicated the Thesis. The candidate has to secure a minimum of 50% of marks in Dissertation Evaluation (Viva-Voce) examination.

7.22 If he fails to fulfill the requirements as specified in 7.21, he will reappear for the Dissertation Viva-Voce examination ***only after three months***. In the reappeared examination also, if he fails to fulfill the requirements, he will not be eligible for the award of the degree, unless he is asked to revise and resubmit his Dissertation Work by the board within a specified time period (within ***four*** years from the date of commencement of his first year first semester).

7.23 The Dissertation Viva-Voce External examination marks must be submitted to the

Examination branch on the day of the examination.

7.24 For mandatory non-credit Audit courses, a student has to secure 40 marks out of 100 marks (i.e. 40% of the marks allotted) in the continuous internal evaluation for passing the subject/course.These marks should also be uploaded along with the internal marks of other subjects.

7.25 No marks or letter grades shall be allotted for mandatory non-credit Audit Courses. Only Pass/Fail shall be indicated in Grade Card.

8.0 Re-Admission/Re-Registration

8.1 Re-Admission for Discontinued Student

A student, who has discontinued the M. Tech. degree programme due to any reason whatsoever, may be considered for 'readmission' into the same degree programme (with the same specialization) with the academic regulations of the batch into which he gets readmitted, with prior permission from the authorities concerned, subject to item 6.6.

8.2 If a student is detained in a subject (s) due to shortage of attendance in any semester, he may be permitted to **re-register** for the same subject(s) in the same category (core or elective group) or equivalent subject, if the same subject is not available, as suggested by the Board of Studies of that department, as and when offered in the subsequent semester(s), with the academic regulations of thebatch into which he seeks re-registration, with prior permission from the authorities concerned, subject to item 3.2

8.3 A candidate shall be given only one-time chance to re-register and attend the classes for a maximum of two subjects in a semester, if the internal marks secured by a candidate are less than 40% and failed in those subjects but fulfilled the attendance requirement. A candidate must re-register for failed subjects within four weeks of commencement of the class work, in the next academic year and secure the required minimum attendance. In the event of the student taking this chance, his Continuous Internal Evaluation (internal) marks and Semester End Examination marks obtained in the previous attempt stand cancelled.

9.0 Examinations and Assessment - The Grading System

9.1 Grades will be awarded to indicate the performance of each student in each Theory Subject, or Lab/Practicals, or Mini Project with Seminar, Dissertation, etc., based on the percentage of marks obtained in CIE + SEE (Continuous Internal Evaluation + Semester End Examination, both taken together) as specified in Item 7 above, and a corresponding Letter Grade shall be given.

9.2 As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades (UGC Guidelines) and corresponding percentage of marks shall be followed:

% of Marks Secured in a subject/Course (Class Intervals)	Letter Grade (UGC Guidelines)	Grade Points
90% and above (≥ 90%, ≤ 100%)	O (Outstanding)	10
Below 90% but not less than 80% (≥80%, <90%)	A^+ (Excellent)	9
Below 80% but not less than 70% (≥ 70%, <80%)	A (Very Good)	8
Below 70% but not less than 60% (≥ 60%, <70%)	B^+ (Good)	7
Below 60% but not less than 50% (≥ 50%, <60%)	B (above Average)	6
Below 50% (< 50%)	F (FAIL)	0
Absent	**Ab**	**0**

9.3 A student obtaining **'F'** Grade in any Subject is deemed to have 'failed' and is required to reappear as 'Supplementary Candidate' for the Semester End Examination (SEE), as and when conducted. In such cases, his Internal Marks (CIE Marks) in those subjects will remain as obtained earlier.

9.4 If a student has not appeared for the examinations, '**Ab**' Grade will be allocated to him for any subject and shall be considered 'failed' and will be required to reappear as 'Supplementary Candidate' for the Semester End Examination (SEE), as and when conducted.

9.5 A Letter Grade does not imply any specific marks percentage; it is only the range of percentage of marks.

9.6 In general, a student shall not be permitted to repeat any Subject/ Course (s) only for the sake of 'Grade Improvement' or 'SGPA/ CGPA Improvement'.

9.7 A student earns Grade Point (GP) in each Subject/ Course, on the basis of the Letter Grade obtainedby him in that Subject/ Course. The corresponding 'Credit Points' (CP) are computed by multiplying the Grade Point with Credits for that particular Subject/ Course.

Credit Points (CP) = Grade Point (GP) x Credits …. For a Course

9.8 The student passes the Subject/ Course only when he **gets GP ≥ 6 (B Grade or above).**

9.9 The Semester Grade Point Average (SGPA) is calculated by dividing the Sum of Credit Points (CP) secured from ALL Subjects/ Courses registered in a Semester, by the Total Number of Credits registeredduring that Semester. SGPA is rounded off to TWO Decimal Places. SGPA is thus computed as

SGPA = { $\sum_{i=1}^{N} C_i G_i$ } / { $\sum_{i=1}^{N} C_i$ } …. For each Semester,

where 'i' is the Subject indicator index (taking into account all Subjects in a Semester), 'N' is the no. of Subjects 'REGISTERED' for the Semester (as specifically required and listed under the

Course Structure of the parent Department), C_i is the no. of Credits allotted to the ith Subject, and G_i represents the Grade Points (GP) corresponding to the Letter Grade awarded for that ith Subject.

9.10 The Cumulative Grade Point Average (CGPA) is a measure of the overall cumulative performance of a student over all Semesters considered for registration. The CGPA is the ratio of the Total Credit Points secured by a student in ALL registered Courses in ALL Semesters, and the Total Number of Credits registered in ALL the Semesters. CGPA is rounded off to TWO Decimal Places. CGPA is thus computed from the I Year Second Semester onwards, at the end of each Semester, as per the formula

CGPA = { $\sum_{j=1}^{M} C_j G_j$ } / { $\sum_{j=1}^{M} C_j$ } … for all S Semesters registered

(ie., up to and inclusive of S Semesters, S ≥ 2),

where 'M' is the TOTAL no. of Subjects (as specifically required and listed under the Course Structure of the parent Department) the Student has 'REGISTERED' for from the 1st Semester onwards upto and inclusive of the Semester S (obviously M > N), 'j' is the Subject indicator index (taking into account all Subjects from 1 to S Semesters), C_j is the no. of Credits allotted to the jth Subject, and G_j represents the Grade Points (GP) corresponding to the Letter Grade awarded for that jth Subject. After registration and completion of I Year I Semester however, the SGPA of that Semester itself may be taken as the CGPA, as there are no cumulative effects.

Illustration of calculation of SGPA

Course/Subject	Credits	Letter Grade	Grade points	Credit Points
Course 1	4	A	8	4*8 = 32
Course 2	4	O	10	4*10 = 40
Course 3	4	B	6	4*6 = 24
Course 4	3	B	6	3*6 = 18
Course 5	3	A+	9	3*9 = 27
Course 6	3	B	6	3*6 = 18
	21			159

SGPA = 159/21 = 7.57

Illustration of calculation of CGPA

Semester	Credits	SGPA	Credits * SGPA
Semester I	24	7	24*7 = 168
Semester II	24	6	24*6 = 144
Semester III	24	6.5	24*6.5 = 156
Semester IV	24	6	24*6 = 144
	96		612

CGPA = 612/96 = 6.37

10.0 Award of Degree and Class

10.1 If a student who registers for all the specified Subjects/ Courses as listed in the Course Structure, satisfies all the Course Requirements, and passes the examinations prescribed in the entire PG Programme (PGP), and secures the required number of **68** Credits (with CGPA ≥ 6.0), shall be declaredto have 'QUALIFIED' for the award of the M.Tech. Degree in the chosen Branch of Engineering and Technology with the specialization that he was admitted into.

10.2 Award of Class

After a student has earned the requirements prescribed for the completion of the programme and is eligible for the award of M.Tech. Degree, he shall be placed in one of the following three classes based on the CGPA:

Class Awarded	CGPA
First Class with Distinction	≥ 7.75
First Class	6.75≤ CGPA < 7.75
Second Class	6.00≤ CGPA < 6.75

A student with final CGPA (at the end of the **PGP) < 6.00** shall not be eligible for the Award of Degree.

11.0 Withholding of Results

If the student has not paid the dues, if any, to the University or if any case of indiscipline is pending against him, the result and degree of the student will be withheld and he will not be allowed into the next semester.

12.0 General

12.1 Credit: A unit by which the course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of teaching (lecture or tutorial) or two hours ofpractical work/field work per week.

12.2 Credit Point: It is the product of grade point and number of credits for a course.

12.3 Wherever the words "he", "him", "his", occur in the regulations, they shall include "she", "her".

12.4 The academic regulation should be read as a whole for the purpose of any interpretation.

12.5 In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the University is final.

12.6 The CMRCET may change or amend the academic regulations or syllabi at any time and the changesor amendments made shall be applicable to all the students with effect from the dates notified by theUniversity.

MALPRACTICE RULES

Disciplinary Action for Malpractices/Improper Conduct in Examinations

	Nature of Malpractices/ Improper conduct	Punishment
1.(a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers, smart watches, electronic gadgets or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only. Confiscation of Cell phones, pager, palm computers, smart watches, electronic gadgets etc. and the same would be handed over only after punishment finalized by Malpractice Committee.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones, pager, palm computers, smart watches, electronic gadgets with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him. Confiscation of Cell phones, pager, palm computers, smart watches, electronic gadgets etc. and the same would be handed over only after punishment finalized by Malpractice Committee.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers, cell phones, smart watches, electronic gadgets or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations excluding Project work/ Mandatory Courses /Technical Seminar and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled. Confiscation of Cell phones, pager, palm computers, smart watches, electronic gadgets etc. and the same would be handed over only after punishment finalized by Malpractice Committee.
3.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate Who has been

		impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the Remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all end semester examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4.	Smuggles the answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all end semester Examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks	Cancellation of the performance in that subject
6.	Refuses to obey the orders of the Chief Superintendent/Assistant– Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the or organizes a walk out or instigates others **to** examination hall-walk out, or threatens the officer- in-charge or any person on duty in or outside the examination hall of any injury**,** to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer- in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates are also debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.

	campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all Semester End Examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of That semester/year. The candidate is also debarred and forfeits the seat.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	If the student belongs to the college, expulsion from the examination performance in that subject and all other subjects shall and cancellation of the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Comes in a state of inebriated/drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for other remaining examinations of the subjects of that semester/year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during	Cancellation of the performance in that subject and all other subjects the

	special scrutiny.	candidate has appeared including practical examinations excluding Project work/ Mandatory Courses /Technical Seminar of that semester/year.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the College Academic Committee for further action to award suitable punishment.	

Malpractices identified by squad or special invigilators

Punishments to the candidates as per the above guidelines.

Malpractice identified at Spot center during valuation

1) The following procedure is to be followed in the case of malpractice cases detected during valuation, scrutiny etc. at spot center. Malpractice is detected at the spot valuation. The case is to be referred to the malpractice committee. Malpractice committee will meet and discuss/question the candidate and based on the evidences, the committee will recommend suitable action on the candidate.
2) A notice is to be served to the candidate(s) involved through the Principal regarding the malpractice and seek explanations.
3) The involvement of staff who are in charge of conducting examinations, invigilators valuing examination papers and preparing / keeping records of documents relating to the examinations in such acts (inclusive of providing in correct or misleading information) that infringe upon the course of natural justice to one and all concerned at the examinations shall be viewed seriously and recommended for award of appropriate punishment after thorough enquiry.
4) Based on the explanation and recommendation of the committee action may be initiated.

Malpractice committee:

(a) Chief Superintendent	Chairman
(b) Controller of Examinations	Member
(c) Dean Academics	Member
(d) Chief Examiner of the Course/ Subject Expert	Member
(e) Concerned Head of the Department	Member
(f) Observer	Member

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DEPARTMENT OF
ELECTRONICS & COMMUNICATION ENGINEERING

COURSE STRUCTURE FOR M. TECH (EMBEDDED SYSTEMS)
EFFECTIVE FROM ACEDEMIC YEAR 2022-23

I – SEMESTER

S.NO	Code	Group	Course Title	L	T	P	Credits
1	B455301	Core- I	Digital System Design with FPGAs	3	0	0	3
2	B455302	Core- II	System Design with Embedded Linux	3	0	0	3
3	B455401 B455402 B455403	PE- I	1. CMOS VLSI Design 2. Pattern Recognition and Machine Learning 3. Wireless Sensor Networks	3	0	0	3
4	B455404 B455405 B455406	PE- II	1. Communications Buses & Interfaces 2. Advanced Computer Architecture 3. CMOS Analog IC Design	3	0	0	3
5	B455501	Lab – I	Digital system Design with FPGAs Lab	0	0	4	2
6	B455502	Lab – II	System Design with Embedded Linux Lab	0	0	4	2
7	B420303		Research Methodology & IPR	2	0	0	2
8		Audit – I	Audit Course – I	2	0	0	0
			Total	**16**	**0**	8	**18**

II – SEMESTER

S.NO	Code	Group	Course Title	L	T	P	Credits
1	B455303	Core- III	ARM Microcontrollers	3	0	0	3
2	B455304	Core- IV	Digital Control Systems	3	0	0	3
3	B455407 B455408 B455409	PE- III	1. IoT Architectures and System Design 2. Design for Testability 3. SoC Design	3	0	0	3
4	B455410 B455411 B455412	PE- IV	1. Hardware and Software Co-Design 2. Secure Networks 3. Physical Design Automation	3	0	0	3
5	B455503	Lab – III	ARM Microcontrollers Lab	0	0	4	2
6	B455504	Lab - IV	Digital Control Systems Lab	0	0	4	2
7	B455801		Mini Project with Seminar	0	0	4	2
8		Audit - II	Audit Course – II	2	0	0	0
			Total	**14**	**0**	**12**	**18**

III – SEMESTER

S.NO	Code	Group	Course Title	L	T	P	Credits
1	B455413 B455414 B455415	PE- V	1. Embedded Networks 2. CMOS Mixed Signal Design 3. Human -Machine Interface	3	0	0	3
2		Open Elective	Open Elective	3	0	0	3
3	B455802	Dissertation	Dissertation Work Review – II	0	0	12	6
			Total	**6**	**0**	**12**	**12**

IV - SEMESTER

S.NO	Code	Group	Course Title	L	T	P	Credits
1	B455803	Dissertation	Dissertation Work Review - III	0	0	12	06
2	B455804	Dissertation	Dissertation Viva-Voce	0	0	28	14
			Total	**0**	**0**	**40**	**20**

Audit Course I & II:

S.NO	Code		Course Title	L	T	P	Credits
1	B400701	Audit Course	English for Research Paper Writing	2	0	0	0
2	B400702		Disaster Management				
3	B400703		Sanskrit for Technical Knowledge				
4	B400704		Value Education				
5	B400705		Constitution of India				
6	B400706		Pedagogy Studies				
7	B400707		Stress Management by Yoga				
8	B400708		Personality Development Through Life Enlightenment Skills				

Open Electives:

S.NO	Code	Course Title
1	B455601	Embedded Systems
2	B420601	Disaster Management
3	B443601	Photovoltaic Systems
4	B458601	Optimization Techniques
5	B4A3604	Digital Forensics

(B455301) DIGITAL SYSTEM DESIGN WITH FPGAs

M.Tech (ES)-I Semester	L	T	P	C
	3	0	0	3

UNIT - I

Programmable Logic Devices: The concept of programmable Logic Devices, SPLDs, PAL devices, PLA devices, GAL devices, CPLD-Architecture, FPGAs-FPGA technology, architecture, virtex CLB andslice, FPGA Programming Technologies, Xilinx XC2000, XC3000, XC4000 Architectures, Actel ACT1, ACT2 and ACT3 Architectures. [TEXTBOOK-1]

UNIT - II

Analysis and derivation of clocked sequential circuits with state graphs and tables: A sequential parity checker, Analysis by signal tracing and timing charts-state tables and graphs-general models for sequential circuits, Design of a sequence detector, More Complex design problems, Guidelines for construction of state graphs, serial data conversion, Alphanumeric state graph notation. Need and Design strategies for multi-clock sequential circuits. [TEXTBOOK-2]

UNIT - III

Sequential circuit Design: Design procedure for sequential circuits-design example, Code converter,Design of Iterative circuits, Design of a comparator, Controller (FSM) – Metastability, Synchronization, FSM Issues, Pipelining resources sharing, Sequential circuit design using FPGAs, Simulation and testing of Sequential circuits, Overview of computer Aided Design. [TEXTBOOK-2]

UNIT - IV

Fault Modeling and Test Pattern Generation: Logic Fault Model, Fault detection & redundancy, Fault equivalence and fault location, Fault dominance, Single stuck at fault model, multiple Stuck at Fault models, Bridging Fault model.

Fault diagnosis of combinational circuits by conventional methods, path sensitization techniques, Boolean difference method, KOHAVI algorithm, Test algorithms-D algorithm, Random testing, transition count testing, signature analysis and test bridging faults. [TEXTBOOK-3 & Ref.1]

UNIT - V

Fault Diagnosis in sequential circuits: Circuit Test Approach, Transition check Approach, State identification and fault detection experiment, Machine identification, Design of fault detection experiment. [Ref.3]

TEXT BOOKS

1. Digital Electronics and design with VHDL- Volnei A. Pedroni, Elsevier publications.
2. Fundamentals of Logic Design-Charles H.Roth, Jr. -5th Ed., Cengage Learning.
3. Digital Circuits and Logic Design-Samuel C. LEE, PHI, 2008.

REFERENCE BOOKS

1. Logic Design Theory-N.N. Biswas, PHI.
2. Digital System Design using programmable logic devices- Parag K. Lala, BS publications.
3. Switching and Finite Automata Theory - Zvi Kohavi & Niraj K. Jha, 3rd Edition, Cambridge, 2010.

Course Outcomes:

After the Completion of the course, the students will be able to

1. Exposes the design approaches using FPGAs
2. Analyse the sequential circuits using state graphs and state tables
3. Design the sequential circuits using state graphs and state tables
4. Develop Fault modelling and test patterns for fault diagnosis in Combinational circuits
5. Design fault detection experiments in Sequential circuits

(B455302) SYSTEM DESIGN WITH EMBEDDED LINUX

M.Tech (ES)-I Semester	L	T	P	C
	3	0	0	3

UNIT- I

Introduction to Real Time Operating Systems: Characteristics of RTOS, Tasks Specifications and types, Real-Time Scheduling Algorithms, Concurrency, Inter-process Communication and Synchronization mechanisms, Priority Inversion, Inheritance and Ceiling. Embedded Linux Vs Desktop Linux, Embedded Linux Distributions, System calls, Static and dynamic libraries, Cross toolchains

UNIT- II

Embedded Linux Architecture, Kernel Architecture – HAL, Memory manager, Scheduler, File System,I/O and Networking subsystem, IPC, User space, Start-up sequence

UNIT- III

Board Support Package Embedded Storage: MTD, Architecture, Drivers, Embedded File System Embedded Device Drivers: Communication between user space and kernel space drivers, Character and Block Device Drivers, Interrupt handling, Kernel modules

Embedded Drivers: Serial, Ethernet, I2 C, USB, Timer, Kernel Modules

UNIT- IV

Porting Applications Real-Time Linux: Linux and Real time, Programming, Hard Real-time Linux

UNIT- V

Building and Debugging: Bootloaders, Kernel, Root file system, Device Tree

TEXT BOOKS:

1. Chris Simmonds, “Mastering Embedded Linux Programming” - Second Edition, PACKTPublications Limited.
2. Karim Yaghmour, “Building Embedded Linux Systems”, O'Reilly & Associates
3. P Raghvan, Amol Lad, Sriram Neelakandan, “Embedded Linux System Design andDevelopment”, Auerbach Publications

REFERENCE BOOKS:

1. Christopher Hallinan, “Embedded Linux Primer: A Practical Real-World Approach”, PrenticeHall, 2nd Edition, 2010.
2. Derek Molloy, “Exploring Beagle Bone: Tools and Techniques for Building with Embedded Linux”, Wiley, 1st Edition, 2014

Course Outcomes:

After the Completion of the course, the students will be able to

1. Apply Real Time Scheduling Algorithms for solving the real time problems
2. Explain the Embedded Linux Architecture and Kernel Architecture
3. Define Board Support Package Embedded Storage and Embedded Device Drivers
4. Write, debug, and design applications in Embedded Real Time Linux.
5. Build and Debug different real time applications by using various kernal debugers

(B455401) CMOS VLSI DESIGN
(PROFESSIONAL ELECTIVE – I)

M.Tech (ES)-I Semester	L	T	P	C
	3	0	0	3

UNIT - I

MOS Design

Pseudo NMOS logic- Inverter, Inverter threshold voltage, output high voltage, Output low voltage, gain at gate threshold voltage, transient response, rise time, fall time, pseudo NMOS logic gates, transistor equivalency, CMOS inverter logic.

UNIT - II

Combinational MOS logic circuits

MOS logic circuits with NMOS loads, Primitive CMOS logic gates- NOR and NAND gates, Complex logic circuits design- realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIAgates, CMOS full-adder, CMOS transmission gates, designing with transmission gates.

UNIT - III

Sequential MOS logic circuits: Behavior of bistable elements, SR Latch, Clocked Latch and Flip-flop circuits, CMOS D Latch and edge triggered flip-flop.

UNIT - IV

Dynamic Logic Circuits: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, high performance dynamic CMOS circuits.

UNIT - V

Semiconductor Memories: Types, RAM array Organization, DRAM- types, operation, leakage currents in DRAM cell and refresh operation, SRAM - operation, leakage currents in SRAM cells, Flash memory-NOR flash and NAND flash.

TEXT BOOKS:

1. Digital Integrated Circuit Design- Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuit Analysis and Design – Sung Mo Kang, YusufLeblebici,TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective- Ming Bo Lin,CRCPress, 2011.
2. Digital Integrated Circuits: A Designs Perspective -Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

Course Outcomes:

After the Completion of the course, the students will be able to

1. Apply Pseudo NMOS logic to design various circuits.
2. Design of combinational MOS logic and sequential MOS logic circuits
3. Carryout the design of different circuits based on dynamic logic
4. Use CMOS transmission gates in various applications
5. Design of different Memories using MOS transistors

(B455402) PATTERN RECOGNITION AND MACHINE LEARNING
(PROFESSIONAL ELECTIVE – I)

M.Tech (ES)-I Semester	L	T	P	C
	3	0	0	3

UNIT-I

Introduction to Pattern recognition: Mathematical Formulation and Basic Functional Equation, Reduction of Dimensionality, Experiments in Pattern Classification, Backward Procedure for Both Feature Ordering- and Pattern Classification, Suboptimal Sequential Pattern Recognition, Nonparametric Design of Sequential Pattern Classifiers, Analysis of Optimal Performance and a Multiclass Generalization

UNIT-II

Linear Models: Linear Basis Function Models -Maximum likelihood and least squares, Geometry of least squares , Sequential learning, Regularized least squares, Multiple outputs , The Bias-Variance Decomposition, Bayesian Linear Regression -Parameter distribution, Predictive, Equivalent, Bayesian Model Comparison, Probabilistic Generative Models-Continuous inputs, Maximum likelihood solution, Discrete features, Exponential family, Probabilistic Discriminative Models -Fixed basis functions, Logistic regression, Iterative reweighted least squares, Multiclass logistic regression, Probit regression,Canonical link functions

UNIT-III

Kernel Methods: Constructing Kernels, Radial Basis Function Networks - Nadaraya-Watson model, Gaussian Processes -Linear regression revisited, Gaussian processes for regression, Learning the hyper parameters, Automatic relevance determination, Gaussian processes for classification, Laplace approximation, Connection to neural networks, Sparse Kernel Machines- Maximum Margin Classifiers, Overlapping class distributions, Relation to logistic regression, Multiclass SVMs, SVMs for regression, Computational learning theory, Relevance Vector Machines- RVM for regression, Analysis of sparsity,RVM for classification

UNIT-IV

Graphical Models: Bayesian Networks, Example: Polynomial regression, Generative models, Discretevariables, Linear-Gaussian models, Conditional Independence- Three example graphs, D-separation, Markov Random Fields -Conditional independence properties, Factorization properties, Illustration: Image de-noising, Relation to directed graphs, Inference in Graphical Models- Inference on a chain, Trees, Factor graphs, The sum-product algorithm, The max-sum algorithm, Exact inference in general graphs, Loopy belief propagation, Learning the graph structure.

UNIT-V

Mixture Models and EM algorithm: K-means Clustering-Image segmentation and compression, Mixtures of Gaussians-Maximum likelihood, EM for Gaussian mixtures, An Alternative View of EM- Gaussian mixtures revisited, Relation to K-means, Mixtures of Bernoulli distributions, EM for Bayesianlinear regression, The EM Algorithm in General, Combining Models- Tree-based Models, Conditional Mixture Models- Mixtures of linear regression models, Mixtures of logistic models, Mixtures of experts.

TEXT BOOKS:

1. Sequential methods in Pattern Recognition and Machine Learning-K.S.Fu, Academic Press,volume no.52.
2. Pattern Recognition and Machine Learning- C. Bishop-Springer,2006.

REFERENCE BOOKS:

1. Pattern Classification- Richard o. Duda, Peter E. hart, David G. Stork, John Wiley& Sons, 2nd Ed., 2001.
2. The elements of Statistical Learning- Trevor Hastie, Robert Tibshirani, Jerome H. Friedman,Springer, 2nd Ed., 2009.

Course Outcomes:

After the Completion of the course, the students will be able to

1. Familiar the basics of pattern classes and functionality.
2. Construct the various linear models.
3. Use the different kernel methods
4. Design of graphical models.
5. Design the Markov and Mixed models.

(B455403) WIRELESS SENSOR NETWORKS
(PROFESSIONAL ELECTIVE – I)

M.Tech (ES)-I Semester	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

UNIT -I:
Introduction to Sensor Networks, unique constraints and challenges, Advantage of Sensor Networks, Applications of Sensor Networks, Types of wireless sensor networks

UNIT –II
Mobile Ad-hoc Networks (MANETs) and Wireless Sensor Networks, Enabling technologies for Wireless Sensor Networks. Issues and challenges in wireless sensor networks

UNIT –III
Routing protocols, MAC protocols: Classification of MAC Protocols, S-MAC Protocol, B-MAC protocol,IEEE 802.15.4 standard and ZigBee

UNIT -IV
Dissemination protocol for large sensor network. Data dissemination, data gathering, and data fusion; Quality of a sensor network; Real-time traffic support and security protocols.

UNIT -V
Design Principles for WSNs, Gateway Concepts Need for gateway, WSN to Internet Communication, and Internet to WSN Communication. Single-node architecture, Hardware components & design constraints, Operating systems and execution environments, introduction to TinyOS and nesC.

TEXT BOOKS:
1. Ad-Hoc Wireless Sensor Networks- C. Siva Ram Murthy,B. S. Manoj, Pearson
2. Principles of Wireless Networks – Kaveh Pah Laven and P. Krishna Murthy, 2002, PE

REFERENCE BOOKS:
1. Wireless Digital Communications – Kamilo Feher, 1999, PHI.
2. Wireless Communications-Andrea Goldsmith, 2005 Cambridge University Press.
3. Mobile Cellular Communication – Gottapu Sasibhushana Rao, Pearson Education, 2012.
4. Wireless Communication and Networking – William Stallings, 2003, PHI.

Course Outcomes:

After the Completion of the course, the students will be able to

1. Analyze and compare various architectures of Wireless Sensor Networks
2. Interpret Design issues and challenges in wireless sensor networks
3. Classify various routing protocols and MAC Protocols
4. Analyze and compare various data gathering and data dissemination methods.
5. "Identify design principals, node architectures, hardware and software required for
6. implementation of wireless sensor networks."

(B455404) COMMUNICATION BUSES AND INTERFACES
(PROFESSIONAL ELECTIVE- II)

M.Tech (ES)-I Semester

L	T	P	C
3	0	0	3

UNIT - I

Serial Busses - Physical interface, Data and Control signals, features, limitations and applications ofRS232, RS485, I2C, SPI

UNIT - II

CAN - Architecture, Data transmission, Layers, Frame formats, applications

UNIT - III

PCIe - Revisions, Configuration space, Hardware protocols, applications

UNIT - IV

USB - Transfer types, enumeration, Descriptor types and contents, Device driver

UNIT - V

Data Streaming Serial Communication Protocol - Serial Front Panel Data Port (SFPDP) using fiber opticand copper cable

TEXT BOOKS:

1. Jan Axelson, "Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems", Lakeview Research, 2nd Edition
2. Jan Axelson, "USB Complete", Penram Publications
3. Mike Jackson, Ravi Budruk, "PCI Express Technology", Mindshare Press
4. Wilfried Voss, "A Comprehensible Guide to Controller Area Network", Copperhill MediaCorporation, 2nd Edition, 2005.
5. Serial Front Panel Draft Standard VITA 17.1 –200x
6. Technical references onwww.can-cia.org, http://www.pcisig.com/www.pcisig.com, http://www.usb.org/www.usb.org

Course Outcomes:

After the Completion of the course, the students will be able to

1. To Identify the suitable serial Bus for data or Control Signals and limitations of various serial interface protocols
2. To Explain the Architecture of the CAN Protocol
3. To Discuss about the various Hardware protocols of PCI
4. To Design of develop peripherals that can be interfered by using USB serial bus
5. Demonstrate the data streaming through Serial Front Panel Data Port (SFPDP) using fiber optic and copper cables

(B455405) ADVANCED COMPUTER ARCHITECTURE
(PROFESSIONAL ELECTIVE- II)

M.Tech (ES)-I Semester	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

UNIT - I

Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law. Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, operations in the instruction set.

UNIT - II

Pipelines: Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT - III

Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.

ILP Software Approach: Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT - IV

Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT - V

Inter Connection and Networks: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture: Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls

TEXT BOOK:

1. John L. Hennessy, David A. Patterson, "Computer Architecture: A Quantitative Approach", 3rdEdition, Elsevier.

REFERENCE BOOKS:

1. John P. Shen and Miikko H. Lipasti, "Modern Processor Design: Fundamentals of Super Scalar Processors", 2002, Beta Edition, McGraw-Hill
2. Kai Hwang, Faye A.Brigs., "Computer Architecture and Parallel Processing", Mc Graw Hill.
3. DezsoSima, Terence Fountain, Peter Kacsuk, "Advanced Computer Architecture - A DesignSpace Approach", Pearson Education.

Course Outcomes:

After the Completion of the course, the students will be able to

1. Illustrate advanced computer architecture aspects.
2. Describe and explain instruction level parallelism with static scheduling and handling of cache memory.
3. Design basic hardware and Software at compiler level.
4. Explain and handle the multi processors and multi thread level parallelism through the distributed shared memory architecture.
5. Describe the networking in modern CPUs and design clusters.

(B455406) CMOS ANALOG IC DESIGN
(PROFESSIONAL ELECTIVE- II)

M.Tech (ES)-I Semester	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

UNIT - I

MOS Devices and Modeling

The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small- Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT- II

Analog CMOS Sub-Circuits

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors- Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT – III

CMOS Amplifiers

Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT - IV

CMOS Operational Amplifiers

Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps,Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques ofOP Amp.

UNIT - V

Comparators

Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford UniversityPress, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

Course Outcomes:

After the Completion of the course, the students will be able to

1. Design basic building blocks of CMOS analog ICs.
2. Carry out the design of single and two stage operational amplifiers and voltage references.
3. Design various Analog CMOS Sub-Circuits like current mirrors.
4. Design various amplifiers like differential, cascode and current amplifiers.
5. Characterize open loop and two stage comparators

(B455501) DIGITAL SYSTEM DESIGN WITH FPGAs LAB

M.Tech (ES)-I Semester	**L**	**T**	**P**	**C**
	0	**0**	**4**	**2**

Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart fromverification by simulation with any of the front end tools.

1. HDL code to realize all the logic gates
2. Design and Simulation of Full Adder, Serial Binary Adder, Multi Precession Adder, CarryLook Ahead Adder.
3. Design of Combinational circuit using Decoders.
4. Design of Combinational circuit using encoder (without and with parity).
5. Design of Combinational circuit using multiplexer.
6. Design of 4 bit binary to gray converter using MUX or Decoders.
7. Design of Multiplexer/ Demultiplexer, comparator in all 3 styles.
8. Modelling of an Edge triggered and Level triggered FFs : D, SR, JK
9. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequencecounter
10. Design of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel inSerial out and Parallel in Parallel Out using different FFs.
11. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
12. Design of 4- Bit Multiplier, Divider.
13. Design of ALU to Perform – ADD, SUB, AND-OR, 1's and 2's Compliment,
14. Implementing the above designs on FPGA kits.

Course Outcomes:

After the Completion of the course, the students will be able to

1. Design ,simulate and various types of adders and implementing using FPGA/CPLD Boards
2. Design ,simulate the decoders, encoders, and implementing using FPGA/CPLD Boards
3. Design ,simulate the multiplexer, demultiplexer ,converters and implementing using FPGA/CPLD Boards
4. Design ,simulate the counters and shift registers and implementing using FPGA/CPLD Boards
5. Design ,simulate the multiplier, divider, ALU and implement using FPGA/CPLD Boards

(B455502) SYSTEM DESIGN WITH EMBEDDED LINUX LAB

M.Tech (ES)-I Semester	L	T	P	C
	0	0	4	2

List of Experiments:

1. **Functional Testing Of Devices:** Flashing the OS on to the device into a stable functional stateby porting desktop environment with necessary packages.
2. **Exporting Display On To Other Systems:** Making use of available laptop/desktop displays as a display for the device using SSH client & X11 display server.
3. **GPIO Programming:** Programming of available GPIO pins of the corresponding device using native programming language. Interfacing of I/O devices like LED/Switch etc., and testing the functionality.
4. **Interfacing Chronos eZ430:** Chronos device is a programmable texas instruments watch which can be used for multiple purposes like PPT control, Mouse operations etc., Exploit the features of the device by interfacing with devices.
5. **ON/OFF Control Based On Light Intensity:** Using the light sensors, monitor the surrounding light intensity & automatically turn ON/OFF the high intensity LED's by taking some pre-defined threshold light intensity value.
6. **Battery Voltage Range Indicator:** Monitor the voltage level of the battery and indicating the same using multiple LED's (for ex: for 3V battery and 3 led's, turn on 3 led's for 2-3V, 2 led's for 1-2V, 1 led for 0.1-1V & turn off all for 0V)
7. **Dice Game Simulation:** Instead of using the conventional dice, generate a random value similar to dice value and display the same using a 16X2 LCD. A possible extension could be to provide the user with option of selecting single or double dice game.
8. **Displaying RSS News Feed On Display Interface:** Displaying the RSS news feed headlines on a LCD display connected to device. This can be adapted to other websites like twitter or other information websites. Python can be used to acquire data from the internet.
9. **Porting Openwrt To the Device:** Attempt to use the device while connecting to a wifi network using a USB dongle and at the same time providing a wireless access point to the dongle.
10. **Hosting a website on Board:** Building and hosting a simple website(static/dynamic) on the device and make it accessible online. There is a need to install server (eg: Apache) and therebyhost the website.
11. **Webcam Server:** Interfacing the regular usb webcam with the device and turn it into fully functional IP webcam & test the functionality.
12. **FM Transmission:** Transforming the device into a regular fm transmitter capable of transmitting audio at desired frequency (generally 88-108 Mhz)

Note: Devices mentioned in the above lists include Arduino, Raspbery Pi, Beaglebone

Course Outcomes:

After the Completion of the course, the students will be able to

1. Demonstrate testing and displaying on devices using Embedded Linux, Arduino, Raspbery Pi Boards.
2. Explain Programming and Interfacing of I/O devices like LED/Swith etc. using Embedded Linux, Arduino, Raspbery Pi Boards.
3. Implement dice game, battery voltage indicator, displaying news using Embedded Linux, Arduino, Raspbery Pi Boards.
4. Experiment the Web Cam Server, FM transmission, and providing wireless access point using Embedded Linux.
5. Build and host a simple website on the device and make it accessible online using Embedded Linux, Arduino, Raspbery Pi, Beaglebone boards.

(B455201) RESEARCH METHODOLOGY AND IPR

M.Tech (ES)-I Semester	L	T	P	C
	2	0	0	2

UNIT- I:
Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT- II:
Effective literature studies approaches, analysis, Plagiarism, Research ethics

UNIT- III:
Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

UNIT- IV:
Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT- V:
Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

TEXT BOOKS:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"

REFERENCE BOOKS:

1. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"
2. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
3. Mayall, "Industrial Design", McGraw Hill, 1992.
4. Niebel, "Product Design", McGraw Hill, 1974.
5. Asimov, "Introduction to Design", Prentice Hall, 1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New Technological Age", 2016.
7. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008

Course Outcomes:

After the Completion of the course, the students will be able to

1. Investigate the solution for research problem
2. Develop the research proposal and paper
3. Describe the process of patenting and development in international scenario
4. Define the patent rights,licencing and transfer of technology
5. Demonstrate the new development in IPR

(B455303) ARM MICROCONTROLLERS

M.Tech (ES)-II Semester	L	T	P	C
	3	0	0	3

ARM Embedded Systems: RISC design philosophy, ARM design philosophy, Embedded system hardware, Embedded system software.

ARM Processor Fundamentals: Registers, Current Program Status Register, Pipeline, Exceptions, Interrupts and Vector Table, Core Extensions, Architecture Revisions, ARM Processor Families.

Architecture of ARM Processors: Introduction to the architecture, Programmer's model- operation modes and states, registers, special registers, floating point registers, Behaviour of the application program status register(APSR)-Integer status flags, Q status flag, GE bits, Memory system-Memory system features, memory map, stack memory, memory protection unit (MPU), Exceptions and Interrupts-what are exceptions, nested vectored interrupt controller(NVIC), vector table, Fault handling,System control block (SCB), Debug, Reset and reset sequence.

UNIT - II

Introduction to the Arm Instruction Set: Data processing instructions, branch instructions, load-store instructions, software interrupt instructions, program status register instructions, loading constants, ARMv5E extensions, Conditional execution.

Introduction to the Thumb Instruction Set: Thumb Register Usage, ARM-Thumb Interworking, OtherBranch Instructions, Data Processing Instructions, Single-Register Load-Store Instructions, Multiple- Register Load-Store Instructions, Stack Instructions, Software Interrupt Instruction.

UNIT - III

Technical Details of ARM Cortex M Processors General information about Cortex-M3 and cortex M4 processors-Processor type, processor architecture, instruction set, block diagram, memory system, interrupt and exception support, Features of the cortex-M3 and Cortex-M4 Processors- Performance, code density, low power, memory system, memory protection unit, interrupt handling, OS support and system level features, Cortex-M4 specific features, Ease of use, Debug support, Scalability, Compatibility.

UNIT - IV

Instruction SET of ARM Cortex M Background to the instruction set in ARM Cortex-M Processors, Comparison of the instruction set in ARM Cortex-M Processors, understanding the assembly language syntax, Use of a suffix in instructions, Unified assembly Language (UAL), Instruction set, Cortex-M4- specific instructions, Barrel shifter, Accessing special instructions and special registers in Programming.

UNIT -V

Floating Point Operations About Floating Point Data,Cortex-M4 Floating Point Unit (FPU)- overview, FP registers overview, CPACR register, Floating point register bank, FPSCR, FPU->FPCCR, FPU- & gt; FPCAR, FPU->FPDSCR, FPU->MVFR0, FPU->MVFR1. ARM Cortex-M4 and DSP

Applications: DSP on a microcontroller, Dot Product example, writing optimized DSP code for the CortexM4-Biquad filter, Fast Fourier transform, FIR filter.

TEXT BOOKS:

1. Andrew N. SLOSS, Dominic SYMES, Chris WRIGHT- ARM System Developer's GuideDesigning and Optimizing System Software, Elsevier Publications, 2004.
2. Joseph Yiu, The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors by Elsevier Publications, 3rd Ed.,

REFERENCE BOOKS:

1. Steve Furber - Arm System on Chip Architectures –Edison Wesley, 2000.
2. David Seal - ARM Architecture Reference Manual, Edison Wesley, 2000.

Course Outcomes:

After the Completion of the course, the students will be able to

1. Explore the selection criteria of ARM processors by understanding the functional level trade off issues.
2. Explore the ARM development towards the functional capabilities.
3. Work with ASM level program using the instruction set.
4. Programming the ARM Cortex M3.
5. Programming the ARM Cortex M3.

(B455304) DIGITAL CONTROL SYSTEMS

M.Tech (ES)-II Semester	L	T	P	C
	3	0	0	3

UNIT- I: REPRESENTATION OF DISCRETE TIME SYSTEMS

Basics of Digital Control Systems. Discrete representation of continuous systems. Sample and hold circuit. Mathematical Modeling of sample and hold circuit. Effects of Sampling and Quantization. Choice of sampling frequency. ZOH equivalent.

Z-Transforms, Mapping from s-plane to z plane, Properties of Z-Transforms and Inverse Z Transforms. Pulse Transfer function: Pulse transfer function of closed loop systems. Solution of Discrete time systems. Time response of discrete time system, Steady State errors.

UNIT- II: DISCRETE TIME STATE SPACE ANALYSIS

State space representation of discrete time systems, Conversion of pulse transfer function to state space models and vice-versa, Solving discrete time state space equations, State Transition Matrix, Pulse Transfer Function Matrix. Discretization of continuous time state space equations. Concept of Controllability, stabilizability, observability, reachability – Controllability and observability tests. Effect of pole zero cancellation on the controllability & observability.

UNIT- III: STABILITY ANALYSIS OF DISCRETE TIME SYSTEM

Concept of stability in z-domain, Stability analysis discrete time system: by Jury test, using bilinear transformation. Stability Analysis of discrete time systems using Lyapunov methods.

UNIT- IV: DESIGN OF DIGITAL CONTROL SYSTEM BY CONVENTIONAL METHODS

Design and realization of digital PID Controller, Design of discrete time controllers with bilinear transformation, Design of digital control system with dead beat response, Practical issues with dead beat response design.

UNIT-V: DESIGN STATE FEEDBACK CONTROLLERS AND OBSERVERS

Design of discrete state feedback controllers through pole placement, Design of Discrete Observer for LTI System: Design of full order and reduced observers, Design of observer-based controllers.

TEXT BOOKS:

1. K. Ogata, “Digital Control Engineering”, Prentice Hall, Englewood Cliffs, 1995.
2. M. Gopal, “Digital Control Engineering”, Wiley Eastern, 1988.
3. V, I, George and C. P. Kurian, Digital Control Systems, CENGAGE Learning, 2012

REFERENCE BOOKS:

1. G. F. Franklin, J. D. Powell and M. L. Workman, “Digital Control of Dynamic Systems”, Addison-Wesley,1998.
2. B.C. Kuo, “Digital Control System”, Holt, Rinehart and Winston, 1980.

Course Outcomes:

After the Completion of the course, the students will be able to

1. Obtain discrete representation of LTI systems.
2. Determine the state space analysis of discrete time systems, test and analyze the controllability and observability for discrete time systems
3. Analyze stability of discrete time systems using various methods
4. Design and analyze digital controllers.
5. Design state feedback controllers and observers

(B455407) IOT ARCHITECTURES AND SYSTEM DESIGN
(PROFESSIONAL ELECTIVE – III)

M.Tech (ES)-II Semester	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

UNIT - I

IoT introduction: Introduction and definition of IoT, Evolution of IoT, IoT growth, Application areas of IoT, Characteristics of IoT, IoT stack, Enabling technologies, IoT levels, IoT sensing and actuation, Sensing types, Actuator types.

UNIT - II

IoT and M2M: M2M to IoT – A Basic Perspective– Introduction, Differences and similarities between M2M and IoT, SDN and NFV for IoT.M2M Value Chains, IoT Value Chains, An emerging industrial structure for IoT, The international driven global value chain and global information monopolies.

UNIT - III

IoT Hands-on: Introduction to Arduino Programming, Integration of Sensors and Actuators with Arduino. Introduction to Python programming, Introduction to Raspberry Pi, Interfacing Raspberry Pi with basic peripherals, Implementation of IoT with Raspberry Pi.

UNIT - IV

IoT Architecture: IoT Architecture components, Comparing IoT architectures, A simplified IoT architecture, The core IoT functional stack, IoT data management and compute stack

UNIT - V

IoT System design: Challenges associated with IoT, Emerging pillors of IoT, Agricultural IoT, Vehicular IoT, Healthcare IoT, Smart cities, Transportation and logistics.

TEXT BOOKS:

1. Sudip Misra, Anandarup Mukherjee, Arijit Roy “Introduction to IOT”, Cambridge University Press.
2. David Hanes, Gonzalo salgueiro, Patrick Grossetete, Rob barton, Jerome henry “IoTFundamentals Networking technologies, protocols, and use cases for IoT”, Cisco Press

REFERENCE BOOKS:

1. Cuno pfister, “Getting started with the internet of things”, O Reilly Media, 2011
2. Francis daCosta, “Rethinking the Internet of Things: A Scalable Approach to Connecting Everything”, 1 st Edition, Apress Publications.
3. “Internet of Things concepts and applications”, Wiley
4. Arshdeep Bahga,Vijay Madisetti “Internet of Things A Hands on approach”, Universities Press
5. Shriram K Vasudevan, RMD Sundaram, Abhishek S Nagarajan, “Internet of things” John Wileyand Sons.
6. Massimo Banzi, Michael Shiloh Make: Getting Started with the Arduino, Shroff Publisher/MakerMedia Publishers.

Course Outcomes:

After the Completion of the course, the students will be able to

1. To introduce the terminology, technology and its applications
2. Integrate the sensors and actuator depending on the applications
3. Interface the IoT and M2M with value chains
4. Write Python programming for Arduino, Raspberry Pi devices
5. Design IoT based systems such as Agricultural IoT, Vehicular IoT etc.

(B455408) DESIGN FOR TESTABILITY
(PROFESSIONAL ELECTIVE – III)

M.Tech (ES)-II Semester	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

UNIT - I

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT - II

Logic and Fault Simulation: Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT - III

Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations ofScan.

UNIT - IV

Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per- Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT - V

Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOK:

1. M.L. Bushnell, V. D. Agrawal, “Essential of Electronic Testing for Digital, Memory and MixedSignal VLSI Circuits”, Kluwer Academic Publishers.

REFERENCE BOOKS:

1. M. Abramovici, M. A. Breuer and A.D Friedman, Digital Systems and Testable Design”, Jaico Publishing House.
2. P. K. Lala, “Digital Circuits Testing and Testability”, Academic Press.

Course Outcomes:

After the Completion of the course, the students will be able to

1. Describe the fundamental concepts of verification and testing the digital circuits.
2. Understand the Simulation for Design Verification and Test Evaluation
3. Describe the Controllability and Observability along with measures of testability.
4. Design the logic for built-in-self test.
5. Describe fundamental concepts of System Configuration with Boundary Scan.

(B455409) SOC DESIGN
(PROFESSIONAL ELECTIVE – III)

M.Tech (ES)-II Semester	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

UNIT - I

ASIC: Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP)concepts.

UNIT - II

NISC: NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction- set Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

UNIT - III

Simulation: Different simulation modes, behavioral, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

UNIT - IV

Low power SoC design / Digital system Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

UNIT - V

Synthesis: Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report, analysis Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs

TEXT BOOKS:

1. Hubert Kaeslin, “Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication”, Cambridge University Press, 2008.
2. B. Al Hashimi, “System on chip-Next generation electronics”, The IET, 2006

REFERENCE BOOKS

1. Rochit Rajsuman, “System-on- a-chip: Design and test”, Advantest America R & D Center, 2000
2. P Mishra and N Dutt, “Processor Description Languages”, Morgan Kaufmann, 2008
3. Michael J. Flynn and Wayne Luk, “Computer System Design: System-on-Chip”. Wiley, 2011

Course Outcomes:

After the Completion of the course, the students will be able to

1. Differentiate between various design strategies like ASIC and SoC etc.Understand the basic components of SoC.
2. Explain the various architectures of the SoC.
3. Distinguish between different types of memory components of SoC.
4. understand the importance of Interconnect Customization and Configuration
5. Various Applications of SoC.

(B455410) HARDWARE AND SOFTWARE CO-DESIGN
(PROFESSIONAL ELECTIVE – IV)

M.Tech (ES)-II Semester	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

UNIT - I

Co-Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology. **Co-Synthesis Algorithms:** Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT - II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT - III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT - IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT - V

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi-language co-simulation, the cosyma system and lycos system.

TEXT BOOKS

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf –Springer, 2009.

REFERENCE BOOKS

1. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, Kluwer Academic Publishers, 2002.
2. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont, Springer,2010

Course Outcomes:

After the Completion of the course, the students will be able to

1. Acquire the knowledge on various models of Co-design.
2. Explore the interrelationship between Hardware and software in a embedded system
3. Acquire the knowledge of firmware development process and tools during Co-design.
4. Implement validation methods and adaptability.
5. Explain the design of system level specification languages

(B455411) SECURE NETWORKS
(PROFESSIONAL ELECTIVE – IV)

M.Tech (ES)-II Semester	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

UNIT -I:
Security: Need, security services, Attacks, OSI Security Architecture, one time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques.

UNIT -II
Number Theory: Introduction, Fermat's and Euler's Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

UNIT -III
Private-Key (Symmetric) Cryptography: Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.

UNIT -IV
Public-Key (Asymmetric) Cryptography: RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC.

UNIT -V
Authentication and System Security: IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer, Secure Electronic Transaction Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, Virus Countermeasures, Firewalls, Trusted Systems.

TEXT BOOKS:
1. William Stallings, "Cryptography and Network Security, Principles and Practices", PearsonEducation, 3rd Edition.
2. Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, PrivateCommunication in a Public World", Prentice Hall, 2nd Edition

REFERENCE BOOKS:
1. Christopher M. King, Ertem Osmanoglu, Curtis Dalton, "Security Architecture, DesignDeployment and Operations", RSA Press,
2. Stephen Northcutt, Leny Zeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, "Inside Network Perimeter Security", Pearson Education, 2nd Edition
3. Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding IncidentDetection and Response", William Pollock Publisher, 2013.

Course Outcomes:

After the Completion of the course, the students will be able to

1. Illustrate the underlying principles and techniques for network and communication security
2. Interpret the Number theory and various Algorithms used for network security
3. Build various techniques for Private-Key Cryptography
4. Develop various cryptography algorithms used for Public key generation
5. Distinguish among different types of threats to the system and handle the same.

(B455412) PHYSICAL DESIGN AUTOMATION
(PROFESSIONAL ELECTIVE – IV)

M.Tech (ES)-II Semester	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

UNIT - I
Introduction to VLSI Physical Design Automation: Design Representation, VLSI Design Styles, and VLSI Physical Design automation.

UNIT - II
Partitioning, Floor planning, Pin Assignment, Standard cell, Performance issues in circuit layout, delay models, Layout styles.

UNIT - III
Placement: Problem formulation, classification, Simulation based placement algorithms, Partitioning based placement algorithms, Time driven and performance driven placement.

UNIT - IV
Global routing: Problem formulation, classification of global routing, Maze routing algorithms, Line- Probe algorithms, and shortest path based algorithms, Steiner Tree based algorithms, Integer programming based approach, Performance driven routing.
Detailed Routing: Problem formulation, classification, Single layer, two layer, three layer and Multi-Layerchannel routing, Algorithms, Switch box routing.

UNIT - V
Over the Cell Routing - Single layer and two-layer routing: Over the cell routing, Two Layer, Three Layer and Multi-Layer OTC Routing.
Via Minimization: Constraint and Unconstrained via minimization.
Clock and Power Routing: Clocking schemes, design considerations for the clock, Problem formulation, Clock routing algorithms, Skew and Delay reduction by Pin Assignment, Multiple clock routing, Power and Ground Routing

TEXT BOOKS:

1. Algorithms for VLSI Physical Design Automation – Naveed Sherwani, 3rd Ed., 2005,
2. Algorithms for VLSI Design Automation, S.H.Gerez, 1999, WILEY Student Edition, John wiley&Sons (Asia) Pvt. Ltd.

REFERENCE BOOKS:

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, 1993, Wiley.
2. Modern VLSI Design: Systems on silicon – Wayne Wolf, 2nd ed., 1998, Pearson EducationAsia

Course Outcomes:

After the Completion of the course, the students will be able to

1. Implement automation process for VLSI System design.
2. Design of floor planing, circuit layout and layout styles
3. Familiarize to use various physical design CAD tools
4. Implementation of Global routing
5. Develop and enhance the existing algorithms and computational techniques for physical design process of VLSI systems

(B455503) ARM MICROCONTROLLERS LAB

M.Tech (ES)-II Semester	L	T	P	C
	0	0	4	2

List of Assignments:

Part A) Experiments to be carried out on Cortex-M3 development boards and using GNU tool- chain

1. Blink an LED with software delay, delay generated using the SysTicktimer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED onceevery five switch presses.
5. UART Echo Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGB LED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a microphone and display sound levels on LEDs.

Course Outcomes:

After the Completion of the course, the students will be able to

1. Install, configure and utilize tool sets for developing applications based on ARM processor core SoC and DSP processor
2. Develop prototype codes using commonly available on and off chip peripherals on the Cortex M3 and DSP development boards.
3. Use the External hardware to Interface various sensors with LPC1768 Microcontroller
4. Use the External hardware to Interface various Input and Output devices with LPC1768 Microcontroller
5. Implement embedded systems with Embedded operating systems

(B455504) DIGITAL CONTROL SYSTEMS LAB

M.Tech (ES)-II Semester	L	T	P	C
	0	0	4	2

Perform the following experiments in real time by interfacing with the related hardware.

List of Experiments:

1. PWM pulse generation
2. Three phase voltage monitoring using A/D converter.
3. Three phase current monitoring using A/D converter.
4. Speed monitoring of AC motor.
5. Sine PWM pulse generation.
6. Inverter output voltage control.
7. Control of AC motor using UFD.
8. Control of DC motor using DC drive.

Course Outcomes:

After the Completion of the course, the students will be able to

1. Generate PWM pulses using various PWM techniques
2. Demonstrate three phase voltage monitoring and current monitoting using A/D converter
3. Monitor the speed of AC motor
4. Control the iverter output voltage
5. Control AC and DC motor

(B455413) EMBEDDED NETWORKS
(PROFESSIONAL ELECTIVE – V)

M.Tech (ES)-III Semester	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

UNIT –I

Embedded Communication Protocols: Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire.

UNIT –II

USB and CAN Bus: USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USBInterface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.

UNIT –III

Ethernet Basics: Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers –Using the internet in local and internet communications – Inside the Internet protocol.

UNIT –IV

Embedded Ethernet: Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT –V

Wireless Embedded Networking: Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.

TEXT BOOKS

1. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, TonyGivargis, John & Wiley Publications, 2002
2. Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port - JanAxelson, Penram Publications, 1996.

REFERENCE BOOKS

1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series -Dogan Ibrahim, Elsevier 2008.
2. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003.
3. Networking Wireless Sensors - Bhaskar Krishnamachari, Cambridge press 2005.

Course Outcomes:

After the Completion of the course, the students will be able to

1. To explain different types of Embedded communication protocols
2. To interface USB and CAN Bus based on data flow rate
3. To identify the elements of Networks and their design choices
4. To Exchange the messages using UDP of TCP Protocols
5. To Establish a WSN for the embedded applications

(B455414) CMOS MIXED SIGNAL DESIGN
(PROFESSIONAL ELECTIVE – IV)

M.Tech (ES)-III Semester	L	T	P	C
	3	0	0	3

UNIT - I

Switched Capacitor Circuits

Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT - II

Phased Lock Loop (PLL)

Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT - III

Data Converter Fundamentals

DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters.

UNIT - IV

Nyquist Rate A/D Converters

Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT - V

Oversampling Converters

Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A.

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002.
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford UniversityPress, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013.

REFERENCE BOOKS:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van DePlassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

Course Outcomes:

After the Completion of the course, the students will be able to

1. Explain the concept of the switched capacitor circuits.
2. Various step in design criteria of the PLL.
3. Analyse the various types of the A/D converters
4. Discuss the different types D/A converters
5. Demonstrate different filter with least interference and Ability to evaluate mixed signal designs

(B455415) HUMAN MACHINE INTERFACE
(PROFESSIONAL ELECTIVE – IV)

M.Tech (ES)-III Semester	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

UNIT - I

Basics of User Interface

Importance of user interface- Definition, importance of good design, benefits of good design, brief history of human-computer interface, Graphical User Interface, Popularity of Graphics, Concept of Direct Manipulation, Graphical Systems, Characteristics of GUI, Web user interface popularity, Characteristics and Principles of user interface

UNIT – II

Foundations of Human Computer Interface

The Human: I/O channels – Memory – Reasoning and problem solving; The Computer: Devices – Memory – processing and networks; Interaction: Models – frameworks – Ergonomics – styles – elements – interactivity- Paradigms. - Case Studies

UNIT – III

Design Process

Interactive Design: Basics – process – scenarios – navigation – screen design – Iteration and prototyping. HCI in software process: Software life cycle – usability engineering – Prototyping in practice
– design rationale. Design rules: principles, standards, guidelines, rules. Evaluation Techniques – Universal Design

UNIT – IV

Models and Theories

HCI Models: Cognitive models: Socio-Organizational issues and stakeholder requirements, Communication and collaboration models-Hypertext, Multimedia and WWW.

UNIT - V

Windows and Interaction Devices

Window characteristics, Components of window, Window Presentation Style, Types of windows, Organizing window functions, Characteristics of input devices, Selection of proper input devices, Output devices

TEXT BOOKS:

1. Wilbert O. Galitz - The essential Guide to User Interface Design, 3rd Ed.,Wiley, 2007 (Unit I & V)
2. Alan Dix, Janet Finlay, Gregory Abowd, Russell Beale, ―Human Computer Interaction‖, 3rd Ed., Pearson Education, 2004 (UNIT II, III & IV)

REFERENCE BOOKS:

1. Daniel Newman, Olivier Blanchard – Human/Machine: The Future of our partnership with machine,
2. Paul R. Daugherty, H. James Wilson – Human+Machine: Reimagining work in the Age of AI Hardcover, Kindle Ed.,

Course Outcomes:

After the Completion of the course, the students will be able to

1. Design effective dialog for HCI
2. Design Effective HCI for Individuals and Persons with Desiabilities
3. Assess the importance of user feedback
4. Explain the HCI implications for designing multimedia/ e-learning Web sites
5. Develop meaningful user interface

(B400701) ENGLISH FOR RESEARCH PAPER WRITING (Audit Course - I & II)

M.Tech (ES)	**L**	**T**	**P**	**C**
	2	**0**	**0**	**0**

UNIT-I:
Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT-II:
Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction

UNIT-III:
Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

UNIT-IV:
key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills areneeded when writing an Introduction, skills needed when writing a Review of the Literature,

UNIT-V:
skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions. useful phrases, how to ensure paper is as good as it could possibly be the first- time submission

TEXT BOOKS/ REFERENCES:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman'sbook.
4. Adrian Wallwork, English for Writing Research Papers, Springer New York DordrechtHeidelberg London, 2011

(B400702) DISASTER MANAGEMENT (Audit Course - I & II)

M.Tech (ES)	L	T	P	C
	2	0	0	0

UNIT-I:

Introduction:

Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

Disaster Prone Areas in India:

Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics

UNIT-II:

Repercussions of Disasters and Hazards:

Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

UNIT-III:

Disaster Preparedness and Management:

Preparedness: Monitoring of Phenomena Triggering A Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT-IV:

Risk Assessment Disaster Risk:

Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

UNIT-V:

Disaster Mitigation:

Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

TEXT BOOKS/ REFERENCES:

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'NewRoyal book Company.
2. Sahni, Pardeep Et. Al. (Eds.)," Disaster Mitigation Experiences and Reflections", Prentice Hall ofIndia, New Delhi.
3. Goel S. L., Disaster Administration and Management Text and Case Studies", Deep &Deep Publication Pvt. Ltd., New Delhi.

(B400703) SANSKRIT FOR TECHNICAL KNOWLEDGE (Audit Course - I & II)

M.Tech (ES)	**L**	**T**	**P**	**C**
	2	**0**	**0**	**0**

UNIT-I:
Alphabets in Sanskrit,

UNIT-II:
Past/Present/Future Tense, Simple Sentences

UNIT-III:
Order, Introduction of roots,

UNIT-IV:
Technical information about Sanskrit Literature

UNIT-V:
Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

TEXT BOOKS/ REFERENCES:

1. "Abhyaspustakam" – Dr. Vishwas, Samskrita-Bharti Publication, New Delhi
2. "Teach Yourself Sanskrit" Prathama Deeksha-Vempati Kutumbshastri, Rashtriya SanskritSansthanam, New Delhi Publication
3. "India's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., New Delhi.

Course Outcomes: Students will be able to

1. Understanding basic Sanskrit language
2. Ancient Sanskrit literature about science & technology can be understood
3. Being a logical language will help to develop logic in students

(B400704) VALUE EDUCATION (Audit Course - I & II)

M.Tech (ES)	L	T	P	C
	2	0	0	0

UNIT-I:
Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism. Moral and non- moral valuation. Standards and principles. Value judgements

UNIT-II:
Importance of cultivation of values. Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Unity. Patriotism. Love for nature, Discipline

UNIT-III:
Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline, Punctuality, Love and Kindness.

UNIT-IV:
Avoid fault Thinking. Free from anger, Dignity of labour. Universal brotherhood and religious tolerance. True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits. Association and Cooperation. Doing best for saving nature

UNIT-V:
Character and Competence –Holy books vs Blind faith. Self-management and Good health. Science of reincarnation, Equality, Nonviolence, Humility, Role of Women. All religions and same message. Mind your Mind, Self-control. Honesty, Studying effectively

TEXT BOOKS/ REFERENCES:

1. Chakroborty, S.K. “Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi

Course outcomes: Students will be able to

1. Knowledge of self-development
2. Learn the importance of Human values
3. Developing the overall personality

(B400705) CONSTITUTION OF INDIA (Audit Course - I & II)

M.Tech (ES)	**L**	**T**	**P**	**C**
	2	**0**	**0**	**0**

UNIT-I:
History of Making of the Indian Constitution: History Drafting Committee, (Composition & Working),
Philosophy of the Indian Constitution: Preamble**,** Salient Features.

UNIT-II:
Contours of Constitutional Rights & Duties: Fundamental Rights Right to Equality**,** Right to Freedom**,** Right against Exploitation**,** Right to Freedom of Religion**,** Cultural and Educational Rights**,** Right to Constitutional Remedies, Directive Principles of State Policy**,** Fundamental Duties.

UNIT-III:
Organs of Governance: Parliament**,** Composition**,** Qualifications and Disqualifications**,** Powers and Functions**,** Executive**,** President**,** Governor**,** Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualification, Powers and Functions.

UNIT-IV:
Local Administration: District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy.

UNIT-V:
Election Commission: Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners. State Election Commission: Role and Functioning. Institute and Bodies for the welfare of SC/ST/OBC and women.

TEXT BOOKS/ REFERENCES:

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

Course Outcomes: Students will be able to:

1. Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
2. Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
3. Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
4. Discuss the passage of the Hindu Code Bill of 1956.

(B400706) PEDAGOGY STUDIES (Audit Course - I & II)

M.Tech (ES)	**L**	**T**	**P**	**C**
	2	**0**	**0**	**0**

UNIT-I:

Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions**.** Overview of methodology and Searching.

UNIT-II:

Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

UNIT-III:

Evidence on the effectiveness of pedagogical practices, Methodology for the indepth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the scho curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.

UNIT-IV:

Professional development: alignment with classroom practices and follow-up support, Peer support, Support from the head teacher and the community. Curriculum and assessment, Barriers to learning: limited resources and large class sizes

UNIT-V:

Research gaps and future directions: Research design**,** Contexts**,** Pedagogy**,** Teacher education**,** Curriculum and assessment**,** Dissemination and research impact.

TEXT BOOKS/ REFERENCES:

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31(2): 245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher educationresearch project (MUSTER) country report 1. London: DFID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, 'learning to read' campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

Course Outcomes: Students will be able to understand:

1. What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries?
2. What is the evidence on the effectiveness of these pedagogical practices, in what conditions,and with what population of learners?
3. How can teacher education (curriculum and practicum) and the school curriculum and guidancematerials best support effective pedagogy?

(B400707) STRESS MANAGEMENT BY YOGA (Audit Course - I & II)

M.Tech (ES)	**L**	**T**	**P**	**C**
	2	**0**	**0**	**0**

UNIT-I:
Definitions of Eight parts of yog. (Ashtanga)

UNIT-II:
Yam and Niyam.

UNIT-III:
Do`s and Don't's in life.
i) Ahinsa, satya, astheya, bramhacharya and aparigraha
ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan

UNIT-IV:
Asan and Pranayam

UNIT-V:
i) Various yog poses and their benefits for mind & body
ii) Regularization of breathing techniques and its effects-Types of pranayam

TEXT BOOKS/ REFERENCES:

1. 'Yogic Asanas for Group Tarining-Part-I": Janardan Swami Yogabhyasi Mandal, Nagpur 2."Rajayoga or conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata

Course Outcomes: Students will be able to:

1. Develop healthy mind in a healthy body thus improving social health also
2. Improve efficiency

(B400708) PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS
(Audit Course - I & II)

M.Tech (ES)	**L**	**T**	**P**	**C**
	2	**0**	**0**	**0**

UNIT-I:

Neetisatakam-Holistic development of personality

- Verses- 19,20,21,22 (wisdom)
- Verses- 29,31,32 (pride & heroism)
- Verses- 26,28,63,65 (virtue)

UNIT-II:

Neetisatakam-Holistic development of personality

- Verses- 52,53,59 (dont's)
- Verses- 71,73,75,78 (do's)

UNIT-III:

Approach to day to day work and duties.

- Shrimad Bhagwad Geeta: Chapter 2-Verses 41, 47,48,
- Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23, 35,
- Chapter 18-Verses 45, 46, 48.

UNIT-IV:

Statements of basic knowledge.

- Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68
- Chapter 12 -Verses 13, 14, 15, 16,17, 18
- Personality of Role model. Shrimad Bhagwad Geeta:

UNIT-V:

- Chapter2-Verses 17, Chapter 3-Verses 36,37,42,
- Chapter 4-Verses 18, 38,39
- Chapter18 – Verses 37,38,63

TEXT BOOKS/ REFERENCES:

1. "Srimad Bhagavad Gita" by Swami Swarupananda Advaita Ashram (Publication Department),Kolkata.
2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya SanskritSansthanam, New Delhi.

Course Outcomes: Students will be able to

1. Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life
2. The person who has studied Geeta will lead the nation and mankind to peace and prosperity
3. Study of Neetishatakam will help in developing versatile personality of students

(B455601) EMBEDDED SYSTEMS
(Open Elective)

	L	T	P	C
M.Tech (ES)	**3**	**0**	**0**	**3**

UNIT-I: Embedded Computing & CPU fundamentals

Embedded Computing: Microprocessors, embedded design process, system description formalisms. Instruction sets- CISC and RISC;

CPU fundamentals: programming I/Os, co-processors, supervisor mode, exceptions, memory management units and address translation, pipelining, super scalar execution, caching, CPU power consumption.

UNIT-II: **Embedded computing platform & Program design and analysis**

Embedded Computing platform: CPU bus, memory devices, I/O devices, interfacing, designing with microprocessors, debugging techniques.

Program design and analysis: models of program, assembly and linking, compilation techniques, analysis and optimization of execution time, energy, power and size.

UNIT-III: Processes and operating systems

Multiple tasks and multiple processes, context switching, scheduling policies, inter-process communication mechanisms.

UNIT-IV: Hardware accelerators & Networks

Hardware accelerators: CPUs and accelerators, accelerator systemdesign.

Networks: Distributed embedded architectures, networks for embeddedsystems, network-based design and Internet-enabled systems.

UNIT-V: System design techniques

Design methodologies, requirements analysis, system analysis and architecture design, quality assurance.

Text Books:

1. Wolf, W. Computers as components- Principles of embeddedcomputing system design. Academic Press (Indian edition available from Harcourt India Pvt. Ltd., 27M Block market, Greater Kailash II,New Delhi-110 048.)

Reference Books

1. Manuel Jiménez Rogelio, PalomeraIsidoro Couvertier "Introduction to Embedded Systems Using Microcontrollers and the MSP430" Springer Publications, 2014.
2. Frank Vahid, Tony D. Givargis, "Embedded system Design: A Unified Hardware/Software Introduction", John Wily & Sons Inc.2002.
3. Peter Marwedel, "Embedded System Design", Science Publishers, 2007.

Course Outcomes:

After the Completion of the course, the students will be able to

1. Explain the Embedded design process and CPU Fundamentals
2. Understand Embedded computing platform and program design.
3. Explain Scheduling policies and inter process mechanisms in Embedded systems
4. Evaluate the Hardware accelerators & networks for Embedded system.
5. Explain various System design methodologies and quality assurance.

(B420601) DISASTER MANAGEMENT
(Open Elective)

Course: M. Tech (ES)

L	T	P	C
3	0	0	3

UNIT-I:

Introduction: Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude. Disaster Prone Areas in India: Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics

UNIT-II:

Repercussions of Disasters and Hazards: Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

UNIT-III:

Disaster Preparedness and Management: Preparedness: Monitoring of Phenomena Triggering A Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT-IV:

Risk Assessment Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

UNIT-V:

Disaster Mitigation: Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

TEXT BOOKS/ REFERENCES:

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'New Royal book Company.
2. Sahni, Pardeep Et. Al. (Eds.)," Disaster Mitigation Experiences and Reflections", Prentice Hall of India, New Delhi.
3. Goel S. L., Disaster Administration and Management Text and Case Studies", Deep &Deep Publication Pvt. Ltd., New Delhi.

(B443601) PHOTOVOLTAIC SYSTEMS
(Open Elective)

L	T	P	C
3	0	0	3

M. Tech (ES)

UNIT-I:
SOLAR ENERGY
Sun and Earth, Solar Spectrum, Solar Geometry, Solar radiation on horizontal and inclined planes, Instruments for measurement of solar radiation, Solar cell, Equivalent circuit, V-I characteristics, Performance improvement.

UNIT-II:
SOLAR CELLS
Manufacture of Solar Cells-Technologies, Design of Solar cells, Photovoltaic modules, Design requirements, Encapsulation systems, Manufacture, Power rating, Hotspot effect, Design qualifications.

UNIT-III:
PROTECTION AND MEASUREMENTS
Flat plate arrays, Support structures, Module interconnection and cabling, Lightning protection, Performance measurement using natural sun light and simulator, Determination of temperature coefficients, Internal series resistance, Curve correction factor.

UNIT-IV:
PHOTOVOLTAIC SYSTEMS
Photovoltaic systems, Types, General design considerations, System sizing, Battery sizing, Inverter sizing, Design examples, Balance of PV systems.

UNIT-V:
MAXIMUM POWER POINT TRACKERS
Maximum power point trackers, Perturb and observe, Incremental conductance method, Hill climbing method, , Hybrid and complex methods, Data based and other approximate methods, Instrument design, Other MPP techniques, Grid interactive PV system.

TEXTBOOKS:
1. F.C.Treble, “Generating electricity from Sun”, Pergamon Press.
2. A.K.Mukherjee, Nivedita Thakur,”Photovoltaic systems: Analysis and design”, PHI, 2011.

REFERENCES:
1. C.S.Solanki,” Solar Photovoltaic’s: Fundamentals, Technologies and applications”, PHI, 2009.

Course Outcomes: After completion of the course, students will be able to:
1. Identify photovoltaic system components and system types
2. Calculate electrical energy and power
3. Correctly size system components, design considerations of solar equipment
4. Design a basic grid-tie PV system.
5. Apply different MPPT techniques to PV systems.

(B458601) OPTIMIZATION TECHNIQUES

(Open Elective)

M. Tech (ES)

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UNIT - I

Introduction and Classical Optimization Techniques: Statement of an Optimization problem – design vector – design constraints – constraint surface – objective function – objective function surface -classification of Optimization problems.

Linear Programming: Standard form of a linear programming problem – geometry of linear programming problems – definitions and theorems – solution of a system of linear simultaneous equations – pivotal reduction of a general system of equations – motivation to the simplex method –simplex algorithm.

UNIT - II

Transportation Problem: Finding initial basic feasible solution by north – west corner rule, least cost method and Vogel's approximation method – testing for optimality of balanced transportation problems. Degeneracy. Assignment problem – Formulation – Optimal solution - Variants of Assignment Problem; Traveling Salesman problem.

UNIT - III

Classical Optimization Techniques: Single variable Optimization – multi variable Optimization without constraints – necessary and sufficient conditions for minimum/maximum – multivariable Optimization with equality constraints: Solution by method of Lagrange multipliers – Multivariable Optimization with inequality constraints: Kuhn – Tucker conditions.

Single Variable Nonlinear Unconstrained Optimization: Elimination methods: Uni Model function-its importance, Fibonacci method & Golden section method.

UNIT - IV

Multi variable nonlinear unconstrained optimization: Direct search methods – Univariant method, Pattern search methods – Powell's, Hooke - Jeeves, Rosenbrock's search methods. Gradient methods: Gradient of function & its importance, Steepest descent method, Conjugate direction methods: Fletcher- Reeves method & variable metric method.

UNIT - V

Dynamic Programming: Dynamic programming multistage decision processes – types – concept of sub optimization and the principle of optimality – computational procedure in dynamic programming – examples illustrating the calculus method of solution - examples illustrating the tabular method of solution.

TEXTBOOKS:

1.Optimization Techniques & Applications by S.S.Rao, New Age International. 2.Optimization for Engineering Design by Kalyanmoy Deb, PHI

REFERENCES:

1. George Bernard Dantzig, Mukund Narain Thapa, "Linear programming", Springer series in Operations Research 3rd edition, 2003.
2. H. A. Taha, "Operations Research: An Introduction", 8th Edition, Pearson/Prentice Hall, 2007.
3.Optimization Techniques by Belegundu & Chandrupatla, Pearson Asia.
4.Optimization Techniques Theory and Practice by M.C. Joshi, K.M. Moudgalya, Narosa Publications

Course Outcomes: After completion of this course, the student will be able to:

1. Explain the need of optimization of engineering systems.
2. Understand optimization of electrical and electronics engineering problems.
3. Apply classical optimization techniques, linear programming, simplex algorithm, transportation problem.
4. Apply unconstrained optimization and constrained non-linear programming and dynamic programming.
5. Formulate optimization problems.

(B4A3604) DIGITAL FORENSICS

(Open Elective)

M.Tech (ES) **L T P C**
3 0 0 3

UNIT - I

Digital Forensics Science: Forensics science, computer forensics, and digital forensics.

Computer Crime: Criminalistics as it relates to the investigative process, analysis of cyber criminalistics area, holistic approach to cyber-forensics

UNIT - II

Cyber Crime Scene Analysis:

Discuss the various court orders etc., methods to search and seizure electronic evidence, retrieved and un-retrieved communications, Discuss the importance of understanding what court documents would be required for a criminal investigation.

UNIT - III

Evidence Management & Presentation:

Create and manage shared folders using operating system, importance of the forensic mindset, define the workload of law enforcement, Explain what the normal case would look like, Define who should be notified of a crime, parts of gathering evidence, Define and apply probable cause.

UNIT - IV

Computer Forensics: Prepare a case, Begin an investigation, Understand computer forensics workstations and software, Conduct an investigation, Complete a case, Critique a case, **Network Forensics:** open-source security tools for network forensic analysis, requirements for preservation of network data.

UNIT - V

Mobile Forensics: mobile forensics techniques, mobile forensics tools.

Legal Aspects of Digital Forensics: IT Act 2000, amendment of IT Act 2008.

Recent trends in mobile forensic technique and methods to search and seizure electronic evidence

TEXT BOOKS:

1. John Sammons, The Basics of Digital Forensics, Elsevier
2. John Vacca, Computer Forensics: Computer Crime Scene Investigation, Laxmi Publications

REFERENCES:

1. William Oettinger, Learn Computer Forensics: A beginner's guide to searching, analyzing, and securing digital evidence, Packt Publishing; 1st edition (30 April 2020), ISBN: 1838648178.
2. Thomas J. Holt, Adam M. Bossler, Kathryn C. Seigfried-Spellar, Cybercrime and Digital Forensics: An Introduction, Routledge.

Course Outcomes: On completion of the course the student should be able to

1. Understand relevant legislation and codes of ethics.
2. Computer forensics and digital detective and various processes, policies and procedures.
3. E-discovery, guidelines and standards, E-evidence, tools and environment.
4. Email and web forensics and network forensics.