H.T No: | | | | | | | | | | | R22

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(UGC AUTONOMOUS)

Examination	:	**M.Tech II Semester Regular & Supplementary Examinations August-2025**
Course Name	:	**ARM Microcontrollers**
Course Code	:	**B455303**
Branch	:	**Embedded Systems**
Date & Session	:	**25-08-2025 AN** **Duration: 3 hours** **Max. Marks: 60**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions

Each question carries ONE mark. **10x1=10M**

1.	Mention any two features of ARM design philosophy.	1 M
2.	Identify the use of the vector table in the ARM architecture.	1 M
3.	List any two branch instructions in the Thumb instruction set.	1 M
4.	Define interworking in ARM-Thumb modes	1 M
5.	Mention two low-power features of Cortex-M3.	1 M
6.	State the use of the system control block (SCB).	1 M
7.	List any two features of the Cortex-M instruction set.	1 M
8.	Write the syntax of a unified assembly instruction.	1 M
9.	Which ARM feature supports Fast Fourier Transform (FFT)?	1 M
10.	State the purpose of MVFR0 and MVFR1.	1 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A).	i) Classify ARM processor families and their use cases.	5M
	ii) Illustrate ARM pipeline operation with a diagram and example.	5M
	OR	
11. B).	i) Discuss the role of interrupts and vector tables in ARM.	6M
	ii) Explain memory protection mechanisms in ARM-based embedded systems.	4M
12. A).	i) Explain the ARMv5E extensions with examples.	5M
	ii) Discuss single-Register transfer load store instructions with syntax.	5M
	OR	
12. B).	i) Explain the register usage difference between ARM and Thumb modes.	5M
	ii) Describe the conditional execution of ARM instructions with examples.	5M
13. A).	Describe the architecture and main features of the ARM Cortex-M3 processor using a block diagram.	10M
	OR	
13. B).	i) Explain the scalability and configurability options in Cortex-M4.	5M
	ii) Explain the memory protection mechanisms in Cortex-M.	5M

(P.T.O..)

14. A). Analyze the role of special instructions like REV, ROR, and CLZ in Cortex-M. 10M

OR

14. B). i) Differentiate between conditional and unconditional execution in Cortex-M instructions. 5M

ii) List and explain the key categories of instructions in Cortex-M4. 5M

15. A). Describe the role of the FPU register bank in Cortex-M4. How are floating-point operands stored and accessed? 10M

OR

15. B). Discuss the significance of the Fast Fourier Transform (FFT) in signal processing. How can Cortex-M4 optimize FFT computations? 10M

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Examination : **M.Tech II Semester Regular & Supplementary Examinations Aug/Sept-2025**
Course Name : **Hardware and Software Co-Design**
Course Code : **B455410**
Branch : **Embedded Systems**
Date & Session : **02-09-2025 AN** **Duration: 3 hours** **Max. Marks: 60**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions

Each question carries ONE mark. **10x1=10M**

1. What is the main objective of hardware-software co-design? 1 M
2. Name a language used in co-design. 1 M
3. What is a target architecture? 1 M
4. What are mixed systems? 1 M
5. What is the role of a compiler in embedded systems? 1 M
6. Name a tool used for embedded processor design. 1 M
7. What is design verification? 1 M
8. Why is design specification important? 1 M
9. What is system-level synthesis? 1 M
10. Name a system-level specification language. 1 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A). i) What is meant by software co-design? Explain the co-design models. 5M
ii) List the different blocks in VLIW architecture and explain. 5M

OR

11. B). i) What is meant by co-synthesis? Describe the distribution system co-synthesis. 5M
ii) Discuss about RISC and CISC architectures. 5M

12. A). i) Explain in detail about prototyping and emulation techniques. 5M
ii) Discuss about prototyping and emulation environments. 5M

OR

12. B). i) Explain the architecture of control dominated system. 5M
ii) Discuss about mixed system. 5M

13. A). What is a compiler development environment? Explain it with a suitable circuit. 10M

OR

13. B). i) What is the need for embedded software development? 5M
ii) Write a short note on compilation techniques. 5M

(P.T.O..)

14. A). i) What is meant by co-design? Explain the co-design computational model. 5M

ii) How is design verification carried out? 5M

OR

14. B). Explain about concurrency in design specifications and verification. 10M

i) Non determinism.

ii) Synchronous and asynchronous computations.

15. A). i) What is meant by Heterogeneous specification? Discuss about Multi-language co-simulation. 5M

ii) Write short notes on System level specification languages. 5M

OR

15. B). i) What are the new trends in COSYMA system? 5M

ii) Discuss how design representation for system level synthesis is done. 5M

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Examination : **M.Tech II Semester Regular & Supplementary Examinations Aug/Sept-2025**
Course Name : **Digital Control Systems**
Course Code : **B455304**
Branch : **Embedded Systems**
Date & Session : **04-09-2025 AN** **Duration: 3 hours** **Max. Marks: 60**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions
Each question carries ONE mark. **10x1=10M**

1. What is meant by primary strip in mapping from s-plane to z-plane? 1 M
2. Define static acceleration error constant. 1 M
3. Write equation of pulse transfer function matrix. 1 M
4. List out different state space representations of discrete time system. 1 M
5. If a system is having multiple closed-loop poles, what is the stability of the system? 1 M
6. What is the difference between Jury and Lyapunov stability tests? 1 M
7. What are the practical issues with dead beat response design? 1 M
8. What are the applications of PID controllers? 1 M
9. How many types of discrete state observers are available? 1 M
10. What is the principle of pole placement in state feedback controllers? 1 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A). With the help of block diagram explain the functioning of digital control system in detail. 10M

OR

11. B). Derive the mathematical model for sample and hold operation and equation for zero-order-hold. 10M

12. A). Express the diagonal canonical form for the system given below 10M

$$\frac{Y(Z)}{U(Z)} = \frac{Z+1}{Z^2+1.3Z+0.4}$$

OR

12. B). Test for controllability for the pulse transfer function given 10M

$$\frac{Y(Z)}{U(Z)} = \frac{Z+0.2}{(z+0.8)(z+0.2)}$$

13. A). Consider the discrete time unity feedback system with open-loop transfer function 10M

$$G(Z) = \frac{K(0.3679Z+0.2642)}{(Z-0.3679)(Z-1)}$$

And determine the range of K for stability using Jury test.

OR

13. B). Determine the Routh stability for the following bilinear polynomial 10M

$Q(W) = W^5 + W^4 + 2W^3 + 2W^2 + 3W + 5 = 0$

(P.T.O..)

14. A). Discuss about direct, standard, series and parallel programming realizations of PID controllers. 10M

OR

14. B). Describe the procedure of designing a digital controller with bilinear transformation. 10M

15. A). Derive the necessary and sufficient condition for design of state feedback controller through pole placement. 10M

OR

15. B). Explain the method of designing a reduced order state observer. 10M

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Examination : **M.Tech II Semester Regular & Supplementary Examinations August-2025**
Course Name : **Design for Testability**
Course Code : **B455408**
Branch : **Embedded Systems**
Date & Session : **08-09-2025 AN** **Duration: 3 hours** **Max. Marks: 60**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions

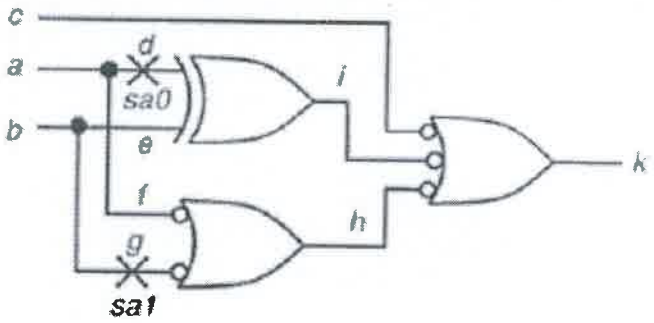
Each question carries ONE mark. **10x1=10M**

1. Define Defect? List out the different types of defects in VLSI chips? 1 M
2. Distinguish between functional testing and structural testing with examples. 1 M
3. What is meant by ATPG? Name any one ATPG technique used for stuck-at faults. 1 M
4. Compare and contrast true-value simulation and fault simulation 1 M
5. How would you use high-level testability measures in behavioral synthesis? 1 M
6. What technique would you apply to convert a latch-based design into a scan-compatible one? 1 M
7. How can BIST reduce test cost in mass production? 1 M
8. How would you choose between scan-based and logic BIST for a large SoC design? 1 M
9. Given a faulty PCB, how can boundary scan help identify connection issues? 1 M
10. How would you configure the TAP port for testing multiple devices on a board? 1 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A). Show that the two faults d: s-a-0 and g: s-a-1 are equivalent in the figure below: 10M



OR

11. B). Discuss the different levels of fault models. 10M

12. A). Compare and contrast true-value simulation and fault simulation. Provide relevant algorithms and use cases. 10M

OR

12. B). Summarize why the reverse order fault simulation is not a practical test compaction technique for sequential circuits. 10M

(P.T.O.)

13. A). Describe in detail about board level and system level DFT approaches. 10M

OR

13. B). What are the main differences between sequential SCOAP measures from the combinational measures. Explain with example. 10M

14. A). Draw the block diagram for a BIST implementation, explain the test procedure. 10M

OR

14. B). Using a diagram, explain how a memory BIST structure can be used to test embedded memories in a VLSI chip. 10M

15. A). Write a short note on Boundary scan description language. 10M

OR

15. B). How can you use boundary scan test instructions for debugging embedded logic without external access? Illustrate with a flowchart. 10M

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