CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(UGC AUTONOMOUS)

Examination	:	M.Tech I Semester Regular & Supplementary Examinations March-2025
Course Name	:	Digital System Design with FPGAs
Course Code	:	B455301
Branch	:	Embedded Systems
Date & Session	:	17-03-2025 AN Duration: 3 hours Max. Marks: 60

(Note: Assume suitable data if necessary)

PART-A
Answer all TEN questions
Each question carries ONE mark.   10x1=10M

1.	What is CPLD?	1 M
2.	What is PLA Device?	1 M
3.	Define a sequential circuit.	1 M
4.	What is sequence detector?	1 M
5.	What is the use of code converter?	1 M
6.	Define Synthesis.	1 M
7.	Define Multiple Stuck at fault.	1 M
8.	What is Transition count testing?	1 M
9.	What is Fault pair?	1 M
10.	Define fault detection and redundancy.	1 M

PART-B
Answer the following. Each question carries TEN Marks.   5x10=50M

11.A).	Compare the performance of various simple PLDs.	10M
	OR	
11. B).	Explain the general block diagram of FPGA with neat sketches.	10M
12. A).	Explain about the design of a sequential parity checker.	10M
	OR	
12. B).	What is a state graph? Explain with an example.	10M
13. A).	Explain about the Metastability in Sequential circuit design.	10M
	OR	
13. B).	Write about the Pipelining resources sharing.	10M
14. A).	Explain Fault dominance and fault location in combinational circuits.	10M
	OR	
14. B).	What are the limitations of the path sensitization method and how to overcome them?	10M
15. A).	Explain about the Machine identification.	10M
	OR	
15. B).	Explain about fault detection experiment using an example.	10M

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Examination	:	M.Tech I Semester Regular & Supplementary Examinations March-2025
Course Name	:	System Design with Embedded Linux
Course Code	:	B455302
Branch	:	Embedded Systems
Date & Session	:	19.03.2025 AN Duration: 3 hours Max. Marks: 60

(Note: Assume suitable data if necessary)

PART-A
Answer all TEN questions
Each question carries ONE mark.   10x1=10M

1. Write is an Operating System.   1 M
2. What is the Need for Task synchronization?   1 M
3. What are the services of Real Time Kernel?   1 M
4. Explain about Memory Manager.   1 M
5. What is an Ethernet?   1 M
6. Write about Interrupt handling in RTOS.   1 M
7. Explain about Programming Real Time Linux.   1 M
8. What are the applications of Linux?   1 M
9. How to build and debug in Embedded Software Programs?   1 M
10. What are BootLoaders?   1 M

PART-B
Answer the following. Each question carries TEN Marks.   5x10=50M

11.A). Explain about Task synchronization issues.   10M

OR

11. B). Differentiate between static and dynamic calls.   10M

12. A). Explain with a neat sketch Embedded Linux Architecture.   10M

OR

12. B). What is IPC? Explain the various IPC mechanisms in RTOS.   10M

13. A). Explain about Embedded device drivers.   10M

OR

13. B). Explain the functioning of USB bus with the help of neat diagram.   10M

14. A). Explain the applications of Embedded Real time Linux.   10M

OR

14. B). Differentiate between Soft Real Time Linux and Real Time Linux.   10M

15. A). Explain about system Integration and debugging In Embedded Systems.   10M

OR

15. B). Write about Root File system in debugging of Embedded software's.   10M

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Examination	:	M.Tech I Semester Regular & Supplementary Examinations March-2025
Course Name	:	CMOS VLSI Design
Course Code	:	B455401
Branch	:	Embedded Systems
Date & Session	:	21.03.2025 AN Duration: 3 hours Max. Marks: 60

(Note: Assume suitable data if necessary)
PART-A
Answer all TEN questions
Each question carries ONE mark.   10x1=10M

1.	Define Threshold voltage of a MOS Transistor.	1 M
2.	Write the merits and demerits of Pseudo-NMOS Logic.	1 M
3.	What is the advantage of using depletion loads in combinational circuits?	1 M
4.	Explain working of pass transistor logic.	1 M
5.	Draw the behavior of bistable elements.	1 M
6.	What is called latch?	1 M
7.	Write the advantages of dynamic logic circuits over static logic circuits.	1 M
8.	What is the basic principle of domino logic?	1 M
9.	Define Static RAM and dynamic RAM.	1 M
10.	Why NOR Flash memory is preferably used?	1 M

PART-B
Answer the following. Each question carries TEN Marks.   5x10=50M

11.A). Draw the Transfer characteristics of CMOS Inverter and explain various regions of operation.   10M

OR

11. B). Draw the transient response of an inverter. Derive the expression for fall time and rise time.   10M

12. A). With a detailed step by step process, design and draw the AND-OR-INVERT form complex gates in CMOS logic for the output equation   10M

$$Y = \overline{(AB + CD)}$$

OR

12. B). Design the following using Transmission gates. i) 4*1 multiplexer ii) EX-OR Gate.   10M

13. A). Draw the circuit diagram of a CMOS negative edge-triggered master-slave D flip-flop and explain the working.   10M

OR

13. B). Explain the operation of NOR based implementation of the clocked JK latch circuit. Also draw the CMOS AOI realization of the JK latch.   10M

(P.T.O..)

14. A). Implement the given function in dynamic CMOS logic and Domino CMOS logic. 10M

$$F = \overline{(A+B).(C+D)}$$

OR

14. B). Explain dynamic Voltage bootstrapping with relevant expressions. 10M

15. A). Explain about the structure of 3-Transistor RAM cell. How the read, write, hold and 10M
refresh operations take place in a DRAM cell.

OR

15. B). Explain the operation of NOR Flash with neat diagram and timing diagrams. 10M

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Examination : M.Tech I Semester Regular & Supplementary Examinations March-2025
Course Name : Advance Computer Architecture
Course Code : B455405
Branch : Embedded Systems
Date & Session : 24.03.2025 AN   Duration: 3 hours   Max. Marks: 60

(Note: Assume suitable data if necessary)
PART-A
Answer all TEN questions
Each question carries ONE mark.   10x1=10M

1.	How would you explain the concept of Locality of Reference?	1 M
2.	Illustrate the use of register indirect addressing mode.	1 M
3.	What is the formula for calculating CPU execution time?	1 M
4.	In which part of the cache can a block be stored?	1 M
5.	Explain briefly about the branch-prediction buffer?	1 M
6.	What does ILP stand for and what does it refer to?	1 M
7.	What are the two key factors that have led to the increased use of MIMD multiprocessors?	1 M
8.	How would you describe the concept of Snooping in a computing context?	1 M
9.	What is the definition of a cluster in computing?	1 M
10.	How do you calculate the total latency of a message?	1 M

PART-B
Answer the following. Each question carries TEN Marks.   5x10=50M

11.A). Discuss the key principles involved in the design of an instruction set and provide an explanation for each.   10M

OR

11. B). How do factors such as time, volume, commodification, and packaging influence the cost of a computer? Provide an explanation.   10M

12. A). What are the major challenges associated with pipelining in computer processors?   10M

OR

12. B). How does virtual memory function, and what role does it play in computer systems?   10M

13. A). How can dynamic scheduling be used to address data hazards? Explain the approach.   10M

OR

13. B). How does hardware support the exposure of additional parallelism at compile time? Describe the entire procedure.   10M

14. A). What is systematic shared-memory architecture, and how does it function?   10M

OR

14. B). What are the basic hardware primitives necessary for implementing synchronization in a multiprocessor system? Discuss.   10M

15. A). What are the practical challenges in interconnecting networks, and how can they be illustrated with examples?   10M

OR

15. B). Discuss the challenges and fallacies of implementing Intel IA-64 architecture in embedded systems.   10M

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