H.T No: | | | | | | | | | | | R22

CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(UGC AUTONOMOUS)

Examination : **M.Tech I Semester Supplementary Examinations Aug/Sept-2025**
Course Name : **CMOS VLSI Design**
Course Code : **B455401**
Branch : **Embedded Systems**
Date & Session : **01-09-2025 AN** **Duration: 3 hours** **Max. Marks: 60**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions

Each question carries ONE mark. **10x1=10M**

1.	What is pseudo NMOS logic?	1 M
2.	Compare CMOS and pseudo NMOS logic in terms of power consumption.	1 M
3.	What is a combinational logic circuit?	1 M
4.	Define NMOS load in MOS logic circuits.	1 M
5.	Define a bistable element in digital electronics.	1 M
6.	Differentiate between a latch and a flip-flop.	1 M
7.	What is dynamic logic?	1 M
8.	Define precharge and evaluate phases in dynamic logic.	1 M
9.	What are the two main types of semiconductor memory?	1 M
10.	What is the difference between NOR and NAND Flash memory?	1 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A).	Derive the expression for the inverter threshold voltage in a pseudo NMOS logic gate.	10M
	OR	
11. B).	Explain the structure and working of a pseudo NMOS inverter. Include circuit diagram and voltage transfer characteristics.	10M
12. A).	Explain the working of MOS logic circuits with NMOS loads. Illustrate with a simple NMOS inverter circuit and truth table.	10M
	OR	
12. B).	Compare CMOS and NMOS logic in terms of speed, power consumption, and noise margin.	10M
13. A).	Compare and contrast the SR latch and clocked SR latch. How does the clock input affect the operation?	10M
	OR	
13. B).	Design a CMOS D latch using transmission gates. Explain its operation with clock input.	10M
14. A).	Design a synchronous dynamic pass transistor logic circuit. Explain its working with a clocked input.	10M
	OR	
14. B).	Compare static and dynamic logic circuits. Highlight differences in area, power, speed, and design complexity.	10M

(P.T.O..)

15. A). List and explain the different types of semiconductor memory. Compare their characteristics and uses. 10M

OR

15. B). Compare SRAM and DRAM. 10M

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CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(UGC AUTONOMOUS)

Examination : **M.Tech I Semester Supplementary Examinations Aug/Sept-2025**
Course Name : **Advanced Computer Architecture**
Course Code : **B455405**
Branch : **Embedded Systems**
Date & Session : **03-09-2025 AN** **Duration: 3 hours** **Max. Marks: 60**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions
Each question carries ONE mark. **10x1=10M**

1. Define Amdahl's Law. 1 M
2. Define operand in instruction set architecture 1 M
3. What is pipelining? 1 M
4. Define a data hazard 1 M
5. What is Instruction-Level Parallelism in processors? 1 M
6. List two advantages of using Tomasulo's approach 1 M
7. Mention two advantages of using multiprocessor systems 1 M
8. What is a distributed shared memory system? 1 M
9. Mention two types of interconnection network media. 1 M
10. What are the key challenges in designing interconnection networks? 1 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A). Explain the differences in operand locations and data flow among the four instruction set architecture classes: Stack, Accumulator, Register-Memory, and Register-Register architectures. 10M

OR

11. B). Explain the factors that influence the cost of a computer system over time. 10M

12. A). Describe the concept of pipelining. Illustrate a classic five-stage MIPS pipeline and explain the role of each stage 10M

OR

12. B). Define and distinguish structural, data, and control hazards. Provide examples where each hazard occurs. 10M

13. A). Define Instruction-Level Parallelism (ILP). Explain how instructions per cycle is used as a metric to measure ILP 10M

OR

13. B). Explain dynamic scheduling? How dynamic scheduling approach exploit Instruction-Level Parallelism. 10M

(P.T.O..)

14. A). Explain how multi-processors utilize TLP to achieve performance gains. 10M

OR

14. B). Compare the performance impact of multi-threading vs multi-processing for general-purpose workloads. 10M

15. A). Explain the key practical issues encountered in designing interconnection networks for multiprocessor systems? 10M

OR

15. B). Describe the Intel IA-64 architecture and its key features for ILP. 10M

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CMR COLLEGE OF ENGINEERING & TECHNOLOGY
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Examination : **M.Tech I Semester Supplementary Examinations Aug/Sept-2025**
Course Name : **System Design with Embedded Linux**
Course Code : **B455302**
Branch : **Embedded Systems**
Date & Session : **09-09-2025 AN** **Duration: 3 hours** **Max. Marks: 60**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions
Each question carries ONE mark. **10x1=10M**

1. Explain about real time operating system. 1 M
2. List system calls. 1 M
3. Outline services of kernel. 1 M
4. Define kernel space. 1 M
5. State the SPI bus. 1 M
6. What is a kernel space driver? 1 M
7. What is a soft real time system? 1 M
8. List the applications of real time linux. 1 M
9. What is debugging? 1 M
10. What are boot loaders? 1 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A). Classify various scheduling algorithms. 10M

OR

11. B). Explain the characteristics of a real time operating system. 10M

12. A). Explain various IPC mechanisms in RTOS. 10M

OR

12. B). Identify the types of kernel and memory space. 10M

13. A). Summarize the functions of I2C bus with an example. 10M

OR

13. B). Summarize interrupt handling in embedded linux. 10M

14. A). Contrast on soft and hard real time operating systems. 10M

OR

14. B). List the applications of embedded realtime linux. 10M

15. A). Explain the significance of bootloader. 10M

OR

15. B). Examine the function of debugging and system integration. 10M

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