CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(UGC AUTONOMOUS)
B.Tech V Semester Supplementary Examinations June/July-2025
Course Name: Electronic Measurements & Instrumentation
(Electronics & Communication Engineering)

Date: 30.06.2025 FN	Time: 3 hours	Max.Marks: 70

(Note: Assume suitable data if necessary)

PART-A
Answer all TEN questions
Each question carries TWO marks.   10x2=20M

1.	What is precision? Explain.	2 M
2.	Explain about the range extension of AC voltmeters.	2 M
3.	List the applications of wave analyzers.	2 M
4.	List the applications of function generator.	2 M
5.	What are the features of CRT? Explain.	2 M
6.	Define deflection sensitivity of a CRT.	2 M
7.	What is LVDT? Write its applications.	2 M
8.	List out differences between active and passive transducer.	2 M
9.	What are the applications and limitations of Wheatstone bridge?	2 M
10.	Explain any one of the method for the measurement of humidity?	2 M

PART-B
Answer the following. Each question carries TEN Marks.   5x10=50M

11.A).	What is meant by Dynamic characteristics of an instrument? Explain the following terms in detail (i) speed of response (ii) Fidelity (iii) Lag (iv) Dynamic error.	10M

OR

11. B).	List out different DC voltmeters and explain any one voltmeter in detail.	10M
12. A).	Draw the circuit diagram of Sweep generator and explain its operation in detail.	10M

OR

12. B).	What is Heterodyning and explain the use of Heterodyning in spectrum analyzer along with its circuit diagram.	10M
13. A).	Draw the circuit diagram of Sampling oscilloscope and explain its operation n detail.	10M

OR

13. B).	Explain the operation of CRO using neat diagrams.	10M
14. A).	What are the two types of anemometer available for liquid flow measurement? Explain the principle and operation of Hotwire Anemometer.	10M

OR

14. B).	What is Piezo-electric effect? Explain the operation of Piezo-electric transducer.	10M
15. A).	Draw the circuit diagram of Schering's Bridge and explain its operation.	10M

OR

15. B).	Briefly explain the working principles and measurement of i) Force ii) Temperature	10M

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CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(UGC AUTONOMOUS)
B.Tech V Semester Supplementary Examinations June/July-2025
Course Name: Antenna & Wave Propagation
(Electronics & Communication Engineering)

Date: 02.07.2025 FN   Time: 3 hours   Max.Marks: 70

(Note: Assume suitable data if necessary)
PART-A
Answer all TEN questions
Each question carries TWO marks.   10x2=20M

1.	Identify the angular field components in spherical coordinates?	2 M
2.	What is the physical meaning of Helmholtz theorem in electromagnetics?	2 M
3.	Mention the advantages of a folded dipole over a simple dipole?	2 M
4.	What is the function of the flare in a horn antenna?	2 M
5.	What is the relation between patch width and resonant frequency?	2 M
6.	Name the material typically used in non-metallic dielectric lenses?	2 M
7.	What is the phase difference between elements in an end fire array?	2 M
8.	What is meant by antenna reciprocity?	2 M
9.	State the difference between space waves and surface waves?	2 M
10.	Mention two differences between LUF and MUF?	2 M

PART-B
Answer the following. Each question carries TEN Marks.   5x10=50M

11.A). Define effective height and effective aperture of an antenna. Derive the relation between them.   10M

OR

11. B). Derive expressions for electric and magnetic fields of an oscillating electric dipole.   10M

12. A). Compare the performance characteristics of a Yagi-Uda array and a folded dipole. Highlight their respective advantages, typical applications, and input impedance behavior?   10M

OR

12. B). Derive the expression for beamwidth and directivity of a pyramidal horn antenna. Explain the factors affecting its design and performance?   10M

13. A). A rectangular patch antenna is to be designed to resonate at 2.4 GHz. Given appropriate substrate properties, calculate its length, width, and effective dielectric constant. Assume necessary data.   10M

OR

13. B). Discuss the concept of zoning in lens antennas. How do tolerances and zoning affect the performance and fabrication of non-metallic dielectric lenses?   10M

(P.T.O..)

14. A). For an end fire array with increased directivity, derive the expression for its array factor and discuss how directivity is enhanced? 10M

OR

14. B). A horn antenna is tested to determine its gain using the absolute method. Outline the test setup, required measurements, and calculation steps. Comment on the limitations of this method? 10M

15. A). Derive the expression for field strength variation in space wave propagation as a function of distance and antenna height. Highlight the effect of Earth's curvature? 10M

OR

15. B). Compare the parameters MUF, LUF, and virtual height in the context of sky wave communication. 10M

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CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(UGC AUTONOMOUS)
B.Tech V Semester Supplementary Examinations June/July-2025
Course Name: **Linear & Digital IC Applications**
(Electronics & Communication Engineering)

Date: 04.07.2025 FN   Time: 3 hours   Max.Marks: 70

(Note: Assume suitable data if necessary)
PART-A
Answer all TEN questions
Each question carries TWO marks.   **10x2=20M**

1.	List the ideal characteristics of an op-amp.	2 M
2.	Name two applications of op-amps.	2 M
3.	What is an active filter?	2 M
4.	Identify two applications of IC 555 timer.	2 M
5.	Define the Nyquist frequency.	2 M
6.	Determine the resolution of an 8-bit ADC.	2 M
7.	Examine Fan-out.	2 M
8.	Develop decoder to convert a binary code into a 7-segment decimal readout.	2 M
9.	Classify the four types of DRAM.	2 M
10.	What are the advantages and disadvantages of an asynchronous counter?	2 M

PART-B
Answer the following. Each question carries TEN Marks.   **5x10=50M**

11.A).	Explain the operation of inverting and Non-inverting amplifiers.	10M
	OR	
11. B).	Build an ideal integrator circuit with output waveforms and explain its operation.	10M
12. A).	Explain how first order low pass filter can be constructed using op-amp.	10M
	OR	
12. B).	Demonstrate the operation of a simple astable multivibrator using IC 555 timer.	10M
13. A).	Construct the block diagram of dual-slope ADC.	10M
	OR	
13. B).	Examine a binary-weighted-input Digital to Analog converter using block diagram.	10M
14. A).	Explain the operation of a CMOS NAND gate with a truth table.	10M
	OR	
14. B).	Construct the 74HC154 binary-to-decimal decoder.	10M
15. A).	i) Design a 3-bit synchronous counter using T flip flop.	7M
	ii) Distinguish between combinational and sequential circuits.	3M
	OR	
15. B).	i) Demonstrate the working principle of SRAM.	5M
	ii) Define the terms:	5M
	a) Memory address	
	b) Memory read operation	

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CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(UGC AUTONOMOUS)
B.Tech V Semester Supplementary Examinations June/July-2025
Course Name: Digital Signal Processing
(Electronics & Communication Engineering)

Date: 07.07.2025 FN	Time: 3 hours	Max.Marks: 70

(Note: Assume suitable data if necessary)

PART-A
Answer all TEN questions
Each question carries TWO marks.   10x2=20M

1. Define linear time invariant system   2 M
2. Explain stability of a system with respect to Z transforms RoC.   2 M
3. Define time shifting property of DFT.   2 M
4. Define Circular convolution.   2 M
5. Using Bilinear transformation, find H (z) from H (s) = 2 / [(S+1) (S-1)] withT = 1 sec.   2 M
6. Explain any two main difference between FIR and IIR filters.   2 M
7. List the conditions for a FIR system to have linear phase.   2 M
8. List any two properties of Chebyshev filter.   2 M
9. Define interpolation with one example   2 M
10. Define finite word-length effects   2 M

PART-B
Answer the following. Each question carries TEN Marks.   5x10=50M

11.A). Determine whether the following systems are linear, time-invariant, causal, and stable. **10M**
Justify your answers with proper reasoning and examples where applicable.

   i) $y(n) = e^{x(n)}$ ii) $y(n) = x(n) + \dfrac{1}{x(n-1)}$

OR

11. B). Find the Z-transform of the following discrete time signals: **10M**

   i) $x(n) = \{-1, 3, 6, 0, 1, 2\}$ ii) $x(n) = \left(\dfrac{1}{3}\right)^{n-1} .u(n-1)$

12. A). Find the linear convolution between the given sequences $x(n) = \{1, 2, -1\}$ and **10M** $h(n) = \{2, 1\}$.

OR

12. B). Find the 8-point DFT of $x(n) = \{1, 0, 1, 0, 1, 0, 1, 0\}$ using DIT-FFT algorithm.   **10M**

13. A). Design a Butterworth IIR low pass filter with the following specifications: pass band **10M** Ripple αp =1 dB, stop band attenuation αs =40 dB, pass band edge frequency is 2 KHz, stop band edge frequency 10 KHz.

OR

13. B). Derive the transformation function to convert a low-pass filter into a high-pass filter using **10M** Spectral Transformation.

(P.T.O..)

14. A). Differentiate between IIR and FIR filters. Discuss the various steps in designing FIR filter. 10M

OR

14. B). Design a FIR high pass filter of length 11 to approximate the ideal filter with a pass band cut off frequency at 1 KHz. Use triangular window. 10M

15. A). With neat diagram explain Interpolation and decimation. 10M

OR

15. B). Explain the concept of round-off noise in IIR digital filters and how it affects filter performance. 10M

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CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(UGC AUTONOMOUS)
B.Tech V Semester Supplementary Examinations June/July-2025
Course Name: **Digital Design Through Verilog HDL**
(Electronics & Communication Engineering)

Date: 09.07.2025 FN   Time: 3 hours   Max.Marks: 70

(Note: Assume suitable data if necessary)
PART-A
Answer all TEN questions
Each question carries TWO marks.   10x2=20M

1.	What are the functions of Programming Language Interface (PLI)?	2 M
2.	List any five common Verilog operators.	2 M
3.	What is the difference between wire, tri, and wand.	2 M
4.	What is meant by continuous assignment in Verilog?	2 M
5.	What is the syntax of a case statement in Verilog?	2 M
6.	List out any four loop constructs.	2 M
7.	Write the syntax to model a "CMOS switch" in Verilog.	2 M
8.	List out some "functions" used in switch-Level Modeling.	2 M
9.	Compare different sequential circuit descriptive models.	2 M
10.	What is a testbench in Verilog?	2 M

PART-B
Answer the following. Each question carries TEN Marks.   5x10=50M

11.A).	i) Write a simple Verilog code which includes the system functions display, monitor, and finish.	5M
	ii) Explain about synthesis procedure in Verilog.	5M
	OR	
11. B).	i) What are the four logic values in Verilog and difference between them?	5M
	ii) List out different White Space Characters along with syntax and their importance Verilog coding.	5M
12. A).	Create a Verilog module using gate-level primitives to model a 1-bit full adder.	10M
	OR	
12. B).	Write a Verilog code for edge-triggered D-Flip-flop.	10M
13. A).	Write a Verilog code to increment numbers from 0 to 127 using behavioral modelling.	10M
	OR	
13. B).	Illustrate with an example the usage of parallel blocks.	10M
14. A).	Generate a switch-level Verilog code for NOR gate.	10M
	OR	
14. B).	How many User defined primitives are available and explain about them?	10M
15. A).	List out and describe the basic memory components used in sequential design.	10M
	OR	
15. B).	Describe the steps involved in testing of combinational circuit in Verilog.	10M

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CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(UGC AUTONOMOUS)
B.Tech V Semester Supplementary Examinations June/July-2025
Course Name: Computer Organization
(Electronics & Communication Engineering)

Date: 09.07.2025 FN   Time: 3 hours   Max.Marks: 70

(Note: Assume suitable data if necessary)
PART-A
Answer all TEN questions
Each question carries TWO marks.   10x2=20M

1. What is the role of the control unit in a CPU?   2 M
2. Define addressing mode. Give one example.   2 M
3. Differentiate between fixed-point and floating-point representation.   2 M
4. What is the main advantage of using Booth's multiplication algorithm?   2 M
5. Mention any two characteristics of the 8086 architecture.   2 M
6. Name any two I/O data transfer methods.   2 M
7. Define pipelining.   2 M
8. What is cache coherency in parallel processors?   2 M
9. What is memory interleaving?   2 M
10. Mention any two cache replacement algorithms.   2 M

PART-B
Answer the following. Each question carries TEN Marks.   5x10=50M

11.A). i) Explain the basic functional blocks of a computer system with a neat block diagram.   5M
        ii) Illustrate the instruction execution cycle. What are the main steps involved in the fetch-   5M
        decode-execute cycle?

OR

11. B). i) Define Register Transfer Language (RTL). Give RTL representations for common   5M
        instruction types.
        ii) Discuss different types of CPU registers and their purpose in instruction execution.   5M

12. A). i) Explain signed number representation. Compare sign-magnitude, 1's complement, and   5M
        2's complement forms.
        ii) Explain floating-point arithmetic operations. What are the challenges involved in   5M
        floating-point addition and subtraction?

OR

12. B). Explain the working of a ripple carry adder. What are its limitations? Describe the carry   10M
        look-ahead adder. How does it improve performance over ripple carry adder?

13. A). i) Describe the role of interrupts in process state transitions. How do they influence   5M
        multitasking?
        ii) Differentiate between hardwired and micro-programmed control unit designs. What are   5M
        the advantages of each?

(P.T.O..)

13. B). Discuss the I/O device interfaces SCSI and USB. How do they differ in terms of data transfer and connectivity? 10M

14. A). What is cache coherence? Explain how it can be solved in multi processors. 10M

OR

14. B). A digital computer has a memory unit of 64K * 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of 4 words. 10M
(i) How many bits are there in the tag, index, block and word fields of the address format?
(ii) How many bits are there in each word of cache and how are they divided into function? Include a valid bit.

15. A). i) Distinguish between the virtual memory and cache memory. Write the merits and demerits of virtual memory. 5M
ii) Give a neat sketch that illustrates the components in a typical memory hierarchy. 5M

OR

15. B). Explain the three mapping procedures used in cache memory organization with suitable examples. 10M

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