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CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(UGC AUTONOMOUS)

Examination : **B.Tech V Semester Supplementary Examinations June/July-2025**
Course Name : **Microcontrollers**
Course Code : **A404309**
Branch : **Electronics & Communication Engineering**
Date & Session : **30-06-2025 FN** **Duration: 3 hours** **Max. Marks: 60**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions

Each question carries ONE mark. **10x1=10M**

1. Give the purpose of assembler directives in assembly language programming. 1 M
2. State the function of the Program Counter (PC) in 8086. 1 M
3. What is the purpose of the timer in the 8051 microcontroller. 1 M
4. Identify the role of the accumulator in the 8051. 1 M
5. Define the function of RS232 in serial communication. 1 M
6. Name a commonly used external communication interface in 8051 microcontrollers. 1 M
7. What is the role of conditional execution in ARM. 1 M
8. Classify the types of instructions available in the ARM instruction set. 1 M
9. What is the significance of low power consumption in CORTEX processors. 1 M
10. Distinguish between multi-core and single-core processors. 1 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A). Discuss the use of call instructions in subroutine handling within 8086. 10M

OR

11. B). Describe the register organization of the 8086 microprocessor. 10M

12. A). Illustrate the I/O ports of the 8051 microcontroller and explain their function. 10M

OR

12. B). List the instruction set categories of the 8051 and explain two instructions from each category. 10M

13. A). Illustrate and write a 8051 assembly program to process of interfacing a keyboard with the 8051 microcontroller. 10M

OR

13. B). Differentiate between I2C, SPI, and UART communication protocols. 10M

14. A). Define the ARM instruction set and its categories, with examples. 10M

OR

14. B). Describe the pipeline architecture in ARM and its significance. 10M

15. A). Analyze the performance characteristics of advanced ARM processors. 10M

OR

15. B). Explain the OMAP processor architecture and its main components. 10M

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Examination	:	**B.Tech V Semester Supplementary Examinations June/July-2025**
Course Name	:	**Antenna & Wave Propagation**
Course Code	:	**A404310**
Branch	:	**Electronics & Communication Engineering**
Date & Session	:	**02-07-2025 FN** **Duration: 3 hours** **Max. Marks: 60**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions

Each question carries ONE mark. **10x1=10M**

1.	Define directivity of antenna.	1 M
2.	Define the terms radiation intensity.	1 M
3.	Give the comparison between axial mode and normal mode of helical antenna.	1 M
4.	Discuss the characteristics of folded dipoles.	1 M
5.	What are the advantages of Microstrip antennas?	1 M
6.	Write a note on F/D ratio.	1 M
7.	Difference between uniform and non-uniform linear array.	1 M
8.	What is meant by pattern Multiplication?	1 M
9.	What is optical horizon?	1 M
10.	Define the term Skip Distance.	1 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A).	Explain the concept of Retarded Potentials.	10M
	OR	
11. B).	Develop an expression for the radiation resistance of a short electric dipole element.	10M
12. A).	With a neat sketch explain the operation of Yagi-Uda array.	10M
	OR	
12. B).	Explain the working of helical antenna in axial mode.	10M
13. A).	i) Explain the radiation mechanism of microstrip antenna. ii) Illustrate the different types of microstrip antennas.	7M 3M
	OR	
13. B).	Briefly explain about Flat Sheet Reflectors.	10M
14. A).	Deduce an expression for the radiation pattern of an end-fire array with N vertical dipoles.	10M
	OR	
14. B).	Briefly explain about gain measurement of an antenna.	10M
15. A).	Explain in detail about Ground wave propagation.	10M
	OR	
15. B).	i) Write the expression for field strength of ground wave propagation. ii) Write short note on a) MUF b) Virtual Height.	2M 8M

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CMR COLLEGE OF ENGINEERING & TECHNOLOGY
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Examination : **B.Tech V Semester Supplementary Examinations June/July-2025**
Course Name : **CMOS VLSI Design**
Course Code : **A404311**
Branch : **Electronics & Communication Engineering**
Date & Session : **04-07-2025 FN** **Duration: 3 hours** **Max. Marks: 60**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions

Each question carries ONE mark. **10x1=10M**

1. Define threshold voltage in a MOS transistor. 1 M
2. What is the figure of merit in CMOS circuits? 1 M
3. What is the purpose of stick diagrams in VLSI? 1 M
4. Mention two challenges of MOS scaling. 1 M
5. What is wiring capacitance? 1 M
6. Define fan-in and its impact on circuit design. 1 M
7. Name two types of memory elements in data path subsystems. 1 M
8. Differentiate between ROM and serial access memory. 1 M
9. What is a PAL? Mention one of its applications? 1 M
10. Mention one principle used in CMOS testing. 1 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A). Derive and explain the Ids-Vds relationship for an NMOS transistor. 10M

OR

11. B). Analyze the working of a CMOS inverter and explain its transfer characteristics with diagrams. 10M

12. A). Explain the VLSI design flow and discuss the function of each step. 10M

OR

12. B). Illustrate the layout design rules and draw the stick diagram for an NMOS inverter. 10M

13. A). Discuss the working and design of alternate gate circuits with examples. 10M

OR

13. B). Explain the effect of driving large capacitive loads and discuss how it impacts circuit performance. 10M

14. A). Design and explain the working of a 4-bit adder using CMOS technology. 10M

OR

14. B). Compare SRAM and DRAM with respect to structure, speed, and power consumption. 10M

15. A). Describe the working and structure of an FPGA. How is it used in VLSI design? 10M

OR

15. B). Discuss various design strategies for testing CMOS circuits and explain chip-level test techniques. 10M

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CMR COLLEGE OF ENGINEERING & TECHNOLOGY
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Examination : **B.Tech V Semester Supplementary Examinations June/July-2025**
Course Name : **IoT Architectures and Protocols**
Course Code : **A404312**
Branch : **Electronics & Communication Engineering**
Date & Session : **07-07-2025 FN** **Duration: 3 hours** **Max. Marks: 60**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions

Each question carries ONE mark. **10x1=10M**

1. List out the Features of IoT. 1 M
2. State the dynamic characteristics of IoT. 1 M
3. Mention the various IoT architectures. 1 M
4. Mention the communication protocols used for M2M local area networks. 1 M
5. What is ZigBee protocol for Internet of Things? 1 M
6. What is the application layer in IoT protocol? 1 M
7. Which protocol is used to link all the devices in IoT? 1 M
8. What is meant by TCP in IoT? 1 M
9. Mention the security features are provided by RPL. 1 M
10. What is the main advantage of using OneM2M in IoT deployments? 1 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A). Describe the various levels of IoT with an example each. 10M

OR

11. B). (i) Discuss various application areas of IoT. 5M
(ii) Discuss about the Sensors and Actuators. 5M

12. A). Explain in detail IOT Worl Forum standardized reference model Architecture. 10M

OR

12. B). (i) Explain the differences and similarities between M2M and IoT. 5M
(ii) Discuss about SDN and NFV for IoT. 5M

13. A). Describe Physical and MAC layers Topology and tabulate the protocol stacks utilizing IEEE 802.15.4. 10M

OR

13. B). Discuss the following: 10M
(i) IEEE 802.11ah
(ii) IP versions

(P.T.O.)

14. A). Describe about application layer protocols 10M
(i) CoAP
(ii) MQTT

OR

14. B). Specify functions of AMQP, HTTP and XMPP in IoT apps. 10M

15. A). Describe in detail about the architecture of ETSI M2M. 10M

OR

15. B). Describe security in the following IoT protocols. 10M
i) MAC 802.15.4.
ii) 6LoWPAN.

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Examination : **B.Tech V Semester Supplementary Examinations June/July-2025**
Course Name : **Computer Organization & Operating Systems**
Course Code : **A404401**
Branch : **Electronics & Communication Engineering**
Date & Session : **09-07-2025 FN** **Duration: 3 hours** **Max. Marks: 60**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions

Each question carries ONE mark. **10x1=10M**

1. List different functional units in computer. 1 M
2. What is the principle of STACK? 1 M
3. Define Control Memory. 1 M
4. Define Hit Ratio. 1 M
5. Name different peripheral devices used in interface. 1 M
6. In a computer system, why a PCI bus is used? 1 M
7. What do you mean by page fault? 1 M
8. What are the necessary conditions for deadlock? 1 M
9. What are the various file accessing methods? 1 M
10. List the operations on a file. 1 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A). Explain about Floating-point and fixed pint representations with an example. 10M

OR

11. B). Describe in detail about STACK organization and also Explain the method of Addressing modes. 10M

12. A). Define the following: i) Control word ii) Micro operation iii) Microinstruction iv) Micro program v) Hardwired control. 10M

OR

12. B). Define cache memory? Explain various mapping techniques in cache memory. 10M

13. A). What is the need of I/O interface module. Differentiate isolated IO and memory mapped I/O? Discuss about priority interrupts. 10M

OR

13. B). Discuss briefly about the following: 10M
i) RS232 ii) IEEE802.3

14. A). Write a short note on the following: 10M
i) Operating system functions
ii) Protection and security of OS.

(P.T.O..)

OR

14. B). Consider the following page reference string: 1, 2, 3, 4, 2, 1, 5, 6, 1, 2, 3, 7, 6, 3, 2, 1, 2, 3, 6. How many page faults would occur for the LRU, FIFO, LFU and optimal page replacement algorithms assuming five frames. 10M

15. A). Explain the different file access methods in detail. 10M

OR

15. B). Discuss File System Implementation in Operating System. 10M

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CMR COLLEGE OF ENGINEERING & TECHNOLOGY
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Examination : **B.Tech V Semester Supplementary Examinations June/July-2025**
Course Name : **Data Communications and Computer Networks**
Course Code : **A404402**
Branch : **Electronics & Communication Engineering**
Date & Session : **09-07-2025 FN** **Duration: 3 hours** **Max. Marks: 60**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions

Each question carries ONE mark. **10x1=10M**

1. What is meant by transmission medium? 1 M
2. Remember the definition of Protocol. 1 M
3. List various services provided by data link layer to network layer. 1 M
4. Mention the IEEE 802.11 frame format. 1 M
5. What is logical addressing? 1 M
6. Mention the need of routing. 1 M
7. What are the three types of events respond by GBN sender? 1 M
8. What is the need of flow control in transport layer? 1 M
9. What are the TCP services? 1 M
10. What are the two main categories of DNS messages? 1 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A). Explain ISO OSI Reference model with neat sketch. 10M

OR

11. B). Explain TCP/IP reference model with neat sketch. 10M

12. A). i. What are the various types of errors? Explain them. 5M
ii. Explain error detection using Checksum. 5M

OR

12. B). Explain in detail the operation of pure ALOHA and slotted ALOHA. 10M

13. A). i. Compare IPV4 and IPV6. 5M
ii. Discuss various types of ICMP messages. 5M

OR

13. B). Draw and explain the router architecture. 10M

14. A). What are the Services and applications of TCP? Compare TCP and UDP Protocol. 10M

OR

14. B). What is Congestion? Explain the causes and effects of congestion. 10M

15. A). Explain briefly about FTP and DNS. 10M

OR

15. B). Explain the commands and responses used in SMTP. 10M

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