H.T No: | | | | | | | | | | | **R18** | **Course Code: A30421**

CMR COLLEGE OF ENGINEERING & TECHNOLOGY

(UGC AUTONOMOUS)

B.Tech VI Semester Supplementary Examinations June-2025

Course Name: Microprocessors & Microcontrollers

(Common for EEE & ECE)

Date: 21.06.2025 AN **Time: 3 hours** **Max.Marks: 70**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions

Each question carries TWO marks. **10x2=20M**

1.	Draw the flag register of 8086 microprocessor.	2 M
2.	List out the 4 assembler directives of 8086 processor and explain any two.	2 M
3.	Write difference between ADD and ADC.	2 M
4.	List out any four logical instructions of 8086 with examples.	2 M
5.	Explain about mode 1 of 8255 PPI.	2 M
6.	Define the control words of 8251 USART.	2 M
7.	Explain the concept of addressing modes used in 8051 microcontroller.	2 M
8.	Explain the different port3 pins of 8051 microcontroller.	2 M
9.	Explain the function of DPTR in 8051.	2 M
10.	Write any two differences between microprocessor and Microcontroller.	2 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A).	With a neat sketch explain the architecture of 8086 microprocessor.	10M
	OR	
11. B).	Explain the Register Organisation of 8086 microprocessor.	10M
12. A).	Develop an ALP for 8086 to find the GCD of a given number two numbers.	10M
	OR	
12. B).	Explain the logical instructions of 8086 with suitable examples.	10M
13. A).	Describe the operation of a parallel comparator A/D converter.	10M
	OR	
13. B).	Illustrate different control word formats of 8255 PPI.	10M
14. A).	Draw the pin diagram of 8051 microcontroller and explain the function of each pin in detail.	10M
	OR	
14. B).	Write short notes on (i) PSW (ii) SCON (iii) PCON (iv) TMOD.	10M
15. A).	Explain the interrupt structure of 8051 Microcontroller.	10M
	OR	
15. B).	Explain the various modes of operation with respect to serial port in8051 microcontroller.	10M

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H.T No: | | | | | | | | | | | **R18** | **Course Code: A30419**

CMR COLLEGE OF ENGINEERING & TECHNOLOGY

(UGC AUTONOMOUS)

B.Tech VI Semester Supplementary Examinations June-2025

Course Name: Microwave Engineering

(Electronics & Communication Engineering)

Date: 24.06.2025 AN **Time: 3 hours** **Max.Marks: 70**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions

Each question carries TWO marks. **10x2=20M**

1. Define dominant and degenerate modes. 2 M
2. List the various microwave spectrum bands. 2 M
3. List the properties of S matrix. 2 M
4. Define isolator and circulator. 2 M
5. List the limitations of conventional microwave tubes. 2 M
6. Define velocity modulation. 2 M
7. Define cross field microwave tube. 2 M
8. What is the need for slow wave structures in travelling wave tubes? 2 M
9. Define Avalanche transit time device. 2 M
10. List the various components used in a microwave bench setup. 2 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A). Derive the wave equations for a TE wave and derive all the field components and parameters in a rectangular waveguide. 10M

OR

11. B). Derive the wave equation and resonant frequency of a rectangular waveguide cavity resonator. 10M

12. A). Illustrate in detail about the operation of two hole and Bethe hole direction couplers. 10M

OR

12. B). Derive the S matrix for Magic Tee junction and gyrator. 10M

13. A). i) Derive an expression for output power and efficiency in two cavity klystrons. 5M

ii) A reflex klystron operates at peak mode of n=2 with beam voltage V_o=250 V, beam current I_o=15 mA. A signal voltage V_1= 45 V is applied. Calculate input, output powers and efficiency? 5M

OR

13. B). Elaborate in detail about the theory of bunching process in reflex klystron with the help of applegate diagram. 10M

14. A). Discuss in detail about the operation of cylindrical magnetron and derive an expression for Hull cutoff Magnetic field. 10M

OR

14. B). Explain the operation of helix travelling wave tube. 10M

15. A). Analyse in detail the various methods used to measure microwave power? 10M

OR

15. B). Discuss in detail about the different modes of operation of Gunn diode? 10M

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H.T No: | | | | | | | | | | | **R18** Course Code: A30420

CMR COLLEGE OF ENGINEERING & TECHNOLOGY

(UGC AUTONOMOUS)

B.Tech VI Semester Supplementary Examinations June-2025

Course Name: VLSI Design

(Electronics & Communication Engineering)

Date: 26.06.2025 AN **Time: 3 hours** **Max.Marks: 70**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions

Each question carries TWO marks. **10x2=20M**

1. List the advantages of MOSFETS over BJTs. 2 M
2. Define the MOSFET Threshold Voltage (V_T) and mention its polarities for NMOS and PMOS transistors. 2 M
3. What are the MOS layers used in an MOSFET fabrication? 2 M
4. List three major advantages of MOSFET scaling. 2 M
5. Draw CMOS gate of And-OR-Invert (AOI) and its truth table. 2 M
6. Draw and explain the 3-input AND gate using switch logic. 2 M
7. Design 1-bit comparator with the help of basic gates. 2 M
8. Draw 1-bit DRAM cell and explain its operation. 2 M
9. What is full-custom design and what are its advantages? 2 M
10. What is static power dissipation in electronic circuits? 2 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A). i) Outline detailed CMOS inverter fabrication steps for n-well process. 7M
ii) What are the other processes available for CMOS fabrication? 3M

OR

11. B). i) What are the advantages of BiCMOS gates over CMOS gates? 3M
ii) Draw and explain basic BiCMOS inverter and suggest a way to improve the performance of basic BiCMOS inverter. 7M

12. A). Illustrate VLSI design flow from specification to GDS and Highlight the front-end and back-end design flows in the flow. 10M

OR

12. B). Draw the schematic diagram and stick diagram of CMOS inverter and List all the layers and draw its layout diagram. 10M

13. A). Explain the most important aspects of Pseudo NMOS logic circuit operation with the help of circuit diagram and its characteristics 10M

OR

13. B). State the reason for CMOS gates difficulty in driving the large capacitive loads? Propose a method to resolve this issue. 10M

(P.T.O.)

14. A). Design 4-bit Braun Array multiplier using minimum no. of simple Full Adder and logic gates. 10M

OR

14. B). i) Compare Serial Access Memories (SAM) with RAMs. 3M

ii) Explain the operation of SAM with its diagram. 7M

15. A). i) List and define various types of power consumptions in electronic circuits. 3M

ii) Discuss the parameters influencing low power designs in VLSI circuits. 7M

OR

15. B). i) Explain CPLD and FPGA architectures with suitable diagrams. 7M

ii) List the differences and applications. 3M

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H.T No: | | | | | | | | | | | **R18** **Course Code: A30444**

CMR COLLEGE OF ENGINEERING & TECHNOLOGY

(UGC AUTONOMOUS)

B.Tech VI Semester Supplementary Examinations June-2025

Course Name: Cellular & Mobile Communications

(Electronics & Communication Engineering)

Date: 28.06.2025 AN **Time: 3 hours** **Max.Marks: 70**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions

Each question carries TWO marks. **10x2=20M**

1.	What is coherence bandwidth?	2 M
2.	Define grade of service in cellular systems.	2 M
3.	What is space diversity?	2 M
4.	What is cross-talk in mobile communication?	2 M
5.	How does phase difference between direct and reflected paths affect signal quality?	2 M
6.	What are the factors affecting path loss in hilly terrain?	2 M
7.	What is channel borrowing in frequency management?	2 M
8.	What is the role of paging channels in mobile networks?	2 M
9.	What is intersystem handoff?	2 M
10.	What is forced handoff?	2 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A).	Illustrate the basic cellular structure and explain the uniqueness of the mobile radio environment.	10M
	OR	
11. B).	Compare the features of 1G, 2G, 3G, and 4G systems. What were the key advancements in each generation?	10M
12. A).	How is co-channel interference measured? Explain how antenna parameters help in its reduction.	10M
	OR	
12. B).	How do power and antenna height affect interference and coverage in cellular systems?	10M
13. A).	Discuss the effect of human-made structures and terrain on signal propagation and traffic handling.	10M
	OR	
13. B).	Summarize near and long-distance propagation. How does Lee's model help in signal prediction?	10M
14. A).	What are the different types of channel assignment strategies? Which is more efficient and why?	10M
	OR	
14. B).	How does sectorization improve frequency reuse? Explain with a diagram.	10M
15. A).	What are the different handoff strategies? Explain mobile-assisted and soft handoffs.	10M
	OR	
15. B).	Evaluate the causes of dropped calls and suggest methods to reduce dropped call rates.	10M

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H.T No: | | | | | | | | | | | **R18** Course Code: A30516

CMR COLLEGE OF ENGINEERING & TECHNOLOGY

(UGC AUTONOMOUS)

B.Tech VI Semester Supplementary Examinations June-2025

Course Name: Operating System

(Electronics & Communication Engineering)

Date: 28.06.2025 AN **Time: 3 hours** **Max.Marks: 70**

(Note: Assume suitable data if necessary)

PART-A

Answer all TEN questions

Each question carries TWO marks. **10x2=20M**

1. List the types of system software and explain how they differ from an operating system. 2 M
2. Define the following: 2 M
   i. Real-time operating system
   ii. Time-sharing system
3. Explain the producer-consumer problem. 2 M
4. Define a thread and differentiate it from a process. 2 M
5. What are the necessary conditions for a deadlock to occur? 2 M
6. Define the following: 2 M
   i. Mutex
   ii. Counting semaphores
7. What is segmentation, and how does it differ from paging? 2 M
8. Using the first-fit algorithm, allocate memory for processes of size 212K, 417K, 112K, and 426K to memory partitions of 100 KB, 500 KB, 200 KB, 300 KB, and 600 KB (in order). 2 M
9. Mention any four file access methods. 2 M
10. List the different file allocation strategies. 2 M

PART-B

Answer the following. Each question carries TEN Marks. **5x10=50M**

11.A). What is system call? Explain various types of system calls provided by Operating System. 10M

OR

11. B). What is an operating system? What are the functions of Operating System? 10M

12. A). Explain shared memory as a method of inter-process communication. 10M

OR

12. B). Consider the set of 4 processes whose burst times and priorities are given below: 10M

Process	Burst Time	Priority
P1	6	3
P2	2	1
P3	8	2
P4	4	4

Draw Gantt charts to show the execution of these processes using:
i. Priority Scheduling (non-preemptive)
ii. Round Robin (time quantum = 2 units)
Calculate the waiting time and turnaround time for each process for both algorithms.

(P.T.O..)

13. A). What is meant by Deadlock? Explain the various types of Deadlock avoidance and Prevention methods. 10M

OR

13. B). Consider the following resource-allocation system: 10M

Process	Allocation (A, B, C)	Max (A, B, C)	Available (A, B, C)
P1	(0, 1, 0)	(7, 5, 3)	(3, 3, 2)
P2	(2, 0, 0)	(3, 2, 2)	
P3	(3, 0, 2)	(9, 0, 2)	
P4	(2, 1, 1)	(4, 2, 2)	
P5	(0, 0, 2)	(5, 3, 3)	

i. Calculate the "Need" matrix.
ii. Determine if the system is in a safe state using the Banker's Algorithm.

14. A). Compare and contrast the following page replacement algorithms with examples: 10M
i. FIFO
ii. LFU

OR

14. B). Explain the concept of page fault handling in demand paging with a neat diagram. 10M

15. A). What is a file system? Explain the different layers of a file system. 10M

OR

15. B). Explain contiguous, linked, and indexed file allocation methods with examples. 10M

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