CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(UGC AUTONOMOUS)

Examination	:	B.Tech V Semester Regular & Supplementary Examinations Nov/Dec-2025
Course Name	:	Antenna & Wave Propagation
Course Code	:	A404310
Branch	:	Electronics & Communication Engineering
Date & Session	:	27-11-2025 AN Duration: 3 hours Max. Marks: 60

(Note: Assume suitable data if necessary)

PART-A
Answer all TEN questions
Each question carries ONE mark.   10x1=10M

1.	What is radiation intensity?	1 M
2.	Define effective aperture.	1 M
3.	What is meant by parasitic elements in an array?	1 M
4.	State the advantages of a horn antenna.	1 M
5.	Mention advantages of a microstrip antenna.	1 M
6.	What are the feed methods used in parabolic reflectors?	1 M
7.	What is uniform linear array?	1 M
8.	Write one difference between broadside and end-fire array.	1 M
9.	What is duct propagation?	1 M
10.	Define critical frequency.	1 M

PART-B
Answer the following. Each question carries TEN Marks.   5x10=50M

11.A).	i) Explain the radiation resistance, beamwidth, effective aperture and directivity of an antenna in detail.	8M
	ii) An antenna has a gain of 10 dB and efficiency of 80%. Find its directivity.	2M

OR

11. B).	Develop the expressions for radiation fields of a small electric dipole antenna and explain its radiation pattern.	10M

12. A).	Develop the geometry and modes of a helical antenna and explain axial and normal modes in detail.	10M

OR

12. B).	Explain about Horn antennas, types of horn antennas and Fermat's principle in their design.	10M

13. A).	Explain the design, characteristics and feed techniques of parabolic reflector antennas.	10M

OR

13. B).	Identify the limitations and feed techniques used in microstrip antennas.	10M

(P.T.O..)

14. A). i) Explain the principle of pattern multiplication and its significance in antenna arrays with example. 5M

ii) Draw the radiation pattern of 4-point isotropic antenna array with $\lambda/2$ separation. 5M

OR

14. B). i) Explain the concept of reciprocity theorem. 3M

ii) Explain gain measurement of antenna in detail. 7M

15. A). Explain super refraction, M-curves, and duct propagation in detail. 10M

OR

15. B). Explain space-wave propagation and discuss the effect of Earth's curvature. 10M

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CMR COLLEGE OF ENGINEERING & TECHNOLOGY
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Examination	:	B.Tech V Semester Regular & Supplementary Examinations Nov/Dec-2025
Course Name	:	CMOS VLSI Design
Course Code	:	A404311
Branch	:	Electronics & Communication Engineering
Date & Session	:	29-11-2025 AN

Duration: 3 hours   Max. Marks: 60

(Note: Assume suitable data if necessary)

PART-A
Answer all TEN questions
Each question carries ONE mark.   10x1=10M

1.	What does CMOS stand for, and why is it efficient?	1 M
2.	What is the effect of threshold voltage in a MOS transistor?	1 M
3.	What is the purpose of scaling in MOS circuits?	1 M
4.	Why are MOS layers necessary for fabrication?	1 M
5.	What does fan-in mean in digital circuits?	1 M
6.	What is switch logic, and where is it used?	1 M
7.	What are adders used for in data path circuits?	1 M
8.	How is ROM different from SRAM in storage type?	1 M
9.	What is an FPGA, and why is it important?	1 M
10.	Why is testing important in CMOS circuits?	1 M

PART-B
Answer the following. Each question carries TEN Marks.   5x10=50M

11.A).	Explain the electrical properties of MOS transistors and describe their threshold voltage.	10M

OR

11. B).	Analyze the working of a CMOS inverter and explain its transfer characteristics with diagrams.	10M
12. A).	What are layout design rules, and why are they important in VLSI circuits?	10M

OR

12. B).	Illustrate the layout diagram and the stick diagram for a CMOS inverter.	10M
13. A).	i) Explain the relationship between capacitance, resistance, and delay in a CMOS circuit.	3M
	ii) Explain about wiring capacitance, suggest ways to minimize it.	7M

OR

13. B).	Design an XOR gate using transmission gates and analyze the delay for a given input capacitance of 20fF. Compare it with a conventional CMOS XOR gate.	10M
14. A).	Design a 4-bit barrel shifter circuit using MOSFET and explain its working.	10M

OR

14. B).	Explain the operation of a zero/one detector circuit in CMOS technology.	10M
15. A).	Explain the structure of an FPGA and discuss its advantages over fixed logic devices for prototyping over ASIC design.	10M

OR

15. B).	Describe the principles and methods for testing CMOS circuits.	10M

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CMR COLLEGE OF ENGINEERING & TECHNOLOGY
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Examination	:	B.Tech V Semester Regular & Supplementary Examinations Nov/Dec-2025	
Course Name	:	IoT Architectures and Protocols	
Course Code	:	A404312	
Branch	:	Electronics & Communication Engineering	
Date & Session	:	02-12-2025 AN	Duration: 3 hours	Max. Marks: 60

(Note: Assume suitable data if necessary)

PART-A
Answer all TEN questions
Each question carries ONE mark. 10x1=10M

1.	List the major applications of IoT.	1 M
2.	What are the components of an IoT ecosystem?	1 M
3.	Define NFV.	1 M
4.	Draw the diagram of core IoT functional stack.	1 M
5.	Define 6LoWPAN and its importance in IoT.	1 M
6.	What are the functions of network layer in IoT?	1 M
7.	Define MPTCP.	1 M
8.	List the main characteristics of IoT protocols.	1 M
9.	What is data integrity in IoT?	1 M
10.	Why privacy is important in IoT applications.	1 M

PART-B
Answer the following. Each question carries TEN Marks. 5x10=50M

11.A).	i) Discuss the historical evolution and growth of the Internet of Things.	5M
	ii) Discuss various types of sensors and actuators used in IoT.	5M

OR

11. B).	With the help of neat diagrams, describe various types of IoT levels using examples.	10M

12. A).	i) Explain the role of value chains in IoT.	5M
	ii) Discuss about differences and similarities between IoT and M2M.	5M

OR

12. B).	i) Explain about Software Define network.	5M
	ii) Explain about IoT world forum architecture.	5M

13. A).	i) Describe the working of ZigBee and Bluetooth Low Energy protocols.	5M
	ii) Discuss about MAC layer of IEEE 802.15.4.	5M

OR

13. B).	Explain in detail about IPv4, IPv6 network layer protocols and write the pros and cons of the protocols.	10M

(P.T.O..)

14. A). What is the purpose of Transport layer protocol? Explain in detail any two transport layer   10M
protocols and write the pros and cons of the protocols.

OR

14. B). i) Differentiate between CoAP and HTTP in IoT communication.   5M
ii) Using neat diagram explain about MQTT protocol.   5M

15. A). i) Write a short note on ONE M2M.   5M
ii) Explain about Open Mobile Alliance protocol.   5M

OR

15. B). i) Discuss various security mechanisms used in IoT application layers.   5M
ii) Discuss about the security in MAC 802.15.4   5M

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CMR COLLEGE OF ENGINEERING & TECHNOLOGY
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Examination	:	B.Tech V Semester Regular & Supplementary Examinations Nov/Dec-2025
Course Name	:	Computer Organization & Operating Systems
Course Code	:	A404401
Branch	:	Electronics & Communication Engineering
Date & Session	:	04-12-2025 AN Duration: 3 hours Max. Marks: 60

(Note: Assume suitable data if necessary)

PART-A
Answer all TEN questions
Each question carries ONE mark. 10x1=10M

1. Evaluate $(-15)_{10} + (+3)_{10}$ using 2's compliment. — 1 M
2. A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers. How many selection inputs are there in each multiplexer? — 1 M
3. What is the difference between hardwired control and a micro programmed control? — 1 M
4. Demonstrate on PROM. — 1 M
5. Distinguish between an Isolated I/O and Memory-Mapped I/O. — 1 M
6. In a computer system, why a PCI bus is used? — 1 M
7. Distinguish between Distributed System and a Real-Time System. — 1 M
8. List any four Operating system services. — 1 M
9. Define mounting. What is the need for mounting in a file system? — 1 M
10. List various file allocation methods. — 1 M

PART-B
Answer the following. Each question carries TEN Marks. 5x10=50M

11.A). i) Explain Arithmetic Logic Shift Unit with neat diagram. — 5M
ii) Write arithmetic microoperations, logic microoperation and shift micro-operations. — 5M

OR

11. B). What is an Addressing mode? List and explain the various addressing modes with an example. — 10M

12. A). Explain any two cache memory mapping techniques with relevant diagrams. — 10M

OR

12. B). With a neat block diagram, explain in detail about micro programmed control unit and explain its operations. — 10M

13. A). i) Explain asynchronous data transfer modes with diagrams. — 5M
ii) With neat diagram explain direct memory access. — 5M

OR

13. B). Explain in detail about Input-Output Interface with neat diagram. — 10M

14. A). What are the necessary conditions for Deadlock? Explain Deadlock prevention and avoidance methods. — 10M

OR

14. B). (i) Explain about the implementation of the hashed page table approach. — 5M
(ii) Briefly explain about demand paging. — 5M

(P.T.O..)

15. A). Explain the following terms with neat diagrams and examples: 10M
     i) Two level directory structures.   ii) DAG structure.

<div align="center">OR</div>

15. B). i) Explain how the remote file sharing can be done in RFS. 5M
     ii) Explain file allocation methods. 5M

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CMR **CMR COLLEGE OF ENGINEERING & TECHNOLOGY**
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Examination	:	B.Tech V Semester Regular & Supplementary Examinations Nov/Dec-2025
Course Name	:	Data Communications and Computer Networks
Course Code	:	A404402
Branch	:	Electronics & Communication Engineering
Date & Session	:	04-12-2025 AN Duration: 3 hours Max. Marks: 60

(Note: Assume suitable data if necessary)
PART-A
Answer all TEN questions
Each question carries ONE mark.   **10x1=10M**

1.	What is a computer network?	1 M
2.	Define protocol.	1 M
3.	Define Point to point protocol.	1 M
4.	Define framing.	1 M
5.	What is the role of ICMP?	1 M
6.	Define Logical addressing.	1 M
7.	What is multicast routing?	1 M
8.	What is multiplexing?	1 M
9.	Define Electronic Mail.	1 M
10.	List out network applications architectures.	1 M

PART-B
Answer the following. Each question carries TEN Marks.   **5x10=50M**

11.A).	i) Describe the characteristics of layered architecture.	5M
	ii) Explain in detail about guided media & unguided media.	5M
	OR	
11. B).	With a neat diagram explain the OSI reference model in detail? Explain the functions performed in each layer.	10M
12. A).	Analyze different error control mechanisms in Data Link Control.	10M
	OR	
12. B).	Explain how bit stuffing and character stuffing are used in data link layer protocols.	10M
13. A).	Explain about IPv6? Compare IPv4and IPv6.	10M
	OR	
13. B).	Describe in detail the operation of Virtual-Circuit Approach: Connection - Oriented Service	10M
14. A).	Interpret in your own words about segment structure in TCP and UDP.	10M
	OR	
14. B).	i) Explain the concept of flow control used in TCP.	4M
	ii) Explain about TCP connection management.	6M
15. A).	Why do we need a DNS? Explain DNS in detail.	10M
	OR	
15. B).	Explain in detail about HTTP operation, Request Message and Response Message types.	10M

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CMR COLLEGE OF ENGINEERING & TECHNOLOGY
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Examination	:	B.Tech V Semester Regular & Supplementary Examinations Nov/Dec-2025
Course Name	:	Electronic Measurements and Instrumentation
Course Code	:	A404403
Branch	:	Electronics & Communication Engineering
Date & Session	:	04-12-2025 AN Duration: 3 hours Max. Marks: 60

(Note: Assume suitable data if necessary)

PART-A
Answer all TEN questions
Each question carries ONE mark.   10x1=10M

1.	Define any two static characteristics.	1 M
2.	What is dynamic error? Plot it with respect to time delay.	1 M
3.	What is meant by harmonic distortion?	1 M
4.	What is a Spectrum Analyzer?	1 M
5.	What are the different modes of operation in dual trace oscilloscope?	1 M
6.	What is the purpose of a trigger pulse in a CRO?	1 M
7.	Define Transducer? What are the various Characteristics of a Transducer?	1 M
8.	What is the basic working principle of a thermocouple?	1 M
9.	Write the limitations of wheatstone bridge?	1 M
10.	Define Data Acquisition System.	1 M

PART-B
Answer the following. Each question carries TEN Marks.   5x10=50M

11.A).	Explain the working of a basic DC voltmeter. How can its range be extended.	10M
	OR	
11. B).	i) Explain about series type ohmmeter in detail.	5M
	ii) Explain about different types of errors.	5M
12. A).	What are the applications and advantages of Arbitrary Waveform Generator? Explain.	10M
	OR	
12. B).	Distinguish between Spectrum Analyzer and Harmonic Distortion Analyzer.	10M
13. A).	Draw the block diagram of CRO and explain each bock in detail.	10M
	OR	
13. B).	Draw the block diagram of a CRT and explain individual parts clearly.	10M
14. A).	Draw the construction diagram and explain the working of LVDT.	10M
	OR	
14. B).	Explain the working principle of Piezo electric transducer in detail.	10M
15. A).	Explain briefly the working of Maxwell's bridge.	10M
	OR	
15. B).	Explain the working of Wheatstone's bridge in detail.	10M

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CMR COLLEGE OF ENGINEERING & TECHNOLOGY
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Examination	:	B.Tech V Semester Regular & Supplementary Examinations Nov/Dec-2025
Course Name	:	Microcontrollers
Course Code	:	A404309
Branch	:	Electronics & Communication Engineering
Date & Session	:	06-12-2025 AN Duration: 3 hours Max. Marks: 60

(Note: Assume suitable data if necessary)
PART-A
Answer all TEN questions
Each question carries ONE mark. 10x1=10M

1. Justify the significance of dividing the Physical memory of 8086µp into EVEN and ODD   1 M
   Address space and list the 8086 Pins involved in the operation?
2. Differentiate between Minimum mode Maximum mode operations of 8086µp.   1 M
3. Configure IE register of 8051µc to enable serial port interrupt and Timer0 interrupt.   1 M
4. List any four architectural features of 8051µc.   1 M
5. Compare I2C and SPI Protocols.   1 M
6. List the features of UART interface.   1 M
7. Write the CPSR register format of ARM Processor.   1 M
8. What is ARM Nomenclature?   1 M
9. Differentiate between RISC and CISC cores.   1 M
10. Write the salient features of ARM Cortex M5 processor.   1 M

PART-B
Answer the following. Each question carries TEN Marks.   5x10=50M

11.A). Explain the various addressing modes supported by 8086µp with suitable example of   10M
   each.

OR

11. B). i) Write a program to find the average of elements given in any array? (Assume the array   5N.
   size as five and initialize the array at address 2000h).
   ii) Explain the significance of memory segmentation in 8086µp.   5M

12. A). i) Explain the architecture of 8051µc with a neat diagram.   5M
   ii) Write a program to generate a square wave of 2khz frequency on pin P1.4 using   5M
   Timer1 in mode1 using 8051µc? (Assume xtal freq= 11.0592Mhz).

OR

12. B). i) Write a program to transfer the string "EXAM" over the serial port of 8051µc at a baud   5M
   rate of 4800? (Assume xtal freq= 11.0592Mhz).
   ii) Explain the following instructions of 8051µc with suitable example?   a) CJNE   5M
   b) DJNZ   c) MOVC   d) MOVX   e) CPL.

(P.T.O..)

13. A). i) Explain the working of SPI protocol with a neat diagram and justify how the exchange of data is done using SPI. 5M

ii) Draw the interface diagram to connect ADC 0809 with 8051μc. 5M

OR

13. B). i) Write a program to interface LCD with 8051μc to display the message "CMRCET" in 1st line and "ECE" in 2nd line. 5M

ii) Interface an 8KX8 Program ROM IC with 8051μc and explain the process. 5M

14. A). i) Differentiate between ARM mode and Thumb mode instructions of ARM. 5M

ii) Explain the 5-stage pipeline structure of ARM with a suitable example. 5M

OR

14. B). Explain any five Branch instructions supported by ARM with a suitable example of each. 10M

15. A). Explain the OMAP Processor features and its working architecture with a neat diagram. 10M

OR

15. B). Explain the ARM Cortex Processor features and its working architecture with a neat diagram. 10M

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