CMR COLLEGE OF ENGINEERING & TECHNOLOGY
(UGC Autonomous)
Kandlakoya, Medchal Road, Hyderabad – 501 401

ACADEMIC REGULATIONS - R 25

FOR CBCS & OUTCOME BASED M.TECH (REGULAR) PROGRAMMES
(Effective for the students admitted into I year from the Academic Year 2025-26)

1.0 Post-Graduate Degree Programme in Engineering & Technology (PGP in E&T)

CMR College of Engineering & Technology is an UGC Autonomous institution affiliated to Jawaharlal Nehru Technological University Hyderabad (JNTUH) offers new regulations termed as R25 regulations for two-year (Four semesters) **Master of Technology** (M.Tech.) degree programme, under Choice Based Credit System (CBCS) with effect from the academic year **2025-26.**

2.0 Eligibility for Admissions

2.1 Admission to the M.Tech. programme shall be made subject to eligibility, qualification and specializations prescribed by the University from time to time, for each specialization under each M.Tech. programme.

2.2 Admission to the post graduate programme shall be made on the basis of either the merit rank or Percentile obtained by the qualified student in the GATE Examination/ the merit rank obtained by the qualified student in an entrance test conducted by Telangana Government (PGECET) for M.Tech. programmes/ an entrance test conducted by JNTUH/ on the basis of any other exams approved by the University, subject to reservations as laid down by the Govt. from time to time.

2.3 The medium of instructions for all PG Programmes will be **ENGLISH** only.

3.0 M.Tech. Programme Structure

3.1 The M.Tech. Programs of JNTUH are of Semester pattern, consisting of **Two** academic years, each academic year having **Two** Semesters (Odd and Even Semesters).

3.2 The two-year M. Tech. program consists of **68** credits and the student has to register for all **68** credits and earn all **68** credits for the award of M. Tech. degree.

3.3 The student shall not take more than four academic years to fulfill all the academic requirements for the award of M. Tech. degree from the date of commencement of first year first semester, failing which the student shall forfeit the seat in M. Tech. programme.

3.4 **UGC/AICTE** specified definitions/descriptions are adopted appropriately for various terms and abbreviations used in these PG academic regulations, as listed below:

3.4.1 Semester Scheme

There shall be a minimum of 15 weeks of instruction, excluding the mid-term and semester-end exams. Around 15 instruction hours, 30 instruction hours and 45 hours of learning need to be followed per one credit of theory course, practical course and project/field-based learning respectively. In each semester, there shall be 'Continuous Internal Evaluation (CIE)' and 'Semester End Examination (SEE)' under Choice Based Credit System (CBCS). The curriculum/course structure suggested by AICTE is followed as a reference document.

3.4.2 Credit Courses

All courses are to be registered by the student in a semester to earn credits which shall be assigned to each course in an L: T: P: C (Lecture Periods: Tutorial Periods: Practical Periods: Credits) structure based on the following general pattern:

- One credit for one hour/week/semester for theory/lecture (L) courses or tutorials (T)
- One credit for two hours/ week/semester for laboratory/ practical (P) /Project/Mini-Project session courses.

3.4.3 Course Classification

All courses offered for the Post-Graduate M.Tech. Degree program are broadly classified as follows. The University has followed in general the guidelines issued by AICTE/UGC.

S. No.	Broad Course Classification	Course Group/ Category	Course Description
1	Core Courses (CoC)	PC- Professional Core	Includes courses related to the parent discipline/department/ branch of Engineering
		Dissertation	M. Tech. Project or PG Project or Major Project
		Mini Project with Seminar	Seminar based on core contents related to Parent Discipline/ Department/ Branch of Engineering
2	Elective Courses (EıE)	PE - Professional Electives	Includes elective courses related to the parent discipline/department/branch of Engineering
		OE - Open Electives	Elective courses which include inter-disciplinary courses or courses in an area outside the parent discipline/department/ branch of Engineering
3	Audit Courses	--	Non-Credit Audit Courses

4.0 Course Registration

4.1 A Faculty Advisor or Counselor shall be assigned to each specialization, who will advise on the Post Graduate Programme, its Course Structure and Curriculum, Choices/Options for Courses, based on his competence, progress, pre-requisites and interest.

4.2 The on-line Registration Requests for any current semester shall be completed before

the commencement of SEEs (Semester End Examinations) of the preceding semester.

4.3 A Student can apply for on-line Registration, only after obtaining the written approval from his Faculty Advisor, which should be submitted to the College Academic Section through the Head of Department (a copy of it being retained with Head of Department, Faculty Advisor and the Student).

4.4 If the Student submits ambiguous choices or multiple options or erroneous entries during on-line Registration for the Course(s) under a given/ specified Course Group/ Category as listed in the Course Structure, only the first mentioned Course in that Category will be taken into consideration.

4.5 Course Options exercised through on-line Registration are final and cannot be changed. further, alternate choices will not be considered. However, if the Course that has already been listed for Registration by the University in a Semester could not be offered due to unforeseen or unexpected reasons, then the Student will be allowed to have alternate choice either for a new Course, if it is offered, or for another existing Course (subject to availability of seats). Such alternate arrangements will be made by the Head of Department, with due notification and time-framed schedule, within the first week from the commencement of Class-work for that Semester.

5.0 Attendance Requirements

Attendance is calculated separately for each course.

5.1 Attendance in all classes (Lectures/Laboratories) is compulsory. The minimum required attendance in each theory course (***also Audit Courses***) including the attendance of mid-term examination / Laboratory etc. is 75%. Two periods of attendance for each theory course shall be considered, if the student appears for the mid-term examination of that course. ***This attendance should also be included in the attendance uploaded every fortnight in the University Website. The attendance of Audit Courses should be uploaded separately to the University.*** A student shall not be permitted to appear for the Semester End Examinations (SEE), if his attendance is less than 75%.

5.2 A student's Seminar report and presentation on Mini Project shall be eligible for evaluation, only if he ensures a minimum of 75% of his attendance in Seminar presentation classes on Mini Project during that Semester.

5.3 **Condoning of shortage of attendance** up to a maximum of 10% (considering the days of attendance in sports, games, NCC, NSS activities and Medical grounds) in each course (Theory/Lab/Mini Project with Seminar) of a semester shall be granted by the College Academic Committee on genuine reasons.

5.4 A prescribed fee per course shall be payable for condoning shortage of attendance after getting the approval of College Academic Committee for the same. The College Academic Committee shall maintain relevant documents along with the request from the student.

5.5 Shortage of Attendance below 65% in any course shall in **no case be condoned.**

5.6 A Student, whose shortage of attendance is not condoned in any course(s) (Theory/Lab/Mini Project with Seminar) in any Semester, is considered as 'Detained in that course(s), and is not eligible to write Semester End Examination(s) of such course(s), in that Semester; and he/she has to seek re- registration for those course(s) in subsequent Semesters, and attend the same as and when offered.

5.7 A student fulfills the attendance requirement in the present semester, shall not be eligible for readmission into the same class.

5.8 **a)** A student shall put in a minimum required attendance in at least three theory courses (excluding Audit course) in first Year I semester for promotion to first Year II Semester.

b) A student shall put in a minimum required attendance in at least three theory courses (excluding
Audit course**)** in first Year II semester for promotion to second Year I Semester.

6.0 Academic Requirements

The following academic requirements must be satisfied, in addition to the attendance requirements mentioned in clause no. 5. The performance of the candidate in each semester shall be evaluated course-wise, with a maximum of 100 marks per course (theory / practical), based on Continuous Internal Evaluation and Semester End Examination.

6.1 A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course, if he secures not less than:

- 40% of Marks (24 out of 60 marks) in the Semester End Examination;
- 40% of Marks in the internal examinations (16 out of 40 marks allotted for CIE); and
- A minimum of 50% of marks in the sum total of CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together; in terms of Letter Grades this implies securing **'B'** Grade or above in a course.

6.2 A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to Mini Project with seminar, if student secures not less than 50% marks (i.e. 50 out of 100 allotted marks). The student would be treated as failed, if student (i) does not submit a seminar report on Mini Project or does not make a presentation of the same before the evaluation committee as per schedule or (ii) secures less than 50% marks in Mini Project with seminar evaluation. The failed student shall reappear for the above evaluation when the notification for supplementary examination is issued.

6.3 A student shall register for all courses for total of **68** credits as specified and listed in the course structure for the chosen specialization, put in the required attendance and fulfill the academic requirements for securing **68** credits obtaining a minimum of **'B'** Grade or above in each course, and shall ***pass all the Audit Courses*** to complete the M.Tech. Programme successfully.

Note: (1) The SGPA will be computed and printed on the marks memo only if the candidate passes in all the courses offered and gets minimum B grade in all the courses.

(2) CGPA is calculated only when the candidate passes in all the courses offered in all the semesters

6.4 Letter Grades obtained in all those courses covering the above specified **68** credits alone shall be considered for the calculation of final CGPA, which will be indicated in the consolidated grade memo.

6.5 When a student is detained due to shortage of attendance in any course(s) in any semester, shall not be permitted to write the Semester End Examinations. However, he is eligible for re-registration of such course(s) in the subsequent semester(s), as and when next offered, with the academic regulations of the batch into which he is re-registered, by paying the prescribed fees per course. In all these re-registration cases, the student shall have to secure a fresh set of internal marks and Semester End Examination marks for performance evaluation in such course(s), and SGPA/CGPA calculations.

6.6 A student eligible to appear for the Semester End Examination in any course, but absent from it or failed (failing to secure 'B' Grade or above), may reappear for that course at the supplementary examination as and when conducted. In such cases, his Internal Marks assessed earlier for that course will be carried over, and added to the marks secured in the supplementary semester end examination, for the purpose of evaluating his performance in that course.

6.7 A Student who fails to earn **68** credits as per the specified course structure, and as indicated above, within **four** academic years from the date of commencement of his first year first semester, shall forfeit his seat in M. Tech. programme and his admission **shall stand cancelled.**

7.0 Evaluation - Distribution and Weightage of Marks

The performance of a student in each semester shall be evaluated course- wise (irrespective of credits assigned) for a maximum of 100 marks.

7.1 The performance of a student in every course (including practicals and Project) will be evaluated for 100 marks each, with 40 marks allotted for CIE (Continuous Internal Evaluation) and 60 marks for SEE (Semester End-Examination). The Continuous Internal Evaluation for theory courses shall be made based on the average of the marks secured in the two Mid-Term Examinations conducted, first Mid- Term examinations in the middle of the Semester and second Mid-Term examinations during the last week of instruction.

7.2 In CIE, for theory courses, during a semester, there shall be two mid-term examinations. Each Mid-Term examination consists of two parts i) **Part – A** for 05 marks, ii) **Part – B** for 25 marks with a total duration of two hours as follows:

7.2.1 Mid Term Examination for 30 marks:

a. Part - A: Objective/quiz paper for 05 marks.

b. Part - B: Descriptive paper for 25 marks.

The objective/quiz paper is set with multiple choice, fill-in the blanks, True or False and match the following type of questions for a total of 5 marks for 10 questions. The descriptive paper shall contain 5 questions with internal choice, each carrying 5 marks. The descriptive paper for first Mid-term examinations would be two questions each from first two units and one question from third unit, and similarly for the second Mid-term examinations it would be one question from third unit and two questions each from fourth and fifth units. The average of the two Mid Term Examinations shall be taken as the final marks for Mid Term Examination (for 30 marks). While the first mid-term examination shall be conducted on 50% of the syllabus, the second mid-term examination shall be conducted on the remaining 50% of the syllabus.

The remaining 10 marks of Continuous Internal Evaluation are distributed as follows:

7.2.2 Five marks for the assignment. Student shall submit two assignments and the average of 2 Assignments each for 5 marks shall be taken. The first assignment should be submitted before the conduct of the first mid-term examination, and the second assignment should be submitted before the conduct of the second mid-term examination.

7.2.3 Five marks for the Viva-Voce/PPT/Poster Presentation/Case Study on a topic in the concerned subject. This assessment shall be completed before II Mid-Term Examination. The Head of the department shall schedule these sessions in their semester plan.

- The Student, in each course, shall have to earn 40% of marks (i.e. 16 marks out of 40 marks) in CIE, 40% of marks (i.e. 24 marks out of 60) in SEE and Overall 50% of marks (i.e. 50 marks out of 100 marks) both CIE and SEE marks taking together.

The student is eligible to write Semester End Examination of the concerned course, if the student scores ≥ 40% (16 marks) of 40 Continuous Internal Examination (CIE) marks.

In case, the student appears for Semester End Examination (SEE) of the concerned course but not scored minimum 40% of CIE marks (16 marks out of 40 internal marks), his performance in that course in SEE shall stand cancelled inspite of appearing the SEE.

The details of the end semester question paper pattern are explained in the next clause:

7.3 The Semester End Examinations (SEE), for theory courses, will be conducted for 60 marks consisting of two parts viz. i) **Part- A** for 10 marks, ii) **Part - B** for 50 marks.

- Part-A is a compulsory question which consists of ten sub-questions with uniform coverage from all units carrying equal marks.
- Part-B consists of five questions (numbered from 2 to 6) carrying 10 marks each. Each of these questions is from each unit and may contain sub-questions. For each question there will be an "either" "or" choice, which means that there will be two

questions from each unit and the student should answer either of the two questions.

- The duration of Semester End Examination is three hours.

7.4 For practical courses there shall be a Continuous Internal Evaluation (CIE) during the semester for 40 marks and 60 marks for semester end examination. Out of the 40 marks for internal evaluation:

1. A write-up on day-to-day experiment in the laboratory (in terms of aim, components/procedure, expected outcome) which shall be evaluated for 10 marks
2. 10 marks for viva-voce (or) tutorial (or) case study (or) application (or) poster presentation of the course concerned.
3. Internal practical examination conducted by the laboratory teacher concerned shall be evaluated for 10 marks.
4. The remaining 10 marks are for Laboratory Project, which consists of the Design (or) Software / Hardware Model Presentation (or) App Development (or) Prototype Presentation submission which shall be evaluated after completion of laboratory course and before semester end practical examination.

   The Semester End Examination for practical courses shall be conducted with an external examiner and the laboratory course teacher. The external examiner shall be a faculty appointed from other colleges.

   In the Semester End Examination for practical courses held for 3 hours, scheme of evaluation for 60 marks is as given below:

1. 10 marks for write-up
2. 25 for conduct experiment/program
3. 15 for evaluation of results of the conducted experiment / program and
4. 10 marks for viva-voce on concerned laboratory course.

For any change of experiment, 5 marks will be deducted from the total of 60 marks. If second time change of experiment is requested; another five marks will be deducted from the 60 marks. No third change will be permitted.

The Student, in each course, shall have to earn 40% of marks (i.e. 16 marks out of 40 marks) in CIE, 40% of marks (i.e. 24 marks out of 60) in SEE and Overall 50% of marks (i.e. 50 marks out of 100 marks) both CIE and SEE marks taking together.

The student is eligible to write Semester End Examination of the concerned course, if the student scores ≥ 40% (16 marks) of 40 Continuous Internal Examination (CIE) marks.

In case, the student appears for Semester End Examination (SEE) of the concerned course but not scored minimum 40% of CIE marks (16 marks out of 40 internal marks), his performance in that course in SEE shall stand cancelled inspite of appearing the SEE.

7.5 For conducting laboratory end examinations of all PG Programmes, one internal examiner and one external examiner are to be appointed by the Principal of the College and this is to be informed to the Director of University Examinations within two weeks, before commencement of the lab end examinations. The external examiner should be selected from outside the College concerned but within the cluster. No external examiner should be appointed from any other College in the same cluster/any other cluster which is run by the same Management.

7.6 There shall be Mini Project with Seminar during I year II semester for internal evaluation of 100 marks. The Departmental Academic Committee (DAC) will review the progress of the mini project during the seminar presentations and evaluate the same for 50 marks. Mini Project Viva Voce will be evaluated by the DAC for another 50 marks before the semester end examinations. Student shall carryout the mini project in consultation with the mini project supervisor which may include critically reviewing the literature, project implementation and submit it to the department in the form of a report and shall make an oral presentation before the DAC consisting of Head of the Department, Mini Project supervisor and two other senior faculty members of the department. The student has to secure a minimum of 50% of marks in i) seminar presentation and ii) mini project viva voce, to be declared successful. If he fails to obtain the minimum marks, he has to reappear for the same as and when scheduled.

7.7 Every candidate shall be required to submit a dissertation on a topic approved by the Dissertation Review Committee.

7.8 The M.Tech. Dissertation shall be prepared in the structure prescribed by the University, adhering to the style files and formatting guidelines. To facilitate this process, each institution will organize a brief orientation session for the entire class/section at the beginning of the final semester, guiding the students on the required structure and formatting of the dissertation.

7.9 A Dissertation Review Committee (DRC) shall be constituted with the Head of the Department as Chairperson, Dissertation Supervisor and one senior faculty member of the Department offering the M.Tech. programme.

7.10 Registration of Dissertation Work: A candidate is permitted to register for the Dissertation Work after satisfying the attendance requirement in all the courses, both theory and laboratory.

7.11 After satisfying the previous clause, a candidate must present in ***Dissertation Work Review - I***, in consultation with his Dissertation Supervisor, the title, objective and plan of action of his Dissertation work to the Dissertation Review Committee (DRC) for approval ***within four weeks*** from the commencement of **Second year First Semester**. Only after obtaining the approval of the DRC can the student initiate the Dissertation work.

7.12 If a candidate wishes to change his supervisor or topic of the Dissertation, he can do so

with the approval of the DRC. However, the DRC shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of Dissertation proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

7.13 A candidate shall submit his Dissertation progress report in two stages at least with a gap of **three**
months between them.

7.14 The work on the Dissertation shall be initiated at the beginning of the II year and the duration of the Dissertation is two semesters. A candidate is permitted to submit Dissertation Thesis only after successful completion of all theory and practical courses with the approval of DRC ***not earlier than 40 weeks*** from the date of approval of the Dissertation work. For the approval of DRC, the candidate shall submit the draft copy of thesis to the Head of the Department and make an oral presentation before the DRC.

7.15 ***The Dissertation Work Review - II*** in II Year I Semester carries 100 internal marks. Evaluation should be done by the DRC for 50 marks and the Supervisor will evaluate the work for the other 50 marks. The Supervisor and DRC will examine the Problem Definition, Objectives, Scope of Work, Literature Survey in the same domain and progress of the Dissertation Work. A candidate has to secure a minimum of 50% of marks to be declared successful in Dissertation Work Review - II. If he fails to obtain the minimum required marks, he has to reappear for Dissertation Work Review - II as and when conducted.

7.16 ***The Dissertation Work Review - III*** in II Year II Sem. carries 100 internal marks. Evaluation should be done by the DRC for 50 marks and the Supervisor will evaluate it for the other 50 marks. The DRC will examine the overall progress of the Dissertation Work and decide whether or not the Dissertation is eligible for final submission. A candidate has to secure a minimum of 50% of marks to be declared successful in Dissertation Work Review - III. If he fails to obtain the required minimum marks, he has to reappear for Dissertation Work Review - III as and when conducted. For Dissertation Evaluation (Viva Voce) in II Year II Semester there are external marks of 100 and it is evaluated by the external examiner. The candidate has to secure a minimum of 50% marks in Dissertation Evaluation (Viva-Voce) examination.

7.17 Dissertation Work Reviews - II and III shall be conducted in phase I (Regular) and Phase II (Supplementary). Phase II will be conducted only for unsuccessful students in Phase I. The unsuccessful students in Dissertation Work Review - II (Phase II) shall reappear for it at the time of Dissertation Work Review - III (Phase I). These students shall reappear for Dissertation Work Review-III in the next academic year at the time of Dissertation Work Review - II only after completion of Dissertation Work Review - II, and then Dissertation Work Review - III follows. The unsuccessful students in Dissertation Work Review - III (Phase II) shall reappear for Dissertation Work Review - III in the next academic year only at the time of Dissertation Work Review -

II (Phase I).

7.18 After approval from the DRC, a soft copy of the thesis should be submitted for Anti-Plagiarism check and the plagiarism report should be submitted to the University and be included in the final thesis. The Thesis will be accepted for submission, if the similarity index is less than **30%**. If the similarity index is more than the required percentage, the student is advised to revise the thesis and re-submit the soft copy of the thesis after one month. The maximum number of re-submissions of thesis after plagiarism check is limited to ***TWO***. The candidate has to register for the Dissertation work and work for two semesters. After three attempts, the admission is liable to be cancelled.

7.19 Three copies of the Dissertation Thesis certified by the supervisor shall be submitted to the College/School/Institute.

7.20 The thesis shall be adjudicated by an external examiner selected by the University. For this, the Principal of the College/School/Institute shall submit a panel of **three** examiners from among the list of experts in the relevant specialization as submitted by the supervisor concerned and Head of the Department.

7.21 If the report of the external examiner is unsatisfactory, the candidate shall revise and resubmit the Thesis. If the report of the examiner is unsatisfactory again, the thesis shall be summarily rejected. Subsequent actions for such dissertations may be considered, only on the specific recommendations of the external examiner and /or Dissertation Review Committee. No further correspondence in this matter will be entertained, if there is no specific recommendation for resubmission.

7.22 If the report of the examiner is satisfactory, the Head of the Department shall coordinate and decide for the conduct of Dissertation Viva-Voce examination. The Dissertation Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner who adjudicated the Thesis. The candidate has to secure a minimum of 50% of marks in Dissertation Evaluation (Viva-Voce) examination.

7.23 If he fails to fulfill the requirements as specified in the above clause, he will reappear for the Dissertation Viva-Voce examination ***only after three months***. In the reappeared examination also, if he fails to fulfill the requirements, he will not be eligible for award of the degree, unless he is asked to revise and resubmit his Dissertation Work by the board within a specified time period.

7.24 The Dissertation Viva-Voce External examination marks must be submitted to the University on the same day of the examination.

7.25 For Audit courses, a student has to secure 40 marks out of 100 marks (i.e. 40% of the marks allotted) in the continuous internal evaluation for passing the course. These marks should also be uploaded along with the internal marks of other courses.

7.26 No marks or letter grades shall be allotted for Audit Courses. Only Pass/Fail shall be indicated in Grade Card.

8.0 Re-Admission/Re-Registration

8.1 Re-Admission for Discontinued Student

A student, who has discontinued the M. Tech. degree programme due to any reason whatsoever, may be considered for '**readmission**' into the same degree programme (with the same specialization) with the academic regulations of the batch into which he gets readmitted, with prior permission from the authorities concerned.

8.2 If a student is detained in a course (s) due to shortage of attendance in any semester, he may be permitted to **re-register** for the same course(s) or the student may register in an equivalent course, If the same course is not available, as suggested by the Board of Studies of that department, in the subsequent semester(s), with the academic regulations of the batch into which he seeks re-registration, with prior permission from the authorities concerned.

8.3 A candidate shall be given chance to re-register any number of courses, if the candidate failed in these courses due to securing less than 40% marks in CIE. A candidate must re-register for failed courses within four weeks of commencement of the class work, in the next academic year and secure the required minimum attendance. In the event of the student taking this chance, his Continuous Internal Evaluation (internal) marks and Semester End Examination marks obtained in the current semester only will be accepted, if he secures pass grade.

9.0 Examinations and Assessment - The Grading System

9.1 Grades will be awarded to indicate the performance of each student in each Theory Course, or Lab/Practicals, or Mini Project with Seminar, Dissertation, etc., based on the percentage of marks obtained in CIE + SEE (Continuous Internal Evaluation + Semester End Examination, both taken together), and a corresponding Letter Grade shall be given.

9.2 As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades (UGC Guidelines) and corresponding percentage of marks shall be follow

% of Marks Secured in a Course (Class Intervals)	**Letter Grade (UGC Guidelines)**	**Grade Points**
90% and above (≥ 90%, ≤ 100%)	O (Outstanding)	10
Below 90% but not less than 80% (≥80%, <90%)	A^+ (Excellent)	9
Below 80% but not less than 70% (≥70%, <80%)	A (Very Good)	8
Below 70% but not less than 60% (≥60%, <70%)	B^+ (Good)	7
Below 60% but not less than 50% (≥ 50%, <60%)	B (above Average)	6
Below 50% (< 50%)	F (FAIL)	0
Absent	**Ab**	**0**

9.3 A student obtaining **'F'** Grade in any Course is deemed to have 'failed' and is required to reappear as 'Supplementary Candidate' for the Semester End Examination (SEE), as and when conducted. In such cases, his Internal Marks (CIE Marks) in those courses will remain as obtained earlier.

9.4 If a student has not appeared for the examinations, '**Ab**' Grade will be allocated to him for any course and shall be considered 'failed' and will be required to reappear as 'Supplementary Candidate' for the Semester End Examination (SEE), as and when conducted.

9.5 A Letter Grade does not imply any specific marks percentage; it is only the range of percentage of marks.

9.6 In general, a student shall not be permitted to repeat any Course (s) only for the sake of 'Grade Improvement' or 'SGPA/ CGPA Improvement'.

9.7 A student earns Grade Point (GP) in each Course, on the basis of the Letter Grade obtained by him in that Course. The corresponding 'Credit Points' (CP) are computed by multiplying the Grade Point with Credits for that particular Course.

Credit Points (CP) = Grade Point (GP) x Credits …. For a Course

9.8 The student passes the Course only when he **gets GP ≥ 6 (B Grade or above).**

9.9 The Semester Grade Point Average (SGPA) is calculated by dividing the Sum of Credit Points secured from all Courses registered in a Semester, by the total number of credits offered in that Semester. SGPA is rounded off to two decimal places. SGPA is thus computed as

$$\textbf{SGPA} = \{ \sum_{i=1}^{N} C_i G_i \} / \{ \sum_{i=1}^{N} C_i \} \textbf{ …. For each Semester}$$

where 'i' is the Course indicator index (taking into account all Courses in a Semester), 'N' is the no. of Courses offered in the Semester (as specifically required and listed under the Course Structure of the parent Department), C_i is the no. of Credits allotted to the i^{th} Course, and G_i represents the Grade Points corresponding to the Letter Grade awarded for that i^{th} Course.

9.10 The Cumulative Grade Point Average (CGPA) is a measure of the overall cumulative performance of a student over all Semesters considered for registration. The CGPA is the ratio of the Total Credit Points secured by a student in all registered Courses in all Semesters, and the Total Number of Credits registered in all the Semesters. CGPA is rounded off to two decimal places. CGPA is thus computed from the I Year Second Semester onwards, at the end of each Semester, as per the formula

$$\textbf{CGPA} = \{ \sum_{j=1}^{M} C_j G_j \} / \{ \sum_{j=1}^{M} C_j \}$$

(ie., up to and inclusive of S Semesters, S ≥ 2),

where 'M' is the total no. of Courses (as specifically required and listed under the Course Structure of the parent Department) the Student has 'registered'. C_j is the no. of Credits allotted to the j^{th} Course, and G_j represents the Grade Points (GP) corresponding to the Letter Grade awarded for that j^{th} Course. After registration and completion of I Year I Semester however, the SGPA of that Semester itself may be taken as the CGPA, as there are no cumulative effects.

Illustration of calculation of SGPA

Course	Credits	Letter Grade	Grade points	Credit Points
Course 1	4	A	8	4*8 = 32
Course 2	4	O	10	4*10 = 40
Course 3	4	B	6	4*6 = 24
Course 4	3	B	6	3*6 = 18
Course 5	3	A+	9	3*9 = 27
Course 6	3	B	6	3*6 = 18
	21			159

SGPA = 159/21 = 7.57

Illustration of calculation of CGPA from SGPA

Semester	Credits	SGPA	Credits * SGPA
Semester I	24	7	24*7 = 168
Semester II	24	6	24*6 = 144
Semester III	24	6.5	24*6.5 = 156
Semester IV	24	6	24*6 = 144
	96		612

CGPA = 612/96 = 6.37

10.0 Award of Degree and Class

10.1 If a student who registers for all the specified Courses as listed in the Course Structure, satisfies all the Course Requirements, and passes the examinations prescribed in the entire PG Programme, and secures the required number of **68** Credits (with CGPA □6.0), shall be declared to have 'qualified' for the award of the M.Tech. Degree in the chosen Branch of Engineering/Technology with the specialization that he was admitted into.

10.2 Award of Class

After a student has earned the requirements prescribed for the completion of the programme and is eligible for the award of M.Tech. Degree, he shall be placed in one of the following three classes based on the CGPA:

Class Awarded	CGPA
First Class with Distinction	≥ 7.50
First Class	6.50≤ CGPA < 7.50
Second Class	6.00≤ CGPA < 6.50

A student with final CGPA (at the end of the **PGP) < 6.00** shall not be eligible for the Award of Degree.

11.0 Withholding of Results

If the student has not paid the dues, if any, to the University or if any case of indiscipline is pending against him, the result and degree of the student will be withheld and he will not be allowed into the next semester.

12.0 Conversion of CGPA into equivalent Percentage of Marks

The following formula shall be used for the conversion of CGPA into equivalent marks, whenever it is necessary

Percentage (%) of Marks = (Final CGPA – 0.5) x 10

13.0 Mapping with the Sustainable Development Goals

All the courses specified in the course structure of every programme are mapped with the one or more sustainable development goals.

14.0 General

14.1 **Credit**: A unit by which the course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of teaching (lecture or tutorial) or two hours of practical work/field work per week.

14.2 **Credit Point:** It is the product of grade point and number of credits for a course.

14.3 Wherever the words “he”, “him”, “his”, occur in the regulations, they shall include “she”, “her”.

14.4 The academic regulation should be read as a whole for the purpose of any interpretation.

14.5 In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the University is final.

14.6 The University may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the University.

MALPRACTICE RULES

Disciplinary Action for Malpractices/Improper Conduct in Examinations

	Nature of Malpractices/ Improper conduct	Punishment
1.(a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers, smart watches, electronic gadgets or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only. Confiscation of Cell phones, pager, palm computers, smart watches, electronic gadgets etc. and the same would be handed over only after punishment finalized by Malpractice Committee.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones, pager, palm computers, smart watches, electronic gadgets with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him. Confiscation of Cell phones, pager, palm computers, smart watches, electronic gadgets etc. and the same would be handed over only after punishment finalized by Malpractice Committee.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers, cell phones, smart watches, electronic gadgets or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations excluding Project work/ Mandatory Courses /Technical Seminar and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled. Confiscation of Cell phones, pager, palm computers, smart watches, electronic gadgets etc. and the same would be handed over only after punishment finalized by Malpractice Committee.
3.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate Who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for

		examinations of the Remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all end semester examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4.	Smuggles the answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all end semester Examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks	Cancellation of the performance in that subject
6.	Refuses to obey the orders of the Chief Superintendent/Assistant– Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the or organizes a walk out or instigates others **to** examination hall-walk out, or threatens the officer- in-charge or any person on duty in or outside the examination hall of any injury**,** to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer- in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates are also debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has

	examination hall.	already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all Semester End Examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of That semester/year. The candidate is also debarred and forfeits the seat.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	If the student belongs to the college, expulsion from the examination performance in that subject and all other subjects shall and cancellation of the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Comes in a state of inebriated/drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for other remaining examinations of the subjects of that semester/year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations excluding Project work/ Mandatory Courses /Technical Seminar of that semester/year.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the College Academic Committee for further action to award suitable punishment.	

Malpractices identified by squad or special invigilators

Punishments to the candidates as per the above guidelines.

Malpractice identified at Spot center during valuation

1) The following procedure is to be followed in the case of malpractice cases detected during valuation, scrutiny etc. at spot center. Malpractice is detected at the spot valuation. The case is to be referred to the malpractice committee. Malpractice committee will meet and discuss/question the candidate and based on the evidences, the committee will recommend suitable action on the candidate.
2) A notice is to be served to the candidate(s) involved through the Principal regarding the malpractice and seek explanations.
3) The involvement of staff who are in charge of conducting examinations, invigilators valuing examination papers and preparing / keeping records of documents relating to the examinations in such acts (inclusive of providing in correct or misleading information) that infringe upon the course of natural justice to one and all concerned at the examinations shall be viewed seriously and recommended for award of appropriate punishment after thorough enquiry.
4) Based on the explanation and recommendation of the committee action may be initiated.

Malpractice committee:

(a) Chief Superintendent	Chairman
(b) Controller of Examinations	Member
(c) Dean Academics	Member
(d) Chief Examiner of the Course/ Subject Expert	Member
(e) Concerned Head of the Department	Member
(f) Observer	Member

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DEPARTMENT OF
ELECTRONICS & COMMUNICATION ENGINEERING

COURSE STRUCTURE FOR M. TECH (EMBEDDED SYSTEMS)
EFFECTIVE FROM ACEDEMIC YEAR 2025-26

I – SEMESTER

S.NO	Code	Group	Course Title	L	T	P	Credits
1	B555301	Core- I	FPGA Based System Design	3	0	0	3
2	B555302	Core- II	Embedded System Design	3	0	0	3
3	B555401 B555402 B555403	PE- I	1. CMOS VLSI Design 2. Wireless Sensor Networks 3. Advanced Computer Architecture	3	0	0	3
4	B555404 B555405 B555406	PE- II	1. Machine Learning and Deep Learning 2. Advanced RISC Architectures 3. Automotive Embedded Systems	3	0	0	3
5	B555501	Lab – I	FPGA Based System Design Laboratory	0	0	4	2
6	B555502	Lab – II	Embedded System Design Laboratory	0	0	4	2
7	B520303		Research Methodology & IPR	2	0	0	2
8		VAC	Audit Course – I	2	0	0	0
			Total	**16**	**0**	**8**	**18**

II – SEMESTER

S.NO	Code	Group	Course Title	L	T	P	Credits
1	B555303	Core- III	Embedded Real Time Operating Systems	3	0	0	3
2	B555304	Core- IV	IoT System Design	3	0	0	3
3	B555407 B555408 B555409	PE- III	1. GPU Architectures 2. VLSI Test and Testability 3. Hardware Software Co-Design	3	0	0	3
4	B555410 B555411 B555412	PE- IV	1. Hardware Security in VLSI Design 2. Hardware Accelerators for Machine Learning Models 3. Image and Video Processing	3	0	0	3
5	B555503	Lab – III	Embedded Real Time Operating System Laboratory	0	0	4	2
6	B555504	Lab - IV	IoT System Design Laboratory	0	0	4	2
7	B555801		Mini Project with Seminar	0	0	4	2
8		VAC	Audit Course – II	2	0	0	0
			Total	**14**	**0**	**12**	**18**

III – SEMESTER

S.NO	Code	Group	Course Title	L	T	P	Credits
1	B555413 B555414 B555415	PE- V	1. Machine Learning for Robotics 2. Edge Computing 3. Embedded Biomedical Applications	3	0	0	3
2		Open Elective	Open Elective	3	0	0	3
3	B555802	Dissertation	Dissertation Work Review – II	0	0	12	6
			Total	**6**	**0**	**12**	**12**

IV - SEMESTER

S.NO	Code	Group	Course Title	L	T	P	Credits
1	B555803	Dissertation	Dissertation Work Review - III	0	0	12	06
2	B555804	Dissertation	Dissertation Viva-Voce	0	0	28	14
			Total	**0**	**0**	**40**	**20**

Audit Course I & II:

S.NO	Code		Course Title	L	T	P	Credits
1	B500701	Audit Course	English for Research Paper Writing	2	0	0	0
2	B500702		Disaster Management				
3	B500703		Value Education				
4	B500704		Constitution of India				

Open Electives:

S.NO	Code	Course Title
1	B555601	Embedded Systems
2	B543601	Photovoltaic Systems
3	B520601	Green Building Technology
4	B558601	Intrusion Detection System

(B555301) FPGA BASED SYSTEM DESIGN

M.Tech (ES)-I Semester	L	T	P	C
	3	0	0	3

UNIT-I

Introduction to FPGA-Based Systems: Introduction, basic concepts, digital design and FPGAs, FPGA-based system design, FPGA architectures, SRAM-based FPGAs, permanently programmed FPGAs, chip I/O, circuit design of FPGA fabrics, architecture of FPGA fabrics.

UNIT II

Combinational Logic Design in FPGAs: Introduction, the logic design process, hardware description languages - modeling with HDLs, Verilog, Combinational network delay, power and energy optimization, arithmetic logic, logic implementation for FPGAs, physical design for FPGAs, the logic design process revisited.

UNIT III

Sequential Logic and State Machines: Introduction, the sequential machine design process, sequential design styles, rules for clocking, performance analysis, power optimization.

UNIT IV

Design Methodologies and Behavioral Architecture: Introduction, behavioral design, design methodologies, design example.

UNIT V

System-Level Design and Advanced FPGA Applications: Introduction, buses, platform FPGAs, multi-FPGA systems, Novel architectures.

TEXT BOOKS

1. Wolf, Wayne. FPGA-Based System Design. Pearson Education India, 2005.

REFERENCE BOOKS

1. Maxfield, Clive. The Design Warrior's Guide to FPGAs: Devices, Tools and Flows. Newnes, 1st ed., 2004.
2. Trimberger, Stephen M. Field-Programmable Gate Array Technology. Springer Science & Business Media, 2012.
3. Kuon, Ian, Russell Tessier, and Jonathan Rose. FPGA Architecture: Survey and Challenges. Now Publishers Inc., 2007.

COURSE OUTCOMES:

After the Completion of the course, the students will be able to

1. Explain the architectural features and functional components of FPGA-based systems and describe their advantages in digital design applications.
2. Design combinational logic circuits using Verilog HDL and evaluate them for delay, power, and resource utilization on FPGA platforms.
3. Develop and simulate sequential logic circuits and finite state machines using appropriate design styles and clocking rules.
4. Apply behavioural design methodologies and demonstrate system modeling using HDLs in real- world case studies.
5. Analyze and propose solutions for large-scale FPGA-based systems involving busses, platform FPGAs, and multi-FPGA architectures.

(B555302) EMBEDDED SYSTEM DESIGN

M.Tech (ES)-I Semester	L	T	P	C
	3	0	0	3

UNIT I

Introduction to Embedded Systems: Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT II

Typical Embedded System: Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: On board and External Communication Interfaces.

UNIT III

Embedded Firmware: Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT IV

RTOS Based Embedded System Design: Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT V

Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS:

1. Introduction to Embedded Systems-Shibu K.V,McGraw Hill.

REFERENCE BOOKS:

1. Embedded Systems-Raj Kamal, TMH.
2. Embedded System Design-Frank Vahid, Tony Givargis, John Wiley.
3. Embedded Systems–Lyla,Pearson,2013
4. An Embedded Software Primer-David E. Simon, Education.

Course Outcomes:

After the Completion of the course, the students will be able to

1. Understand the Characteristics of Embedded systems
2. Differentiate the design requirements between General Purpose and Embedded Systems.
3. Acquire the knowledge of firmware design principles.
4. Understand the role of Real-time Operating System in Embedded Design
5. Acquire the knowledge and experience of task level Communication in any Embedded System

(B555401) CMOS VLSI DESIGN
(PROFESSIONAL ELECTIVE – I)

M.Tech (ES)-I Semester	L	T	P	C
	3	0	0	3

UNIT - I

MOS Design

Pseudo NMOS logic- Inverter, Inverter threshold voltage, output high voltage, Output low voltage, gain at gate threshold voltage, transient response, rise time, fall time, pseudo NMOS logic gates, transistor equivalency, CMOS inverter logic.

UNIT - II

Combinational MOS logic circuits

MOS logic circuits with NMOS loads, Primitive CMOS logic gates- NOR and NAND gates, Complex logic circuits design- realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full-adder, CMOS transmission gates, designing with transmission gates.

UNIT - III

Sequential MOS logic circuits

Behavior of bistable elements, SR Latch, Clocked Latch and Flip-flop circuits, CMOS D Latch and edge triggered flip-flop.

UNIT - IV

Dynamic Logic Circuits

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, high performance dynamic CMOS circuits.

UNIT - V

Semiconductor Memories

Types, RAM array Organization, DRAM- types, operation, leakage currents in DRAM cell and refresh operation, SRAM - operation, leakage currents in SRAM cells, Flash memory-NOR flash and NAND flash.

TEXT BOOKS:

1. Digital Integrated Circuit Design- Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuit Analysis and Design – Sung Mo Kang, YusufLeblebici,TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective- Ming Bo Lin,CRC Press, 2011.
2. Digital Integrated Circuits: A Designs Perspective -Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

Course Outcomes:

After the Completion of the course, the students will be able to

1. Apply Pseudo NMOS logic to design various circuits.
2. Design of combinational MOS logic and sequential MOS logic circuits
3. Carryout the design of different circuits based on dynamic logic
4. Use CMOS transmission gates in various applications
5. Design of different Memories using MOS transistors

(B555402) WIRELESS SENSOR NETWORKS
(PROFESSIONAL ELECTIVE – I)

M.Tech (ES)-I Semester	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

UNIT -I:
Introduction to Sensor Networks, unique constraints and challenges, Advantage of Sensor Networks, Applications of Sensor Networks, Types of wireless sensor networks

UNIT –II
Mobile Ad-hoc Networks (MANETs) and Wireless Sensor Networks, Enabling technologies for Wireless Sensor Networks. Issues and challenges in wireless sensor networks

UNIT –III
Routing protocols, MAC protocols: Classification of MAC Protocols, S-MAC Protocol, B-MAC protocol,IEEE 802.15.4 standard and ZigBee

UNIT -IV
Dissemination protocol for large sensor network. Data dissemination, data gathering, and data fusion; Quality of a sensor network; Real-time traffic support and security protocols.

UNIT -V
Design Principles for WSNs, Gateway Concepts Need for gateway, WSN to Internet Communication, and Internet to WSN Communication. Single-node architecture, Hardware components & design constraints, Operating systems and execution environments, introduction to TinyOS and nesC.

TEXT BOOKS:
1. Ad-Hoc Wireless Sensor Networks- C. Siva Ram Murthy,B. S. Manoj, Pearson
2. Principles of Wireless Networks – Kaveh Pah Laven and P. Krishna Murthy, 2002, PE

REFERENCE BOOKS:
1. Wireless Digital Communications – Kamilo Feher, 1999, PHI.
2. Wireless Communications-Andrea Goldsmith, 2005 Cambridge University Press.
3. Mobile Cellular Communication – Gottapu Sasibhushana Rao, Pearson Education, 2012.
4. Wireless Communication and Networking – William Stallings, 2003, PHI.

Course Outcomes:

After the Completion of the course, the students will be able to

1. Analyze and compare various architectures of Wireless Sensor Networks
2. Interpret Design issues and challenges in wireless sensor networks
3. Classify various routing protocols and MAC Protocols
4. Analyze and compare various data gathering and data dissemination methods.
5. "Identify design principals, node architectures, hardware and software required for
6. implementation of wireless sensor networks."

(B555403) ADVANCED COMPUTER ARCHITECTURE
(PROFESSIONAL ELECTIVE- I)

M.Tech (ES)-I Semester	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

UNIT - I

Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law. Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, operations in the instruction set.

UNIT - II

Pipelines: Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT - III

Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.

ILP Software Approach: Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT - IV

Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT - V

Inter Connection and Networks: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture: Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls

TEXT BOOK:

1. John L. Hennessy, David A. Patterson, "Computer Architecture: A Quantitative Approach", 3rdEdition, Elsevier.

REFERENCE BOOKS:

1. John P. Shen and Miikko H. Lipasti, "Modern Processor Design: Fundamentals of Super Scalar Processors", 2002, Beta Edition, McGraw-Hill
2. Kai Hwang, Faye A.Brigs., "Computer Architecture and Parallel Processing", Mc Graw Hill.
3. DezsoSima, Terence Fountain, Peter Kacsuk, "Advanced Computer Architecture - A DesignSpace Approach", Pearson Education.

Course Outcomes:

After the Completion of the course, the students will be able to

1. Illustrate advanced computer architecture aspects.
2. Describe and explain instruction level parallelism with static scheduling and handling of cache memory.
3. Design basic hardware and Software at compiler level.
4. Explain and handle the multi processors and multi thread level parallelism through the distributed shared memory architecture.
5. Describe the networking in modern CPUs and design clusters.

(B555404) MACHINE LEARNING AND DEEP LEARNING
(PROFESSIONAL ELECTIVE- II)

M.Tech (ES)-I Semester	L	T	P	C
	3	0	0	3

UNIT-I

Machine Learning Basics: Learning algorithms, Capacity, over fitting and under fitting, estimators, bias and variance, maximum likelihood estimation, Bayesian statistics, Supervised and unsupervised learning algorithms, building a machine learning algorithm, challenges motivating deep learning.

UNIT-II

Deep Feed forward Networks: Gradient-based learning, hidden units, architecture design, back- propagation and other differentiation algorithms.

UNIT-III

Regularization for Deep Learning: Norm penalties, Dataset augmentation, multi-task learning, early stopping, sparse representations, ensemble methods, dropout.

Optimization: Optimization for Training Deep Models, challenges in neural network optimization, basic algorithms, parameter initialization strategies, algorithms with adaptive learning rates.

UNIT-IV

Convolutional Neural Networks: The convolution operation, motivation, pooling, convolution and pooling as an infinitely strong prior, variants of the basic convolution function, structures outputs, data types, efficient convolution algorithms, random or unsupervised features.

Sequence Modeling:

Recurrent and Recursive Nets, Recurrent Neural Networks, Recursive Neural Networks, Long Short- Term Memory, optimization for long-term dependencies.

UNIT V

Practical Methodology: Performance metrics, selecting hyper parameters, debugging strategies.

Applications: Large-scale deep learning, computer vision, speech recognition, natural language processing, other applications.

TEXT BOOKS:

1. Good fellow, Ian, Yoshua Bengio, and Aaron Courville. Deep Learning. MIT Press, 2016.

REFERENCE BOOKS:

1. Géron, Aurélien. Hands-On Machine Learning with Scikit-Learn, Keras, and TensorFlow. 2nd ed., O'Reilly Media, 2019.
2. Bishop, Christopher M. Pattern Recognition and Machine Learning. Springer, 2006.
3. Chollet, François. Deep Learning with Python. 2nd ed., Manning Publications, 2021.

COURSE OUTCOMES:

After the Completion of the course, the students will be able to

1. Analyse machine learning algorithms and evaluate model performance using concepts like over fitting, bias-variance, and likelihood-based estimation.
2. Design deep feed forward neural networks using appropriate architectures, activation functions, and back propagation techniques.
3. Apply regularization and optimization techniques to improve generalization and training efficiency of deep neural networks.
4. Implement convolutional and recurrent neural network models for processing spatial and sequential data.
5. Evaluate model performance and deployment strategies in real-world applications such as computer vision, NLP, and speech recognition.
6.

(B555405) ADVANCED RISC ARCHITECTURES
(PROFESSIONAL ELECTIVE- II)

M.Tech (ES)-I Semester	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

UNIT I:
Fundamental techniques of computer design: RISC and CISC architectures – Computer arithmetic – Comparison of RISC and CISC architectures. Verilog: Introduction and review of basic designs using Verilog. MIPS processor: Introduction to MIPS features – MIPS instruction set – Logical design of MIPS data path – Control unit and instruction decoder.

UNIT II:
Processor Pipelining: Basics of Pipelining, Classic five stage pipelining in RISC processor, Performance issues in pipelining, Pipeline Hazards (Structural hazards, Data Hazards, Control Hazards), Data forwarding and bypassing techniques, Branch prediction technique: Static and Dynamic branch prediction.

UNIT III:
Memory hierarchy: Memory hierarchy, Locality of References, Cache memory principles, Types of caches (Virtual and Physical cache), Cache architecture, Direct mapped, set associative and fully associative caches, Block Replacement Techniques and Write Strategy, Design Concepts in Cache Memory. Basic and Advanced Optimization Techniques in Cache Memory.

UNIT IV:
RISC-V Architecture: RISC-V Instruction Set Architecture, Registers – General Purpose Registers, Control and Status Registers, Operating Modes, Programmers' Model for Base Integer ISA, Base Instruction Formats, Exceptions, Traps, and Interrupts, Machine-Level CSRs misa, mhartid, mstatus, mtvecmedeleg and mideleg, mip and mie, mepc, mcause, mtval.

UNIT V:
VEGA THEJAS32 Microcontroller: Functional Bock diagram, CPU, Memory Mapped input output and Interrupts Project using ARIES Development board.

TEXT BOOKS:

1. Computer Architecture, A quantitative approach by John L Hennessy and David A Patterson Fifth Edition.
2. Computer organization and architecture, designing for performance, William Stallings Eight Edition.

REFERENCE BOOKS:

1. Georg Hager, Gerhard Wellein, Introduction to High Performance Computing for Scientists and Engineers, Chapman & Hall / CRC Computational Science series,2011.
2. The RISC-V Reader by David A Patterson and Andrew Waterman First Edition.
3. The RISC-V Instruction Set Manual Volume I: User-Level ISA Version 2.1

COURSE OUTCOMES:

After the Completion of the course, the students will be able to

1. Apply the Instruction pipeline concept in IC design
2. Analyze the Hazards and Performance issues in Pipelining
3. Evaluate the Optimization techniques in Cache memory
4. Create IC designs using RISC-V Instruction set Architecture
5. Create an application using VEGA THEJAS32 Microcontroller

(B555406) AUTOMOTIVE EMBEDDED SYSTEMS
(PROFESSIONAL ELECTIVE- II)

M.Tech (ES)-I Semester	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

UNIT I

Vehicle Functional Domains and Their Requirements: General Context, Functional Domains: Power Train Domain, Chassis, Domain, Body Domain, Multimedia, Telematic, and HMI, Active/Passive Safety, Diagnostic. Standardized Components, Models, and Processes: In-Vehicle Networks and Protocols, Operating Systems, Middleware, Architecture Description Languages for Automotive Applications. Certification Issue of Safety-Critical In-Vehicle Embedded Systems.

Application of the AUTOSAR Standard: Motivation: Shortcomings in Former Software Structures, Setting up AUTOSAR, Main Objectives of AUTOSAR, Working Methods in AUTOSAR. Mainstay of AUTOSAR-AUTOSAR Architecture: AUTOSAR Concept, Layered Software Architecture. Main Areas of AUTOSAR Standardization: BSW and RTE: BSW, BSW Conformance Classes, RTE. Main Areas of AUTOSAR Standardization-Methodology and Templates: Objectives of the Methodology, Description of the Methodology, AUTOSAR Models, Templates, and Exchange Formats, System Configuration, ECU Configuration, Implementation to Existing Development Processes and Tooling. AUTOSAR in Practice-Conformance Testing. AUTOSAR in Practice-Migration to AUTOSAR ECU. AUTOSAR in Practice-Application of OEM– Supplier Collaboration. AUTOSAR in Practice: Demonstration of AUTOSAR-Compliant ECUs: Description of the Demonstrator, Concepts Shown by the Demonstrator.

UNIT II

Intelligent Vehicle Technologies: Introduction: Road Transport and Its Evolution: Such a Wonderful Product, Safety Problems, Congestion Problem, Energy and Emissions. New Technologies: Sensor Technologies, Sensor Fusion, Wireless Network Technologies, Intelligent Control Applications, Latest Driving Assistance. Dependability Issues: Introduction, Fail-Safe Automotive Transportation Systems, Intelligent Autodiagnostic. Fully Autonomous Car-Dream or Reality?: Automated Road Vehicles, Automated Road Network, Automated Road Management, Deployment Paths.

Embedded Automotive Protocols: Automotive Communication Systems-Characteristics and Constraints: From Point-to-Point to Multiplexed Communications, Car Domains and Their Evolution, Different Networks for Different Requirements, Event-Triggered versus Time-Triggered. In-Car Embedded Networks: Priority Buses, TT Networks, Low-Cost Automotive Networks, Multimedia Networks. Middleware Layer: Rationale for a Middleware, Automotive MWs Prior to AUTOSAR, AUTOSAR. Open Issues for Automotive Communication Systems: Optimized Networking Architectures, System Engineering.

UNIT III

FlexRay Protocol: Introduction: Event-Driven versus Time-Driven Communication, Objectives of FlexRay, History of FlexRay. FlexRay Communication: Frame Format, Communication Cycle, Static Segment, Dynamic Segment. FlexRay Protocol: Protocol Architecture, Protocol Wakeup and Startup, Wakeup, Clock Synchronization, Fault-Tolerance Mechanisms. FlexRay Application: FlexRay Implementation, FlexRay Tool Support. Impact on Development, Verification of FlexRay.

Dependable Automotive CAN Networks: Introduction: Main Requirements of Automotive Networking, Networking Technologies, CAN Features and Limitations. Data Consistency Issues: Management of Transient Channel Faults in CAN, Impairments to Data Consistency, On the Probability of the Data Inconsistency Scenarios, Solutions to Really Achieve Data, Consistency over CAN. CANcentrate and ReCANcentrate-Star Topologies for CAN: Rationale, CANcentrate and ReCANcentrate Basics, Other Considerations. CANEL: Clock Synchronization, Data Consistency, Error Containment, Support for Fault Tolerance, CANELy Limitations. FTT-CAN-Flexible Time- Triggered Communication on CAN: FTT System Architecture, Dual-Phase Elementary Cycle, SRDB, Main Temporal Parameters within the EC, Fault-Tolerance Features, Accessing the Communication Services. FlexCAN-A Deterministic, Flexible, and Dependable Architecture for Automotive Networks: Control System Transactions, FlexCAN Architecture, How FlexCAN Addresses CAN Limitations, FlexCAN Applications and Summary. Other Approaches to Dependability in CAN: TTCAN, Fault-Tolerant Time-Triggered Communication Using CAN, TCAN, ServerCAN, Fault-Tolerant Clock Synchronization Over CAN.

UNIT IV

Product Lines in Automotive Electronics: Characteristics of Automotive Product Lines: Basic Concepts of Software Product Lines, Characteristics and Needs of Automotive Electronics with Respect to Product-Line Engineering. Basic Terminolog: Software Product Lines, Variability, Feature Modeling as a Form of Variability Modeling, Discussion-Feature Modeling for the Automotive Domain. Global Coordination of Automotive Product-Line Variability: Coordination of Small- to Medium-Sized Product Lines, Coordination of Highly Complex Product Lines. Artifact- Level Variability: Basic Approach, Difficulties Related to Artifact-Local Variability, Representing Variability in ECU, Requirements Specifications, Evaluation of Representations, Mapping Representations to a Common Basis.

Reuse of Software in Automotive Electronics: Reuse of Software-A Challenge for Automotive OEMs. Requirements for the Reuse of Software in the Automotive Domain. Supporting the Reuse of Application Software Components in Cars: Processes, Development of Modularized Automotive Software Components, Function Repository, Development of an In-Vehicle Embedded System. Application Example.

UNIT V

Automotive Architecture Description Languages: Introduction. Engineering Information Challenges: Reducing Cost and Lead Time, Development Organization and Information Exchange, Product Complexity, Quality and Safety, Concurrent Engineering, Reuse and Product Line Architectures, Analysis and Synthesis, Prototyping. State of Practice: Model-Based Design, Tools, Problems beyond Model-Based Design. ADL as a Solution: General Aspects on an Automotive ADL, What Needs to Be Modeled. Existing ADL Approaches: Forsoft Automotive, SysML, Architecture and Analysis Description Language, Modeling and Analysis of Real-Time and Embedded Systems, AUTOSAR Modeling, EAST-ADL.

Model-Based Development of Automotive Embedded Systems:

Introduction: What Is MBD? Motivating MBD for Automotive Embedded Systems: Role of MBD in Automotive Embedded Systems Development, MBD Means, Driving Factors for MBD, Potential Benefits of MBD Approaches. Context, Concerns, and Requirements: Contextual Requirements on MBD, Product Concerns Addressed by MBD Efforts. MBD Technology: Modeling Languages: Abstractions, Relations, and Behavior, Analysis Techniques, Synthesis Techniques, Tools. State of the Art and Practice: Automotive State of Practices, Research and Related Standardization Efforts. Guidelines for Adopting MBD in Industry: Strategic Issues, Adopting MBD: Process and Organizational Considerations, Desired Properties of MBD Technologies, Common Arguments against MBD and Pitfalls.

TEXT BOOKS:

1. N. Navet and F. Simonot-Lion, Eds., Automotive Embedded Systems Handbook. Boca Raton, FL, USA: CRC Press, 2008.
2. William B Ribbens, Understanding Automotive Electronics: An Engineering Perspective, Seventh Edition, Elsevier, 2012.
3. Feiler, P. H., Gluch, D. P., & Hudak, J. J. (2012). Model-Based Engineering with AADL: An Introduction to the SAE Architecture Analysis & Design Language. Addison-Wesley/SAE International.

REFERENCE BOOKS:

1. Ola Larses, Architecting and Modeling Automotive Embedded Systems, KTH, 2005
2. AUTOSAR. (2025). Standards of AUTOSAR. Retrieved from https://www.autosar.org/standards
3. Vlacic, L., Parent, M., &Harashima, F. (2001). Intelligent Vehicle Technologies: Theory and Applications. Elsevier Science.

COURSE OUTCOMES:

After the Completion of the course, the students will be able to

1. Understand and analyze the structure, requirements, and standardized architecture of in-vehicle embedded systems including AUTOSAR.
2. Explain the role of intelligent technologies and communication protocols in modern vehicles.
3. Explain and Analyze FlexRay and CAN protocols.
4. Apply principles of software product-line engineering and variability modeling.
5. Demonstrate an understanding of automotive architecture description languages and model- based development techniques.

(B555501) FPGA BASED SYSTEM DESIGN LABORATORY

M.Tech (ES)-I Semester	L	T	P	C
	0	0	4	2

List of Experiments (Any 12 Experiments)

1. **LED Blinking Using Verilog:** Implement a basic LED blink circuit to understand FPGA programming and output pin control.
2. **Design and Simulation of Basic Logic Gates using Verilog HDL:** To write HDL code for basic logic gates (AND, OR, NOT, XOR), simulate their functionality, and verify the outputs using a waveform viewer.
3. **Implementation of 4-bit Adder/Subtractor on FPGA:** To design and implement a 4-bit adder/subtractor using Verilog, simulate and verify functionality on an FPGA development board.
4. **Design of a 4x1 Multiplexer and 1x4 Demultiplexer:** To write and simulate Verilog code for a 4x1 MUX and 1x4 DEMUX and validate outputs through FPGA implementation.
5. **Comparator Design (2-bit or 4-bit):** Design a simple digital comparator circuit that compares two binary inputs.
6. **Design and Implementation of a 4-bit Synchronous Counter:** To implement a 4-bit up/down synchronous counter using HDL, simulate for timing and logic correctness, and deploy it on FPGA hardware.
7. **Finite State Machine (FSM) Design:** Sequence Detector-To design a Moore or Mealy FSM for sequence detection, simulate the state transitions, and implement the design on an FPGA board.
8. **Design and Implementation of an ALU Supporting Basic Operations:** To design an Arithmetic Logic Unit that performs basic arithmetic and logic functions (ADD, SUB, AND, OR, NOT) and test it on FPGA.
9. **Interfacing Seven Segment Display with FPGA:** To write HDL code to drive a seven-segment display with binary or BCD inputs and implement the interface on FPGA hardware.
10. **Shift Register (Left/Right):** Design a shift register that shifts input bits left or right on each clock pulse.
11. **Implementation of Traffic Light Controller using FSM on FPGA:** To design a traffic light controller using finite state machines, simulate its time sequence, and implement it on FPGA hardware.
12. **PWM Signal Generation using FPGA:** To implement a pulse-width modulation (PWM) generator using Verilog HDL and demonstrate its use in applications like LED brightness control.
13. **Real-Time Clock Design and Display using FPGA:** To implement a real-time clock on FPGA with hour-minute-second display and use multiplexed seven-segment display for output.
14. **Serial Input with UART Receiver (Basic):** Implement a simple UART receiver to receive serial data and blink an LED.
15. **Implementing Digital Filters (FIR/IIR) on FPGA:** To implement a basic Finite Impulse Response (FIR) or Infinite Impulse Response (IIR) filter in HDL and simulate its output for given inputs.

COURSE OUTCOMES:

After the Completion of the course, the students will be able to

1. Write and simulate HDL code for basic combinational and sequential digital circuits using Verilog HDL.
2. Design and implement complex digital systems such as FSMs, arithmetic logic units, and communication modules on FPGA platforms.
3. Develop and verify interfacing protocols for external hardware devices like seven-segment displays, keypads, and UART communication.
4. Apply design methodologies for timing, synchronization, and resource optimization in FPGA- based digital system design.
5. Demonstrate the ability to deploy and debug digital designs on FPGA development boards, validating functionality through hardware testing

(B555502) EMBEDDED SYSTEM DESIGN LABORATORY

M.Tech (ES)-I Semester	L	T	P	C
	0	0	4	2

List of Experiments:

1. **Functional Testing Of Devices:** Flashing the OS on to the device into a stable functional stateby porting desktop environment with necessary packages.
2. **Exporting Display On To Other Systems:** Making use of available laptop/desktop displays as a display for the device using SSH client & X11 display server.
3. **GPIO Programming:** Programming of available GPIO pins of the corresponding device using native programming language. Interfacing of I/O devices like LED/Switch etc., and testing the functionality.
4. **Interfacing Chronos eZ430:** Chronos device is a programmable texas instruments watch which can be used for multiple purposes like PPT control, Mouse operations etc., Exploit the features of the device by interfacing with devices.
5. **ON/OFF Control Based On Light Intensity:** Using the light sensors, monitor the surrounding light intensity & automatically turn ON/OFF the high intensity LED's by taking some pre-defined threshold light intensity value.
6. **Battery Voltage Range Indicator:** Monitor the voltage level of the battery and indicating the same using multiple LED's (for ex: for 3V battery and 3 led's, turn on 3 led's for 2-3V, 2 led's for 1-2V, 1 led for 0.1-1V & turn off all for 0V)
7. **Dice Game Simulation:** Instead of using the conventional dice, generate a random value similar to dice value and display the same using a 16X2 LCD. A possible extension could be to provide the user with option of selecting single or double dice game.
8. **Displaying RSS News Feed On Display Interface:** Displaying the RSS news feed headlines on a LCD display connected to device. This can be adapted to other websites like twitter or other information websites. Python can be used to acquire data from the internet.
9. **Porting Openwrt To the Device:** Attempt to use the device while connecting to a wifi network using a USB dongle and at the same time providing a wireless access point to the dongle.
10. **Hosting a website on Board:** Building and hosting a simple website(static/dynamic) on the device and make it accessible online. There is a need to install server (eg: Apache) and therebyhost the website.
11. **Webcam Server:** Interfacing the regular usb webcam with the device and turn it into fully functional IP webcam & test the functionality.
12. **FM Transmission:** Transforming the device into a regular fm transmitter capable of transmitting audio at desired frequency (generally 88-108 Mhz).

Note: Devices mentioned in the above lists include Arduino, Raspbery Pi, Beaglebone

Course Outcomes:

After the Completion of the course, the students will be able to

1. Demonstrate testing and displaying on devices using Embedded Linux, Arduino, Raspbery Pi Boards.
2. Explain Programming and Interfacing of I/O devices like LED/Switch etc. using Embedded Linux, Arduino, Raspbery Pi Boards.
3. Implement dice game, battery voltage indicator, displaying news using Embedded Linux, Arduino, Raspbery Pi Boards.
4. Experiment the Web Cam Server, FM transmission, and providing wireless access point using Embedded Linux.
5. Build and host a simple website on the device and make it accessible online using Embedded Linux, Arduino, Raspbery Pi, Beaglebone boards.

(B520303) RESEARCH METHODOLOGY & IPR

M.Tech (ES)-I Semester	L	T	P	C
	2	0	0	2

UNIT- I:

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT- II:

Effective literature studies approaches, analysis, Plagiarism, Research ethics

UNIT- III:

Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

UNIT- IV:

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT- V:

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

TEXT BOOKS:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"

REFERENCE BOOKS:

1. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"
2. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
3. Mayall, "Industrial Design", McGraw Hill, 1992.
4. Niebel, "Product Design", McGraw Hill, 1974.
5. Asimov, "Introduction to Design", Prentice Hall, 1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New Technological Age", 2016.
7. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008

COURSE OUTCOMES:

After the Completion of the course, the students will be able to

1. Investigate the solution for research problem
2. Develop the research proposal and paper
3. Describe the process of patenting and development in international scenario
4. Define the patent rights,licencing and transfer of technology
5. Demonstrate the new development in IPR

(B555303) EMBEDDED REAL TIME OPERATING SYSTEM

M.Tech (ES)-II Semester	L	T	P	C
	3	0	0	3

UNIT-I

Introduction to RTOS: Real life examples of embedded systems, real-time embedded systems, the future of embedded systems, a brief history of operating systems, defining an RTOS, the scheduler, objects, services, key characteristics of an RTOS.

UNIT-II

Tasks: Introduction, defining a task, task states and scheduling, typical task operations, typical task structure, synchronization, communication, and concurrency.

Semaphores: Introduction, defining semaphores, typical semaphore operations, typical semaphore use.

Message Queues: Introduction, defining message queues, message queue states, message queue content, message queue storage, typical message queue operations, and typical message queue use.

UNIT-III

Exceptions and Interrupts: Introduction, what are exceptions and interrupts, a closer look at exceptions and interrupts, processing general exceptions, the nature of spurious interrupts.

Timer and Timer Services: Introduction, real-time clocks and system clocks, programmable interval timers, timer interrupt service routines, a model for implementing the soft-timer handling facility, timing wheels, soft timers and timer related operations.

UNIT-IV

Memory Management: Introduction, dynamic memory allocation in embedded systems, fixed-size memory management in embedded systems, blocking vs. non-blocking memory functions, hardware memory management units.

UNIT-V

Modularizing Applications: Introduction, an outside-in approach to decomposing applications, guidelines and recommendations for identifying concurrency, schedulability analysis – rate monotonic analysis.

Common Design Problems: Introduction, resource classification, deadlocks, priority inversion.

TEXT BOOKS:

1. Qing Li, and Caroline Yao. Real-Time Concepts for Embedded Systems. CMP Books, 2003.

REFERENCE BOOKS:

1. Prasad, K. V. K. K. Embedded Real-Time Systems: Concepts, Design & Programming. Dream Tech Press, 2005.
2. Simon, David E. An Embedded Software Primer. 1st ed., 5th impression, Addison-Wesley Professional, 2007.
3. Singh, Rajib Mall. Real-Time Systems: Theory and Practice. Pearson Education India, 2006.

COURSE OUTCOMES

1. Analyse key concepts and roles of real-time operating systems in embedded system design.
2. Evaluate task scheduling and synchronization methods in real-time systems.
3. Design interrupt and timer handling mechanisms for embedded real-time environments.
4. Apply real-time memory management techniques in embedded applications.
5. Create modular real-time applications to resolve deadlocks and priority inversion.

(B555304) IOT SYSTEM DESIGN

M.Tech (ES)-II Semester

L	T	P	C
3	0	0	3

UNIT - I

IoT introduction: Introduction and definition of IoT, Evolution of IoT, IoT growth, Application areas of IoT, Characteristics of IoT, IoT stack, Enabling technologies, IoT levels, IoT sensing and actuation, Sensing types, Actuator types.

UNIT - II

IoT and M2M: M2M to IoT – A Basic Perspective– Introduction, Differences and similarities between M2M and IoT, SDN and NFV for IoT.M2M Value Chains, IoT Value Chains, An emerging industrial structure for IoT, The international driven global value chain and global information monopolies.

UNIT - III

IoT Hands-on: Introduction to Arduino Programming, Integration of Sensors and Actuators with Arduino. Introduction to Python programming, Introduction to Raspberry Pi, Interfacing Raspberry Pi with basic peripherals, Implementation of IoT with Raspberry Pi.

UNIT - IV

IoT Architecture: IoT Architecture components, Comparing IoT architectures, A simplified IoTarchitecture, The core IoT functional stack, IoT data management and compute stack

UNIT - V

IoT System design: Challenges associated with IoT, Emerging pillors of IoT, Agricultural IoT, VehicularIoT, Healthcare IoT, Smart cities, Transportation and logistics.

TEXT BOOKS:

1. Sudip Misra, Anandarup Mukherjee, Arijit Roy “Introduction to IOT”, Cambridge UniversityPress.
2. David Hanes, Gonzalo salgueiro, Patrick Grossetete, Rob barton, Jerome henry “IoTFundamentals Networking technologies, protocols, and use cases for IoT”, Cisco Press

REFERENCE BOOKS:

1. Cuno pfister, “Getting started with the internet of things”, O Reilly Media, 2011
2. Francis daCosta, “Rethinking the Internet of Things: A Scalable Approach to ConnectingEverything”, 1 st Edition, Apress Publications.
3. “Internet of Things concepts and applications”, Wiley
4. Arshdeep Bahga,Vijay Madisetti “Internet of Things A Hands on approach”, Universities Press
5. Shriram K Vasudevan, RMD Sundaram, Abhishek S Nagarajan, “Internet of things” John Wileyand Sons.
6. Massimo Banzi, Michael Shiloh Make: Getting Started with the Arduino, Shroff Publisher/MakerMedia Publishers.

Course Outcomes:

After the Completion of the course, the students will be able to

1. Integrate the sensors and actuator depending on the applications
2. Interface the IoT and M2M with value chains
3. Write Python programming for Arduino, Raspberry Pi devices
4. Understand Various IOT Architectures
5. Design IoT based systems such as Agricultural IoT, Vehicular IoT etc.,

(B555407) GPU ARCHITECTURES
(PROFESSIONAL ELECTIVE – III)

M.Tech (ES)-II Semester	L	T	P	C
	3	0	0	3

UNIT I

GPU architectures: Introduction to the ideas of parallelism and the GPU programming model CPU vs GPU Parallelizing algorithms on paper, First CUDA program**.**

UNIT II

CUDA programming: Hardware of Graphics Processing Units and parallel communication patterns, Brief on GPU architecture, Basics of CUDA C, Floating point precision and support on GPUs.

UNIT III

Parallel primitives and algorithms on GPU: The CUDA programming language will be mastered while learning how to implement these algorithms., Matrix Operations, Stencil – Image Blurring, Filters, GaussJacobi-Finite difference updates for PDEs, Histogram, binning 1, Reduce – Maximum and Minimum – Summation, Prefix-sum (Scan) Algorithm – Radix Sort, Generating Cummulative Distributions, Complex algorithms – N-body solutions.

UNIT IV

Optimizing GPU Applications: Coalesced Memory Transactions, Grid Blocks, Thread Blocks, domain decomposition, Asynchronous Kernels and Multistreaming Possible Items: Libraries on GPU, cuBLAS Thrust, cuFFT, cuRAND, Multi-node GPU processing, Multi-GPU per node processing, CUDA in other languages (Python/Fortran), Scaling.

UNIT V

Deep learning on GPUs: Deep learning on GPUs, Combining graphics and compute, Display the results of computations– Interactive systems, Collision detection with voxelized solid (Gargoyle), Ray tracing in CUDA kernels, or ray tracing cores, Microsoft DXR (DX12 API), Vulkan, NVIDIA OptiX / RTX, NVIDIA Turing: "World's First Ray Tracing GPU"- Quadro RTX, Geforce RTX

REFERENCE BOOKS:

1. GPUs for Graphics: OpenGL 4.0 Shading Language Cookbook, 2nd Edition
2. Jason Sanders, Edward Kandrot, CUDA by Example: An Introduction to General-Purpose GPU Programming, Publisher: Addison-Wesley Professional,2013, 3rd Edition.

COURSE OUTCOMES:

After the Completion of the course, the students will be able to

1. Understand working proficiency with CUDA, algorithmic GPU programming and parallel computing
2. Comprehend with classic scientific computing algorithms and problems
3. Optimize GPU code and debug GPU code
4. Analyze architecture specific details like memory access coalescing,shared memory usage, GPU thread scheduling
5. Apply deep learning algorithms on embedded GPUs

(B555408) VLSI TEST AND TESTABILITY
(PROFESSIONAL ELECTIVE – III)

M.Tech (ES)-II Semester	L	T	P	C
	3	0	0	3

UNIT-I

Basics of Testing and Fault Modeling: Introduction to Testing - Faults in digital circuits - Modeling of faults - Logical Fault Models - Fault detection - Fault location - Fault dominance - Logic Simulation-Types of simulation - Delay models - Gate level Event-driven simulation.

UNIT-II

Test Generation for Combinational and Sequential Circuits: Test generation for combinational logic circuits - Testable combinational logic circuit design - Test generation for sequential circuits - design of testable sequential circuits. Design for Testability

UNIT-III

Design for Testability: Ad-hoc design - Generic scan-based design - Classical scan-based design – System level DFT approaches.

UNIT-IV

Self-Test and Test Algorithms: Built-In Self-Test - Test pattern generation for BIST - Circular BIST- BIST Architectures - Testable Memory Design - Test algorithms - Test generation for Embedded RAMs.

UNIT-V

Fault Diagnosis: Logic Level Diagnosis - Diagnosis by UUT reduction - Fault Diagnosis for Combinational Circuits - Self-checking

TEXT BOOKS:

1. Abramovici, M., M. A. Breuer, and A. D. Friedman. Digital Systems Testing and Testable Design. 1st ed., Jaico Publishing House, 2002.
2. Bushnell, M. L., and V. D. Agrawal. Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits. Illustrated ed., Springer Science & Business Media, 2006

REFERENCE BOOKS

1. Lala, P. K. Digital Circuit Testing and Testability. Academic Press, 2002.
2. Crouch, A. L. Design-for-Test for Digital IC's and Embedded Core Systems. 1st ed., Prentice Hall International, 1999

COURSE OUTCOMES

After the Completion of the course, the students will be able to

1. Identify different types of faults in digital circuits and explain their corresponding logical fault models.
2. Apply test generation techniques to detect faults in combinational and sequential digital circuits.
3. Design scan-based and ad-hoc DFT architectures for improving circuit testability.
4. Implement Built-In Self-Test (BIST) strategies for digital systems and memory blocks.
5. Analyse fault diagnosis techniques to locate and interpret faults in logic-level digital circuits.

(B555409) HARDWARE AND SOFTWARE CO-DESIGN
(PROFESSIONAL ELECTIVE – III)

M.Tech (ES)-II Semester	L	T	P	C
	3	0	0	3

UNIT - I

Co-Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co-Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT - II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT - III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT - IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT - V

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi-language co-simulation, the cosyma system and lycos system.

TEXT BOOKS

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf –Springer, 2009.

REFERENCE BOOKS

1. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, Kluwer Academic Publishers, 2002.
2. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont, Springer,2010

COURSE OUTCOMES:

After the Completion of the course, the students will be able to

1. Acquire the knowledge on various models of Co-design.
2. Explore the interrelationship between Hardware and software in a embedded system
3. Acquire the knowledge of firmware development process and tools during Co-design.
4. Implement validation methods and adaptability.
5. Explain the design of system level specification languages

(B555410) HARDWARE SECURITY IN VLSI DESIGN

(PROFESSIONAL ELECTIVE – IV)

M.Tech (ES)-II Semester	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

UNIT I

Introduction to Hardware Security: Overview of a computing system, layers of a computing system, hardware security vs. hardware trust, attacks, vulnerabilities and countermeasures, conflict between security and test/debug, evolution of hardware security, overview of electronic hardware – nanoscale technologies, ASICs and FPGAs, printed circuit board, embedded systems, hardware-firmware- software interaction.

UNIT II

Hardware Trojans: Introduction, SoC design flow, hardware trojans, hardware trojans in FPGA designs, hardware trojans taxonomy, trust benchmarks, countermeasures against hardware trojans, hardware trojan attacks.

Hardware IP Piracy and Reverse Engineering: Introduction, hardware intellectual property (IP), security issues in IP-based SoC design, security issues in FPGA, reverse engineering and tampering.

UNIT III

Side-Channel Attacks: Introduction, taxonomy of side-channel attacks, uncommon side-channel attacks, power analysis attacks, electromagnetic (EM) side-channel attacks, fault-injection attacks, timing attacks.

Test-Oriented Attacks: Introduction, scan-based attacks, JTAG-based attacks.

UNIT IV

Physical Attacks and Countermeasures: Introduction, reverse engineering, probing attack.
Attacks on PCB: Security challenges, attack models, bus snooping attack.

UNIT-V

Hardware Security Primitives: Introduction, physical unclonable functions (PUFs), true random number generator (TRNG), design of anti-counterfeit, existing challenges and attacks.

Security and Trust Assessment: Security assets and attack models, pre-silicon and post-silicon security and trust assessment.

TEXT BOOKS:

1. Bhunia, Swarup, and Mark M. Tehranipoor. Hardware Security: A Hands-on Learning Approach. 1st ed., Academic Press, 2019.

REFERENCE BOOKS:

1. Tehranipoor, Mark, and Cliff Wang, editors. Introduction to Hardware Security and Trust. Springer, 2012.
2. Bhunia, Swarup, and Sandip Ray. Fundamentals of IP and SoC Security: Design, Verification, and Debug. Springer, 2017.
3. Wolf, Marilyn. Embedded System Interfacing: Design for the Internet-of-Things (IoT). Morgan Kaufmann, 2019.
4. Skorobogatov, Sergei. Semi-Invasive Attacks: A New Approach to Hardware Security Analysis. Springer, 2007.

COURSE OUTCOMES:

After the Completion of the course, the students will be able to

1. Identify and explain the key layers and components of VLSI systems vulnerable to hardware attacks.
2. Analyse different types of hardware Trojans and IP piracy techniques and suggest appropriate countermeasures.
3. Evaluate side-channel and test-oriented attacks on SoC and FPGA-based systems using suitable models.
4. Demonstrate an understanding of physical attacks and PCB vulnerabilities through attack modeling and analysis.
5. Design and implement hardware security primitives such as PUFs and TRNGs to protect VLSI designs from cloning and counterfeiting.

(B555411) HARDWARE ACCELERATORS FOR MACHINELEARNING MODELS (PROFESSIONAL ELECTIVE – IV)

M.Tech (ES)-II Semester

L	T	P	C
3	0	0	3

UNIT- I

Overview of DNNs: Convolutional Neural Networks (CNNs), Popular DNN Models, DNN development resources: Frameworks, Models, Popular Data Sets for Classification, And Data Sets for Other Tasks

Evolution of hardware platforms for Deep Learning: CPUs, GPUs, FPGAs, DSPs, accelerators; Hardware considerations in inference and training, Accelerate Kernel Computations on CPU and GPU Platforms, Energy-Efficient Dataflow for Accelerators, DNN data handling characteristics, Weight Stationary (WS), Output Stationary (OS), No Local Reuse (NLR), Row Stationary (RS). Accelerating the convolution operation: Algorithms, Data flow patterns, Memory reuse Case-study on writing a custom GPU

UNIT- II:

Kernel for accelerating convolution, optimizing networks: Weight quantization, network compression, sparse operations, zero forwarding, learning with hardware in the loop, learning and inference on low-memory devices.

UNIT – III

Memory and compute: Optimizations to CNNs such as tiling, loop optimizations, batching, quantization, pruning, Cache Blocking, four convolution strategies (Direct, GEMM, FFT and Winograd), Model-size aware and system-aware pruning of CNNs, MLPerf Benchmark for evaluating DNN accelerators.

UNIT- IV

Near-data processing: DRAM, SRAM, Non-volatile Resistive Memories, Sensors, co-design of DNN models and hardware: Reduce Precision, Reduced Number of Operations and Model Size. Benchmarking metrics DNN evaluation and comparison, Metrics for DNN Models, Metrics for DNN Hardware.

UNIT-V

Deep Learning on Systolic Array and Tensor Processing Unit (TPU) v1 to v4, Distinct Characteristics of Training and Inference, Architectures of TPU v1, v2, v3 and v4; comparison between their architectures, Comparison of CPU, TPU and GPU, Deep Learning on FPGA and Microsoft's Brainwave Architecture, Deep Learning techniques on FPGA; efficacy of FPGAs for binarized neural networks (BNNs).

TEXT BOOKS:

1. Shiho Kim, Ganesh Chandra Deka,Hardware Accelerator Systems for Artificial Intelligence and Machine Learning, Volume 122 - March 28, 2021, 1st Edition,

REFERENCE BOOKS:

1. V. Sze, Y. -H. Chen, T. -J. Yang and J. S. Emer, "Efficient Processing of Deep Neural Networks: A Tutorial and Survey," in Proceedings of the IEEE, vol. 105, no. 12, pp. 2295-2329, Dec. 2017, doi:10.1109/JPROC.2017.2761740.
2. https://docs.amd.com/r/2022.2-English/ug896-vivado-ip/Xilinx-Resources

Course Outcomes:

After the Completion of the course, the students will be able to

1. Explore the various DNN models and development resources.
2. Understand the hardware implementation strategies for DNN.
3. Develop the memory optimization and computational optimization techniques to DNN.
4. Perform the near-data processing and benchmark evaluation to DNN models.
5. Design and implement the accelerator logic to DNN models.

(B555412) IMAGE AND VIDEO PROCESSING
(PROFESSIONAL ELECTIVE – IV)

M.Tech (ES)-II Semester	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

UNIT I

Fundamentals of Image Processing: Basic steps of Image processing system sampling and quantization of an Image – Basic relationship between pixels

Image Transforms: 2 – D Discrete Fourier Transform, Discrete Cosine Transform (DCT), Introduction to wavelet Transform, Continuous wavelet Transform, Discrete wavelet Transform, Filter banks

UNIT II

Image Enhancement:

Spatial Domain Methods: Histogram Processing, Fundamentals of Spatial Filtering, Smoothing Spatial filters, Sharpening Spatial filters

Frequency domain methods: basics of filtering in frequency domain, image smoothing, image sharpening, selective filtering.

UNIT III

Segmentation: Segmentation concepts, Point, Line and Edge Detection, Edge Linking using Hough Transform, Thresholding, Region Based segmentation.

Morphological Image Processing

Dilation and Erosion, Opening and closing, the hit or miss Transformation, Overview of Digital Image Watermarking Methods

UNIT IV

Image Compression: Image compression fundamentals – Coding Redundancy, Spatial and Temporal Redundancy. Compression Models: Lossy and Lossless, Huffmann Coding, Arithmetic Coding, LZW Coding, Run Length Coding, Bit Plane Coding, Transform Coding, Predictive Coding, Wavelet Coding, Wavelet Based Image Compression, JPEG standards.

Image Restoration: Degradation Models, PSF, Circulant And Block - Circulant Matrices, Deconvolution, Restoration Using Inverse Filtering, Wiener Filtering.

UNIT V

Basic Steps of Video Processing: Analog video, Digital Video, Time varying Image Formation Models: 3D Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video Signals, Filtering Operations

2-D Motion Estimation: Optical Flow, General Methodologies, Pixel Based Motion Estimation, Block Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi Resolution Motion Estimation. Waveform based Coding, Block based Transform Coding, Predictive Coding, Application of Motion Estimation in video Coding. Overview of motion compensated hybrid coding (MPEG & H-264)

TEXT BOOKS:

1. Digital Image Processing, Gonzaleze and Woods, 3rd Edition, Pearson
2. Video Processing and Communication, Yao Wang, Joern Ostermann and Ya-Qin Zhang, 1st Edition, Prentice Hall
3. Digital Video Processing, M. Tekalp, Prentice Hall International

REFERENCE BOOKS:

1. Digital Signal Processing: Principles, Algorithms & Applications, J. G. Proakis& D. G. Manolokis, 4th Edition, PHI, 2001
2. Adaptive Filter Theory, S. Haykin Pearson, 2003
3. DSP–A Practical Approach, Emmanuel C. I. Feacher, Barrie W. Jervis, 2nd Edition, Pearson Education, 2008
4. Modern Spectral Estimation: Theory & Application, S. M. Kay, 1988, PHI
5. H-264 & MPEG-4 Video Compression, Video Coding for Next Generation multimedia, I. E. Richardson, John Wiley & Sons, 2009

Course Outcomes:

After the Completion of the course, the students will be able to

1. Understand the fundamentals of digital image processing
2. Appreciate the advantages of compression in image /video processing
3. Understand the concepts of video formation, sampling and representation
4. Understand the principles of motion estimation in a video
5. Analyze the principles of multi-dimensional estimation with reference to a video signal.

(B555503) EMBEDDED REAL TIME OPERATING SYSTEM LABORATORY

M.Tech (ES)-II Semester	L	T	P	C
	0	0	4	2

List of Experiments:

Develop program in Linux for the following:

1. Develop a program utilizing command line arguments (argc and argv)
2. Create new process using fork( ).
3. Communicate between parent and child process using pipes.
4. Communicate between parent and child process using FIFOs
5. Develop a program to communicate between processes using message queue.
6. Develop a program using system calls that is similar to 'cp' command.
7. Create a new thread using POSIX Thread library
8. Develop a program to demonstrate the use of synchronizing access to shared resource using semaphores. (POSIX Thread based)
9. Develop a program to demonstrate the use of synchronizing access to shared resource using mutex. (POSIX Thread based)
10. Develop a program to demonstrate the use of signaling semaphore for sending event from one thread to another. (POSIX Thread based)

Course Outcomes:

After the Completion of the course, the students will be able to

1. Apply various real time concepts in building embedded systems
2. Implement the RTOS development tools in building real time embedded Systems
3. Appreciate the necessity of Inter Process Communication and Synchronization mechanisms
4. Apply the concept of RTOS in the designing of real time systems

(B555504) IOT SYSTEM DESIGN LABORATORY

M.Tech (ES)-II Semester	L	T	P	C
	0	0	4	2

List of Experiments:

1. Micro-Controller Programming
2. Single-board Computer Programming
3. Posting Data to an IoT Cloud Platform
4. Connecting an IoT Gateway to an IoT Cloud
5. Connecting a Sensor Node to IoT Gateway
6. End to End Full Stack IoT Development
7. Introduction to Wireshark on Raspberry Pi
8. Programming Arduino with Blockly
9. Programming Raspberry Pi with Python
10. Bluetooth Low Energy (BLE) Based Systems
11. RFID and NFC Based Tracking
12. Multimedia Communication
13. Microcontroller Programming Simulator
14. Advance Sensors, Actuators, Components
15. Getting Started with Raspberry Pi Camera
16. Debugging the Raspberry Pi

Course Outcomes:

After the Completion of the course, the students will be able to

1. Program microcontrollers and single-board computers for sensor and actuator interfacing.
2. Build and deploy complete IoT systems with cloud connectivity.
3. Use tools and protocols for IoT communication, including BLE, RFID, and NFC.
4. Simulate, debug, and enhance IoT applications using Raspberry Pi and related tools.

(B555413) MACHINE LEARNING FOR ROBOTICS
(PROFESSIONAL ELECTIVE – V)

M.Tech (ES)-III Semester	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

UNIT I

Introduction to Robotics: Types and Classification of robots; Science and Technology of Robots Rigid Body Transformation: Overview of Rigid Body Kinematics; Homogeneous Transformation; Link Transformation Matrices, Forward and Inverse Kinematics & Dynamics of Robots, Planning and Control of Robots,Robotic vision sensors and their interfacing

UNIT II

Fundamentals of Computer Vision: Image acquisition and representation, image transformation, filtering, restoration, morphing, Camera Models, Calibration, Single view geometry, Multiple view geometry, Epipolar geometry, RANSAC

UNIT III

Position and Orientation: Feature-based alignment; Pose estimation; Time-varying pose and trajectories, Structure from motion, dense Motion Estimation, Visual Odometry (Semi-direct VO, direct sparse odometry), Bundle Assignment

UNIT IV

Localization and Mapping: Initialization, Tracking, Mapping, geometric SLAM formulations (indirect vs. direct error formulation, geometry parameterization, sparse vs. dense model, optimization approach), Relocalization and map Optimization, Visual SLAM, Examples: Indirect (Feature based) methods (MonoSLAM, PTAM, ORB-SLAM), Direct methods (DTAM, LSD- SLAM), Sensor combinations (IMU, mono vs. stereo, rgb-depth), analysis and parameter studies.

UNIT V

Recognition and Interpretations: Concepts of machine learning and deep learning, sequence modeling, Learning for robotic vision

TEXT BOOKS

1. Fu. K.S., Gonzalez R.C. and Lee C.S.G., Robotics: Control, Sensing, Vision and Intelligence, Tata McGraw Hill, 2008,ISE Edition.
2. Ghosal A. Robotics: Fundamental Concepts and Analysis, Oxford University Press, 2006, 1st Edition.

REFERENCE BOOKS

1. H. R. Everett, Sensors for Mobile Robots: Theory and Application, A K Peters/CRC Press, 1995, 1st Edition.
2. Dahiya, Ravinder S., Valle, Maurizio, Robotic Tactile Sensing, Springer, 2013.

Course Outcomes:

After the Completion of the course, the students will be able to

1. To explain different types of Embedded communication protocols
2. To interface USB and CAN Bus based on data flow rate
3. To identify the elements of Networks and their design choices
4. To Exchange the messages using UDP of TCP Protocols
5. To Establish a WSN for the embedded applications

(B555414) EDGE COMPUTING
(PROFESSIONAL ELECTIVE – IV)

M.Tech (ES)-III Semester	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

UNIT I

Introduction to Cloud and its limitations to support low latency and RTT. From Cloud to Edge computing: Waves of innovation, Introduction to Edge Computing Architectures

UNIT II

Edge Computing to support User Applications (5G-Slicing, self-driving cars and more). Concepts of distributed systems in edge computing such as time ordering and clock synchronization, distributed snapshot, etc.

UNIT III

Introduction to Edge Data Center, Lightweight Edge Clouds and its services provided by different service providers. Introduction to Dockercontainers and Kubernetes in edge computing. Design of edge storage systems like key-value stores

UNIT IV

Introduction to MQTT and Kafka for an end-to-end edge pipeline. Edge analytics topologies for M2M and WSN network (MQTT).

UNIT V

Use cases of machine learning for edge sensor data in predictive maintenance, image classifiers and self-driving cars. Deep Learning On-Device inference at the edge to support latency-based applications.

TEXT BOOKS:

1. Cloud Computing: Principles and Paradigms", Editors: Rajkumar Buyya James Broberg,Andrzej M. Goscinski, Wiley, 2011
2. "Fog and Edge Computing: Principles and Paradigms", Rajkumar Buyya (Editor), Satish Narayana Srirama (Editor), Wiley, 2019.
3. "Cloud and Distributed Computing: Algorithms and Systems", Rajiv Misra, Yashwant Patel, Wiley 2020.

Course Outcomes:

After the Completion of the course, the students will be able to

1. Understand the fundamentals of edge computing, its architecture, and its role in low-latency, real-time applications
2. Analyze and implement distributed data analytics techniques and edge-cloud frameworks for intelligent data processing
3. Gain hands-on experience with edge computing technologies such as Docker, Kubernetes, MQTT, Kafka, and time synchronization
4. Apply machine learning and deep learning models in edge scenarios such as autonomous systems, predictive maintenance, and reinforcement learning

(B555415) EMBEDDED BIOMEDICAL APPLICATION
(PROFESSIONAL ELECTIVE – IV)

M.Tech (ES)-III Semester	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

UNIT I
INTRODUCTION TO BIOMEDICAL ENGINEERING: Origin of bio potential and its propagation- Resting and Action Potential – Bio signals characteristicsTypes of electrodes - Types of transducers and applications-Bio-amplifiers- Types of recorders, components of a biomedical system.

UNIT II:
WEARABLE HEALTH DEVICES: Concepts of wearable technology in health care-Components of wearable devices- Biosensors- Blood glucose sensors - Head worn- Hand worn- Body worn- pulse oxymeter- Cardiac pacemakers – Hearing aids and its recent advancements-wearable artificial kidney.

UNIT III:
EMBEDDED SYSTEM FOR MEDICAL IMAGE PROCESSING: Introduction to embedded image processing. ASIC vs FPGA - memory requirement-, power consumption- parallelism - Design issues in VLSI implementation of Image processing algorithms - interfacing. Hardware implementation of image processing algorithms: Segmentation and compression

UNIT IV:
EMBEDDED SYSTEM FOR DIAGNOSTIC APPLICATIONS: ICCU patient monitoring system – ECG-EEG-EMG acquisition system-MRI scanner - CT scanner Sonography

UNIT V:
CASE STUDY: Respiratory measurement using spirometer- IPPB unit for monitoring respiratory parameters - ventilators- -Defibrillator- Glucometer-Heart- Lung machine.

TEXT BOOKS:

1. Leslie Cromwell, “Biomedical Instrumentation and Measurement”, Prentice Hall of India New Delhi, 2007.
2. John G.Webster, “Medical Instrumentation Application and Design”, 3rd Edition, Wiley India Edition, 2007.
3. Khandpur R.S, Handbook of Biomedical Instrumentation, Tata McGraw Hill, New Delhi, 3rd Edition, 2014.
4. L.A Geddes and L.E.Baker, Principles of Applied Biomedical Instrumentation, 3rd Edition John Wiley and Sons, Reprint 2008.
5. Richard S.Cobbold, Transducers for Biomedical Measurements; Principle and applicationsJohn Wiley and sons, 1992.

Course Outcomes:

After the Completion of the course, the students will be able to

1. Demonstrate the fundamental art of biomedical engineering.
2. Illustrate about wearable health devices and its importance.
3. Implement image processing applications using software and hardware.
4. Compare various embedded diagnostic applications.
5. Build and analyze of some biomedical equipment

(B500701) ENGLISH FOR RESEARCH PAPER WRITING
(Audit Course - I & II)

M.Tech (ES)	**L**	**T**	**P**	**C**
	2	**0**	**0**	**0**

UNIT-I:
Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT-II:
Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction

UNIT-III:
Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

UNIT-IV:
key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills areneeded when writing an Introduction, skills needed when writing a Review of the Literature,

UNIT-V:
skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions. useful phrases, how to ensure paper is as good as it could possibly be the first- time submission

TEXT BOOKS/ REFERENCES:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman'sbook.
4. Adrian Wallwork, English for Writing Research Papers, Springer New York DordrechtHeidelberg London, 2011

(B500702) DISASTER MANAGEMENT
(Audit Course - I & II)

M.Tech (ES)	L	T	P	C
	2	0	0	0

UNIT-I:

Introduction:

Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

Disaster Prone Areas in India:

Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics

UNIT-II:

Repercussions of Disasters and Hazards:

Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

UNIT-III:

Disaster Preparedness and Management:

Preparedness: Monitoring of Phenomena Triggering A Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT-IV:

Risk Assessment Disaster Risk:

Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

UNIT-V:

Disaster Mitigation:

Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

TEXT BOOKS/ REFERENCES:

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'NewRoyal book Company.
2. Sahni, Pardeep Et. Al. (Eds.)," Disaster Mitigation Experiences and Reflections", Prentice Hall ofIndia, New Delhi.
3. Goel S. L., Disaster Administration and Management Text and Case Studies", Deep &Deep Publication Pvt. Ltd., New Delhi

(B500704) VALUE EDUCATION
(Audit Course - I & II)

M.Tech (ES)	**L**	**T**	**P**	**C**
	2	**0**	**0**	**0**

UNIT-I:
Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism. Moral and non- moral valuation. Standards and principles. Value judgements

UNIT-II:
Importance of cultivation of values. Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Unity. Patriotism. Love for nature, Discipline

UNIT-III:
Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline, Punctuality, Love and Kindness.

UNIT-IV:
Avoid fault Thinking. Free from anger, Dignity of labour. Universal brotherhood and religious tolerance. True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits. Association and Cooperation. Doing best for saving nature

UNIT-V:
Character and Competence –Holy books vs Blind faith. Self-management and Good health. Science of reincarnation, Equality, Nonviolence, Humility, Role of Women. All religions and same message. Mind your Mind, Self-control. Honesty, Studying effectively

TEXT BOOKS/ REFERENCES:
1. Chakroborty, S.K. “Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi

Course outcomes: Students will be able to
1. Knowledge of self-development
2. Learn the importance of Human values
3. Developing the overall personality

(B500705) CONSTITUTION OF INDIA
(Audit Course - I & II)

M.Tech (ES)	**L**	**T**	**P**	**C**
	2	**0**	**0**	**0**

UNIT-I:
History of Making of the Indian Constitution: History Drafting Committee, (Composition & Working),
Philosophy of the Indian Constitution: Preamble**,** Salient Features.

UNIT-II:
Contours of Constitutional Rights & Duties: Fundamental Rights Right to Equality**,** Right to Freedom**,** Right against Exploitation**,** Right to Freedom of Religion**,** Cultural and Educational Rights**,** Right to Constitutional Remedies, Directive Principles of State Policy**,** Fundamental Duties.

UNIT-III:
Organs of Governance: Parliament**,** Composition**,** Qualifications and Disqualifications**,** Powers and Functions**,** Executive**,** President**,** Governor**,** Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualification, Powers and Functions.

UNIT-IV:
Local Administration: District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy.

UNIT-V:
Election Commission: Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners. State Election Commission: Role and Functioning. Institute and Bodies for the welfare of SC/ST/OBC and women.

TEXT BOOKS/ REFERENCES:

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

Course Outcomes: Students will be able to:

1. Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
2. Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
3. Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
4. Discuss the passage of the Hindu Code Bill of 1956.

(B555601) EMBEDDED SYSTEMS
(Open Elective)

	L	T	P	C
M.Tech (ES)	**3**	**0**	**0**	**3**

UNIT-I: Embedded Computing & CPU fundamentals

Embedded Computing: Microprocessors, embedded design process, system description formalisms. Instruction sets- CISC and RISC;

CPU fundamentals: programming I/Os, co-processors, supervisor mode, exceptions, memory management units and address translation, pipelining, super scalar execution, caching, CPU power consumption.

UNIT-II: **Embedded computing platform & Program design and analysis**

Embedded Computing platform: CPU bus, memory devices, I/O devices, interfacing, designing with microprocessors, debugging techniques.

Program design and analysis: models of program, assembly and linking, compilation techniques, analysis and optimization of execution time, energy, power and size.

UNIT-III: Processes and operating systems

Multiple tasks and multiple processes, context switching, scheduling policies, inter-process communication mechanisms.

UNIT-IV: Hardware accelerators & Networks

Hardware accelerators:CPUs and accelerators, accelerator systemdesign.

Networks: Distributed embedded architectures, networks for embedded systems, network-based design and Internet-enabled systems.

UNIT-V: System design techniques

Design methodologies, requirements analysis, system analysis andarchitecture design, quality assurance.

Text Books:

1. Wolf, W. Computers as components- Principles of embeddedcomputing system design. Academic Press (Indian edition available from Harcourt India Pvt. Ltd., 27M Block market, Greater Kailash II,New Delhi-110 048.)

Reference Books

1. Manuel Jiménez Rogelio, PalomeraIsidoro Couvertier “Introduction to Embedded Systems Using Microcontrollers and the MSP430” Springer Publications, 2014.
2. Frank Vahid, Tony D. Givargis, “Embedded system Design: A Unified Hardware/Software Introduction”, John Wily & Sons Inc.2002.
3. Peter Marwedel, “Embedded System Design”, Science Publishers, 2007.

Course Outcomes:

After the Completion of the course, the students will be able to

1. Explain the Embedded design process and CPU Fundamentals
2. Understand Embedded computing platform and program design.
3. Explain Scheduling policies and inter process mechanisms in Embedded systems
4. Evaluate the Hardware accelerators & networks for Embedded system.
5. Explain various System design methodologies and quality assurance.

(B543601) PHOTOVOLTAIC SYSTEMS
(Open Elective)

	L	T	P	C
M.Tech (ES)	**3**	**0**	**0**	**3**

UNIT-I: SOLAR ENERGY Sun and Earth, Solar Spectrum, Solar Geometry, Solar radiation on horizontal and inclined planes, Instruments for measurement of solar radiation, Solar cell, Equivalent circuit, V-I characteristics, Performance improvement.

UNIT-II: **SOLAR CELLS** Manufacture of Solar Cells-Technologies, Design of Solar cells, Photovoltaic modules, Design requirements, Encapsulation systems, Manufacture, Power rating, Hotspot effect, Design qualifications.

UNIT-III: **PROTECTION AND MEASUREMENTS** Flat plate arrays, Support structures, Module interconnection and cabling, Lightning protection, Performance measurement using natural sun light and simulator, Determination of temperature coefficients, Internal series resistance, Curve correction factor.

UNIT-IV: **PHOTOVOLTAIC SYSTEMS** Photovoltaic systems, Types, General design considerations, System sizing, Battery sizing, Inverter sizing, Design examples, Balance of PV systems.

UNIT-V: **MAXIMUM POWER POINT TRACKERS** Maximum power point trackers, Perturb and observe, Incremental conductance method, Hill climbing method, , Hybrid and complex methods, Data based and other approximate methods, Instrument design, Other MPP techniques, Grid interactive PV system.

TEXTBOOKS: 1. F.C.Treble, "Generating electricity from Sun", Pergamon Press. 2. A.K.Mukherjee, Nivedita Thakur," Photovoltaic systems: Analysis and design", PHI, 2011.

REFERENCES: 1. C.S.Solanki," Solar Photovoltaic's: Fundamentals, Technologies and applications", PHI, 2009.

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Identify photovoltaic system components and system types
2. Calculate electrical energy and power
3. Correctly size system components, design considerations of solar equipment
4. Design a basic grid-tie PV system

(B520601)GREEN BUILDING TECHNOLOGIES
(Open Elective)

	L	T	P	C
M.Tech (ES)	**3**	**0**	**0**	**3**

UNIT- I Introduction Environmental implications of buildings energy, carbon emissions, water use, waste Disposal. Building materials: sources, methods of production and environmental Implications. Green cover and built environment.

UNIT- II Implications of Resources Implication of resources for Building Materials and alternative concepts. Recycling of Industrial and Building Wastes. Biomass Resources for buildings.

UNIT- III Comforts in Building Comforts in Building: Thermal Comfort in Buildings-Issues; Heat Transfer Characteristics of Building Materials and Building Techniques. Incidence of Solar Heat on Buildings.

UNIT- IV Energy Conservation Utility of Solar energy is buildings concepts of Solar Passive Cooling and Heating of Buildings. Low Energy Cooling. Case studies of Solar Passive Cooled and Heated Buildings.

UNIT- V Green Composites for Buildings & Waste Management Green Composites for buildings. Concepts of Green Composites. Water Utilization in Buildings. Waste Management: Low Energy Approaches to Water Management, Management of Solid Wastes, Management of Sullage water and Sewage.

TEXT BOOKS:

1. K.S. Jagadish, B.U. Venkatarama Reddy and K.S. Nanjundarao. Alterative Building Materials and Technologies. New Age International, 2007. R22 B.Tech. Civil Engineering JNTUH Hyderabad Page 85 of 132

2. Michael Bauer, Peter Mosle and Michael Schwarz “Green Building-Guide book for Sustainable Architecture “Springer, 2010.

REFERENCE BOOKS:

1. Osman Attmann Green Architecture Advanced Technologies and Materials. McGraw Hill, 2010.
2. Michael F. Ashby Materials and the Environment, Elsevier, 2009.
3. Jerry Yudelson Green building Through Integrated Design McGraw Hill, 2009.
4. Mili M.Ajumdar (Ed) Energy Efficient Building in India. Teri and Mnes, 2001/2002
5. Low Energy Cooling for Sustainable Buildings John Wiley and Sons Ltd. 2009.
6. Green My Home’: 10 Steps to Lowering Energy Costs and Reducing Your Carbon Footprint by Dennis.
7. C. Brewer, ISBN: 97814227798411, Publisher: Kaplan Publishing. Publications Date
8. B. Givoni Man, Climate and Architecture Elsevier, 1969. 9. T. A Markus and E. N. Morris Buildings Climate and Energy. Pitman, London Arvindkishan et al (Ed)

(B558601) INTRUSION DETECTION SYSTEMS
(Open Elective)

	L	T	P	C
M.Tech (ES)	**3**	**0**	**0**	**3**

UNIT - I The state of threats against computers, and networked systems-Overview of computer security solutions and why they fail-Vulnerability assessment, firewalls, VPN's -Overview of Intrusion Detection and Intrusion Prevention, Network and Host-based IDS

UNIT - II Classes of attacks - Network layer: scans, denial of service, penetration Application layer: software exploits, code injection-Human layer: identity theft, root access-Classes of attackers-Kids/hackers/sop Hesitated groups-Automated: Drones, Worms, Viruses

UNIT - III A General IDS model and taxonomy, Signature-based Solutions, Snort, Snort rules, Evaluation of IDS, Cost sensitive IDS

UNIT - IV Anomaly Detection Systems and Algorithms-Network Behavior Based Anomaly Detectors (rate based)-Host-based Anomaly Detectors-Software Vulnerabilities-State transition, Immunology, Payload Anomaly Detection

UNIT - V Attack trees and Correlation of alerts- Autopsy of Worms and Botnets-Malware detection - Obfuscation, polymorphism- Document vectors. Email/IM security issues-Viruses/Spam-From signatures to thumbprints to zero day detection-Insider Threat issues-Taxonomy-Masquerade and Impersonation Traitors, Decoys and Deception-Future: Collaborative Security

TEXT BOOKS:

1. Peter Szor, The Art of Computer Virus Research and Defense, Symantec Press ISBN 0-321- 30545-3.
2. Markus Jakobsson and Zulfikar Ramzan, Crimeware, Understanding New Attacks and Defenses.

REFERENCE BOOKS:

1. Saiful Hasan, Intrusion Detection System, Kindle Edition.
2. Ankit Fadia, Intrusion Alert: An Ethical Hacking Guide to Intrusion Detection